Design of Router using Black-Bus Architecture

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Abstract—Network-on-a-Chip (NoC) has become popular as a high-performance interconnect, especially in comparison with the traditional buses, which cannot transfer more than one data-stream simultaneously, are more likely to become a bottleneck. In traditional routers, each intermediate node has a buffer capable of storing a flit. But the problem of buffer deadlock occurs when the buffers are full. In this paper, we propose a novel data-transfer method called Black-Bus as a NoC and the use of First-In-First-Out (FIFO) queue. In Black-Bus, a local identifier (ID) is attached to each raw data as routing information. Unlike the traditional packet transfer, the local ID is transferred on dedicated wires attached to data lines to remove complicated packet generation procedure in a node. Only a small-sized local ID is required to specify routing tags to the destination, and intermediate routers change it to solve local ID conflicts between paths on a physical channel. Evaluation results show that in a 16-node system, most of the applications require only at most 3 bits for the local ID. And thus the Black-Bus data-transfer reduces up to 75% of routing tags compared with global addressing scheme used in the traditional packet networks.

Index Terms—router, FIFO, Black-Bus, Network-on-a-Chip, on-chip interconnect, X-Y routing, Systems-on-a-Chip, table-lookup routing.

I. INTRODUCTION

The connection between IP cores and processors in a System-on-a-Chip is established by On-chip interconnects, which are responsible for performance and hardware cost. An SoC bus has been widely used as an on-chip interconnect, which is the method for transferring data. These buses are shared by all the connected modules over common wires [1][2][3]. NoC[5] borrows networking structure used in computer network, parallel computer, or System Area Networks(SANs)[6] [7] [8] [9] and serves as an on-chip interconnect. In traditional NoC schemes, packet comprised of data along with a header at a source node which was supposed to be decomposed at the destination which burdened the node heavily. This burden of complicated network interface cannot be ignored especially in case of some recent SoCs or dynamic reconfigurable processor arrays [10] [11] consisting of the large number of components.

In this paper, we propose a FIFO queued on-chip interconnects called Black-Bus for SoCs or dynamic reconfigurable processor arrays with a large number of components. It employs a FIFO instead of packet buffer, which are used in traditional router. Also network router is employed internally, while sender and receiver nodes can treat as if were a dedicated bus. This results in smaller hardware on the routers and simpler network interface in each node.

Distinguished features of the proposed router are summarized as follows:

A. In Black-Bus, with the introduction of a local identifier (ID), the need for generation of packet header, and pack data into a certain length body is eliminated.

B. In most of the cases, the traffic patterns and pats are pre-analyzed, since most NoCs are designed for dedicated purposes [12]. Using local ID other than global address to specify destination, the amount of required bits is reduced.

C. Black-Bus data-transfer is independent of network topology.

D. The use of FIFO in place of in-port buffers enables the deadlock-free routing by queuing of the intermediate data even when the output node is not free.

The rest of paper is organized as follows. In Section II, Black-Bus data-transfer is proposed. In Section III, evaluation results are shown, and in Section IV, the conclusion and the future work are presented.

II. BLACK-BUS DATA-TRANSFER

A. Basic Architecture and Data Transfer Scheme

Figure 1 shows our target architecture using Black-Bus and FIFO. It is an example of SoCs with a large number of components, reconfigurable processor arrays [10] [16], or chip-multiprocessors with simple node structure [11].

The objectives of Black-Bus are (1) removal of complicated network interface controller on nodes, and (2) sending raw data like conventional buses or dedicated wires. All the physical channels between nodes and routers, and all the physical channels between routers are connected using wires and so these objectives can be achieved.

A packet is transferred as follows:

1. A node outputs raw data with a local ID. The local ID can be generated by using the ID table in the node. This eliminates the procedure of generating a packet header in a node, as well as pucking data into...
2. After arrival of the raw data with the local ID at a router, it obtains its output port number and output local ID by referring a routing table in the router.

3. After being transferred from the output port in a router, the connecting node or router can receive the raw data with its local ID.

4. Even if the target neighboring node FIFO is full due to non-release of the required output port, the intermediate FIFO starts writing the data in its memory and thus the deadlock-free routing is achieved.

5. When the destination node receives the raw data and its local ID, its ID table finds its source node corresponding to its input local ID and completes the data transfer.

Comparison of FIFO and packet buffer

Case: If the buffer is occupied, the transmitting router keeps the data and waits for the target buffer being released. While in FIFO, it stores the data into its allotted memory and releases on first-in-first-out basis.

B) Static Analysis of the Routing paths

An NoC designed for specific purpose can be easily analyzed for communicating pairs and their paths after task mapping. Firstly, analysis of the routing paths is done as shown below.

1. Associate counters to all the physical channels, and they are initialized to zero.
2. Select a communication pair of nodes from all the communication pairs, which are still not traced.
3. Search its path based on a deterministic routing algorithm.
4. Increment counters of the physical channels that the path includes.

With this analysis, the maximum number of data streams, which share the same physical channel, is derived.

Figure 2 shows an example of the static analysis of routing paths on the mesh topology with e-cube routing[14], under the complement traffic pattern[20]. As shown in Figure 2, there are 16 paths, (0, 15), (1, 14), (2, 13), . . . , (15, 0), where (x, y) stands for a path from node x to node y. In this pattern, there exist at most two paths for each physical channel.

Consider the case path (4, 11) has the local IDs 0, 0, 1, 0 on router 4, 8, 9, 10, while path (5, 10) has the local IDs 0, 0 on router 5, 9, 10 respectively. Note that the different local IDs must be allocated for eliminating the conflict.
Figure 2: All paths in mesh with X-Y routing under complement traffic pattern

For example, in Figure 2, path (4, 11), and (5, 10) must have different IDs in the physical channel between node 9 and 10, while path (0, 15), (1, 14) or (1, 14), (5, 10) also must have different IDs respectively. That is, the path (4, 11) uses different local ID on the physical channel 9 → 10. This ID modification can be implemented easily on the intermediate Black-Bus router, since dedicated wires are used for the local ID transfer as shown in Figure 1 and 3.

Figure 3 shows an example of FIFO queued Black-Bus router structure. Assuming two-dimensional mesh in Figure 3, it has five I/O ports, where four of them are connected to neighboring routers, and the remaining one is connected to the local node. It consists of FIFO, distributed local ID tables, and a 5×5 crossbar.

C) Comparison with Traditional Packet Transfer

Advantages of FIFO queued Black-bus data-transfer in comparison with the conventional packet transfer methods used in parallel computers and SANs.

• It unburdens procedure to assemble packets, and users are free from complicated packet structure.

• The routing scheme with the local ID decreases both the size of routing tag and routing table.

• The FIFO queue prevents deadlock even if the target router is performing some other function and thus the chances of congestion are reduced.

III. IMPLEMENTATION

The Router is implemented using VHDL coding in Xilinx ISE 13.1. First, the FIFO module and ID table is tested by supplying with the series of 8-bit data to FIFO, where 5-bits MSB is the raw data and the very next 2-bits are the local IDs from the preceding two router’s ID tables and the 1-bit LSB is provided by the intermediate ID table. After having the output from these modules, it is sent to crossbar5×5, whose input is the 8-bit data, where 5-bits MSB are the raw data and remaining 3-bits are the address to target output terminal as shown in Figure 3.

III. SIMULATION RESULT

A. Data inputs
data1:
(data1 is changing each time after an interval of 10ns)
• 80
• 40
• 00
• 18
• 21
• 28
• 30
• 38
Data2:
(data2 is input at 50ns)
• 40

In Figure 4, the first three output cycles are empty because of
the initialization of FIFO module and the immediate next cycle gives the output in which 5-bits MSB are the raw data and the next 3-bits are the local IDs attached to it.

This will serve as the 8-bit input to the next target router in which next local ID will be generated by its ID table and will be joined to incoming 8-bits and thus the input to FIFO becomes of 9-bits.

Evaluation results proves that the maximum number of IDs required in the worst case would be six IDs.

Figure 3: A Simple FIFO queued Black-Bus Router for 2-D Mesh Topology

The data-transfer method called FIFO queued Black-Bus for on-chip interconnection is proposed. In Black-Bus, a local identifier (ID) is attached to each raw data as routing information. Unlike the traditional packet transfer, the header information is transferred on dedicated wires attached to data lines to remove complicated packet generation procedure in a node. Only a small-sized local ID is required to specify routing tags to the destination, and the arising ID conflict is easily solved by intermediate routers. The required local ID are very less compared to the header data in traditional packet transfer and routing table sizes are very small. Evaluation results show that most of the applications demand only at most 3 bit for the local ID. In case of worst case scenario the maximum number of IDs required case would be six IDs. Our target router using FIFO queued Black-Bus data-transfer reduces up to 75% of routing tags compared with global addressing scheme used in the traditional packet networks. As for the future work consideration, the design of network architecture for multi-context reconfigurable processor systems can be achieved.

VI. REFERENCES


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