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Implementation of Power Gating Technique in CMOS Full Adder Cell to Reduce Leakage Power and Ground Bounce Noise for Mobile Application

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***Abstract*— Adder is the paramount circuit for many complex arithmetic operations. The adder cells mainly focus on reduction of power and increasing of speed. For mobile applications, designers work within a limited leakage power specification in order to meet good battery life. The designers apart from leveling of leakage current to ensure correct circuit operation also focuses on minimization of power dissipation. The power reduction must be achieved without comprising performance which makes it hard to reduce leakage current during normal operation of mobile. Power Gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground. The device is turned off during sleep mode to cut-off the leakage path. This technique results in a substantial reduction in leakage at a minimal impact on performance. This paper will focus on reducing sub threshold leakage power consumption and ground bounce noise during the sleep to active mode transition. In the present paper we will propose low leakage 1 bit CMOS full adder circuit in 90nm technology with supply voltage of 1V. We will perform analysis and simulation of various parameters such as standby leakage power, active power, ground bounce noise and propagation delay using Cadence Spectre 90nm standard CMOS technology.**

***Index Terms*— cell, Ground bounce noise, Leakage power, Stacking power gating, Sleep transistor.**

I. INTRODUCTION

Electronic device such as mobile phone is used commonly these days. It's battery life span is of great concern. When mobile phone is operated in standby mode, certain programs of mobile phone are turned off during active or talk mode but this doesn't stop the battery from getting depleted. This is because circuits which are de-activated by turning off certain programs still have leakage currents flowing through them. Even though the magnitude of leakage current is lesser than the normal operating current but leakage current erodes battery life over relatively long standby time whereas the normal operating current erodes battery life over relatively short talk time. Thus this is why low power circuits for mobile applications are of great interest.

Implementation of adder cells to reduce the power consumption and to increase the speed has proved to be a worthy solution towards power reduction. Moreover, realization of adders with different approaches using CMOS technology widens the area of power reduction [1], [2] Performance of the adder cells can be evaluated by measuring the factors such as leakage power, active power, ground bounce noise in context to voltage and transistor scaling.

Reducing the transistor's gate length when no voltage is applied at gate results in more leakage current between source and drain of the transistor which eventually results in the more power consumption [3], [4]. Moreover, apart from sub threshold current, tunneling current also increases with transistor scaling. This implies that leakage power would contribute more than 50% of total power in sub 100nm technology [5]. Thus it becomes extremely essential to lower the static power without compromising the performance.

Many well known techniques are present to lower the leakage power. Power gating is one such technique. This technique uses high threshold voltage sleep transistor which cut-off a circuit block when the block is not switching [9]. Here the sleep transistor is connected between actual ground rail and virtual ground [6], [7]. This insertion of sleep transistor divides the power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off during inactive period. The sizing of sleep transistor is an important design factor. This technique is also known as MTCMOS or Multi-Threshold CMOS and reduces standby or leakage power. Power gating affects design architecture more than clock gating. It increases time delays as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Shutting down the blocks can be achieved either by software or hardware. Power gating uses low-leakage PMOS or NMOS as sleep transistors. This paper concentrates on reduction of leakage power and ground bounce noise which occurs during the transition from sleep

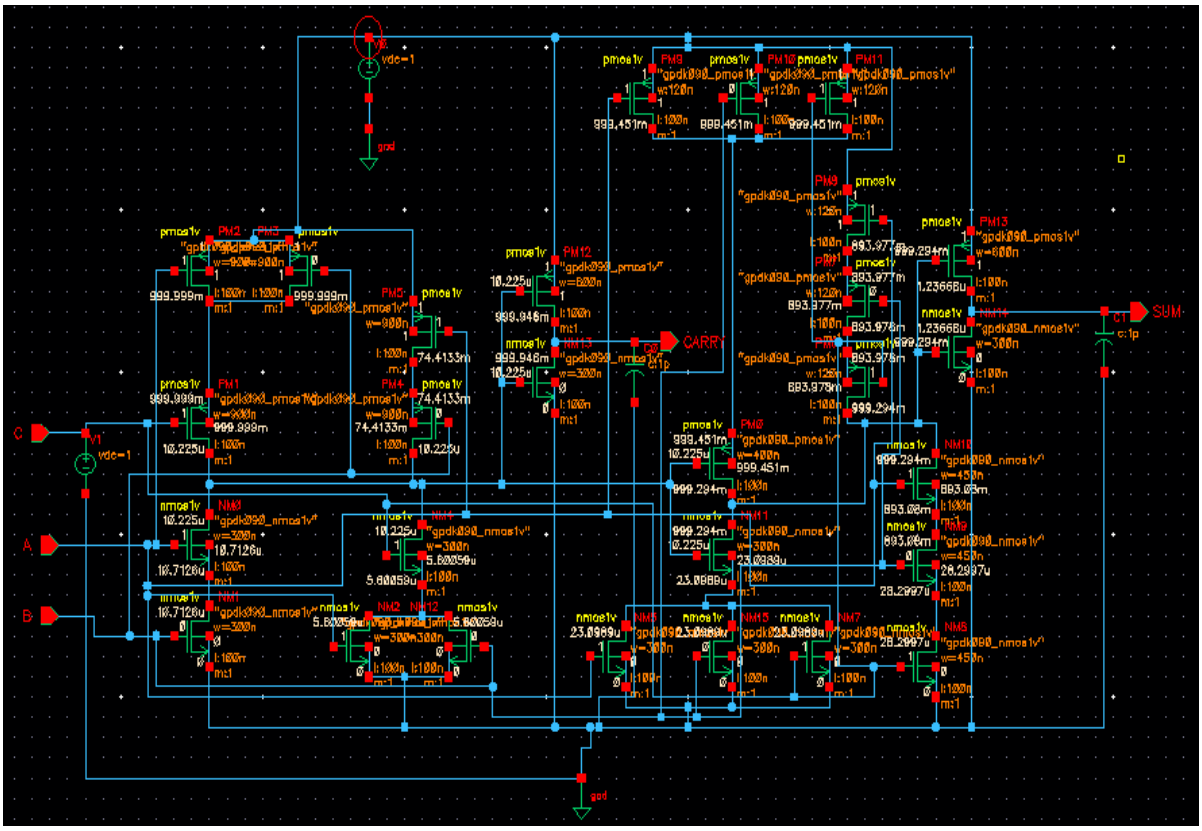

Figure 1: Conventional CMOS full adder.

mode to active mode. In this paper 1-bit full adder has been realized with different approaches for the leakage power reduction in 90nm technology. Conventional CMOS full adder is considered as the base adder and the simulation results of other adders have been compared with this base adder.

II. PROPOSED FULL ADDER CIRCUITS

To minimize the number of transistors required to implement a given logic function can be done by pseudo NMOS and Pass-transistor but they result in more static power dissipation whereas on the other hand, dynamic logic style needs small silicon area for the implementation of complex function but charge leakage and charge refreshing reduces the operating frequency. In general, none of the mentioned styles can beat the CMOS style [2], [7].

The conventional CMOS adder has been shown in Fig. 1. As told earlier, it is the base adder and all simulation results comparison has been done with it. It consists of 28 transistors incorporating PMOS pull up and NMOS pull down networks to produce desired outputs. Here the sizing of transistors plays a vital role. Here, the transistor ratio of PMOS to NMOS has been kept 2 for an inverter and on considering the remaining blocks as equivalent inverters also follows the same ratios. When it is simulated in 90nm process, it provided very poor results in context to leakage power. Thus the adder circuit was modified with proper sizing using power gating technique and has been shown in Fig.2 and Fig.3

In Fig.2 power gating technique has been shown to reduce the leakage power by placing a sleep transistor between actual ground rail and circuit ground (virtual ground). Here low leakage NMOS is used as a sleep transistor. Estimation of the ground bounce noise is done when circuit is connected to the sleep transistor. In Fig.2 stacking power gating technique is shown to achieve the peak of ground bounce noise.

Here the width and length of smallest transistor has been kept 120nm and 100nm respectively for 90nm CMOS technology. The W/L ratio for NMOS is kept as 1.2 whereas for PMOS it's 3.8 which are 3.1 times that of NMOS in Fig.1. The sizing of each block is based on the assumptions that each block is equivalent to inverter and same inverter ratio is maintained for each block. Since sub threshold current is directly proportional to W/L ratio of transistor so the sizing reduces the standby leakage current to a very great extent. Adder design shown in Fig.2 and Fig.3 reduces the ground bounce noise but not up to the mark so in Fig.3 a new modified adder design of what shown in Fig.2 has been given.

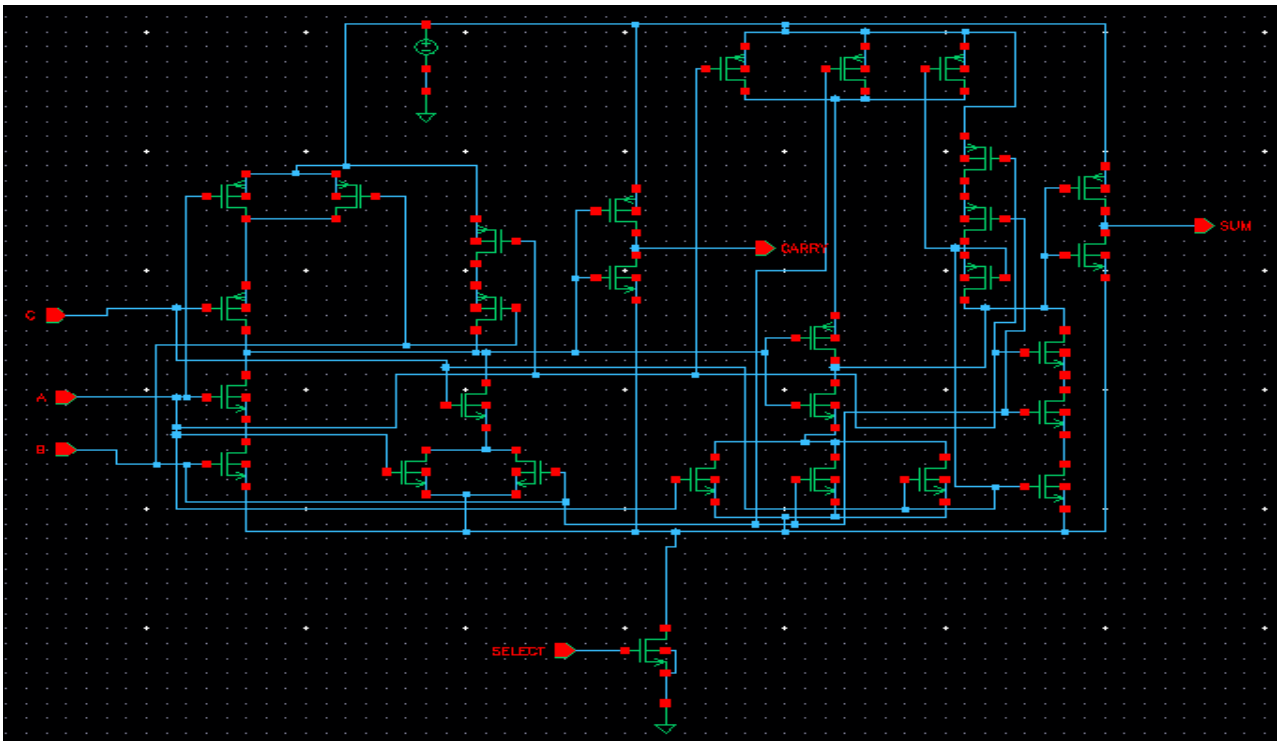

Figure 2: Full adder (Design1) circuit with sleep transistor

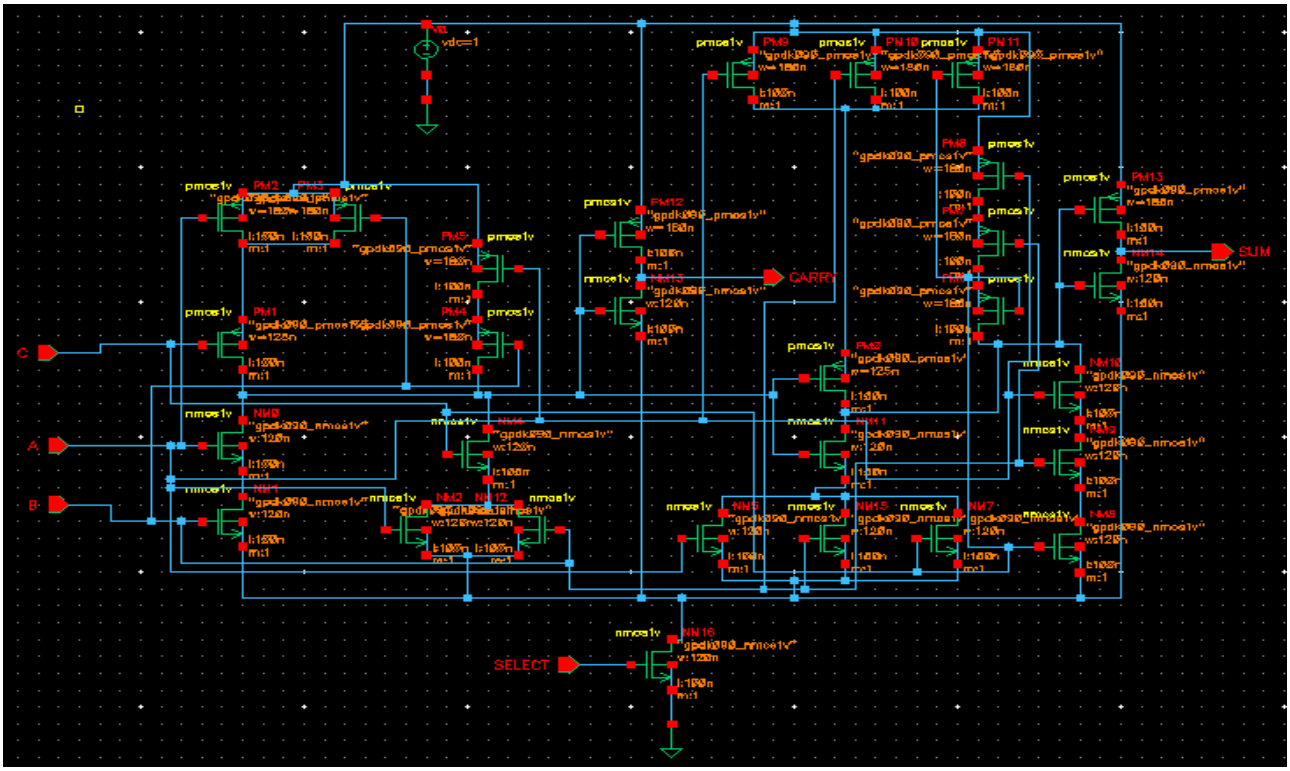

Figure 3: 1 bit full adder (Design2) circuit with sleep transistor

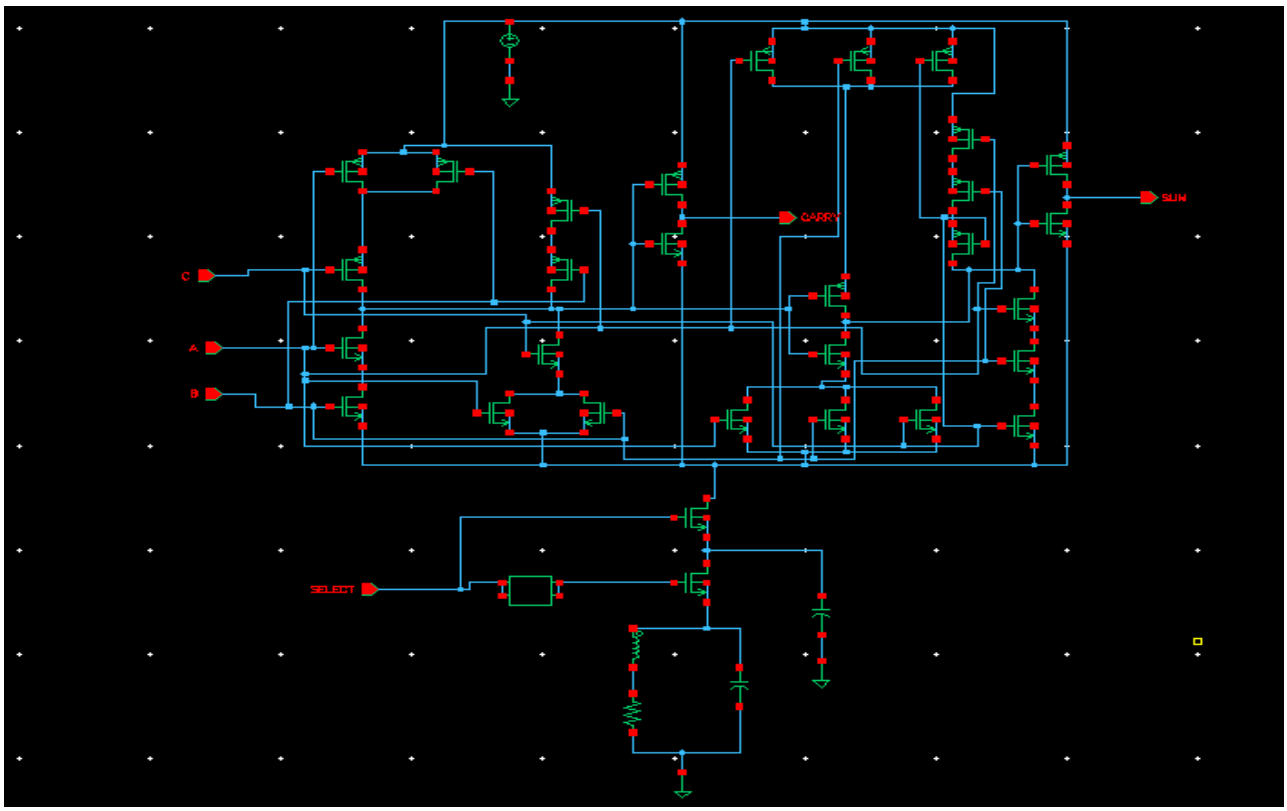

Figure 4: Schematic view of Design 2 with stacking power gating technique (proposed) Modified Design 2

This adder uses the stacking power gating technique where the magnitude of peak current and glitches in power rails is done by stacking sleep transistors [9].

In this technique, both MSL1 and MSL2 sleep transistors are turned off. Here, SELECT input is applied in such a manner that ground bounce noise is lowest and this is achieved by keeping the value of ΔT which gives the summation of ground bounce noises of these two transistors lowest. If ΔT is half the oscillation period of the ground bounce noise then the positive peak of the ground bounce noise lay over the negative peak thereby bringing ground bounce noise closer to zero. In this technique we used the stacking sleep transistor to minimize the peak current and voltage glitches in power rails i.e ground bounce.

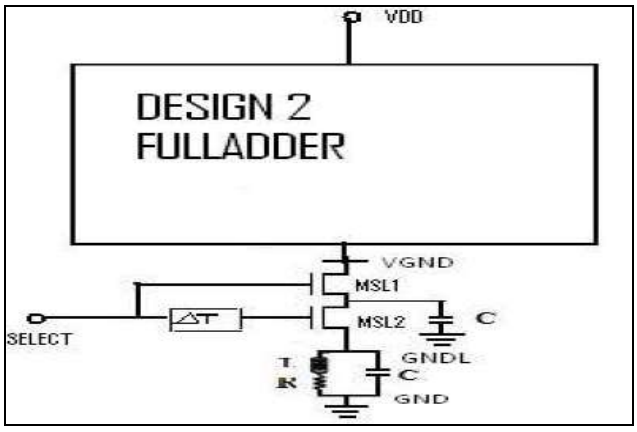

Figure 5: Design 2 with stacking power gating technique (proposed) Modified Design 2

II. PERFORMANCE ANALYSIS AND SIMULATION RESULTS

We have performed simulations using cadence-spectre simulator and the technology used for simulation is 90nm CMOS technology.

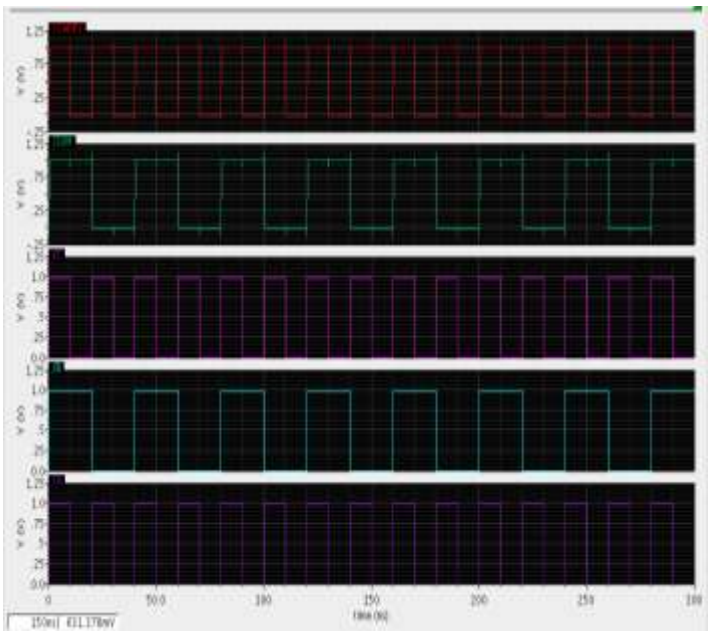

Figure 6: Functional simulation of Conventional CMOS 1-bit Full adder cell

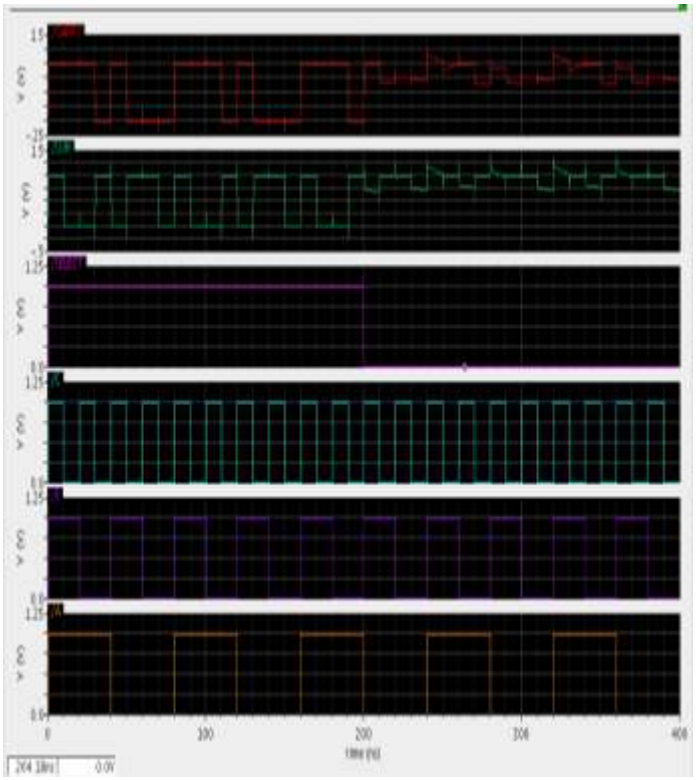

Figure 7: Functional simulation of Full adder (Design1) circuit with sleep transistor

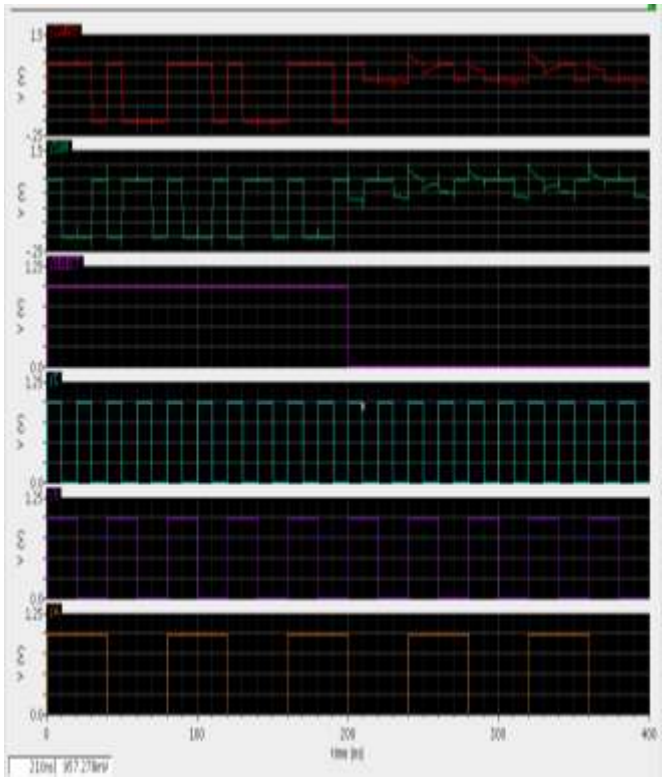

Figure 9: Functional simulation of Design 2 with stacking power gating technique.

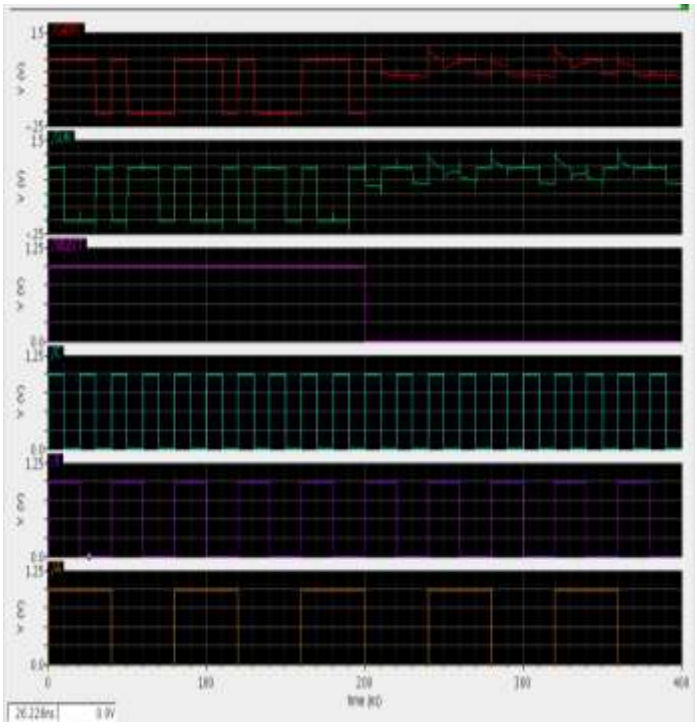

Figure 8: Functional simulation of 1-bit Full adder (Design2) circuit with sleep transistor

A. Active Power:

The dissipation of power which occurs during the active mode of the circuit is active power. This active power consists of dynamic power as well as the static power so it is being named as an active power. It is measured by giving input vectors to the circuit and then calculating the average power dissipation and then comparing the result with the base adder i.e. conventional 1-bit CMOS full adder.

TABLE 1.

ACTIVE POWER DISSIPATION OF 1-BIT FULL ADDER CELL

Circuit	Conventional CMOS	Design 1	Design 2	Design2 with Stacking Power gating
Active Power (µw)	7.56	5.14	2.57	3.17

B. Standby leakage power:

The dissipation of power which occurs when the circuit is in standby mode. Sleep transistor is connected to the NMOS pull down network of 1 bit full adder circuit and it is turned off by applying 0V. For simplicity, size of a sleep transistor equals the size of largest transistor in the network (pull up or pull-down) connected to the sleep transistor. It is measured by applying input vector combinations to the circuit.

TABLE 2.

Standby Leakage Power Comparisons

Input Vector	Standby leakage Power(nWatt)			
	Conventional CMOS Adder Cell	Design 1	Design 2	Design 2 with Stacking power gatting
0 0 0	64.72	13.21	8.64	7.69
0 0 1	69.62	14.91	10.47	6.25
0 1 0	87.45	17.24	11.78	5.28
0 1 1	86.32	19.41	14.27	6.69
1 0 0	63.24	18.71	13.71	5.31
1 0 1	60.21	15.62	12.54	7.18
1 1 0	66.55	14.67	11.11	6.92
1 1 1	61.28	10.14	8.49	4.67

C. Delay:

In electronics and digital circuits the propagation delay, or gate delay, is the length of time which starts when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is stable and valid. Often this refers to the time required for the output to reach from 10% to 90% of its final output level when the input changes. Speed of an integrated circuit is inversely proportional to the propagation delay and it is an important performance parameter. Table 3 shows the comparison of delay among the three different circuits.

D. Grounds bounce noise reduction:

Ground Bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die. Essentially it is caused by a current surge passing through the lead inductance of the package. The effect is most pronounced when all outputs switch simultaneously. In saturation region an instantaneous charge current passes through the sleep transistor, during power mode transition. There are some methods such as power gating to address the problem of ground bounce in low-voltage CMOS circuits. All the three design we are reduced the ground bounce noise using the Stacking power gating logic circuits.

TABLE 3.

PROPOGATION DELAY OF 1-BIT FULL ADDER CELL

Input Vector			Conventional CMOS Adder (ps)		Design 1(ps)		Design 2(ps)		Modified Design2(ps)	
A	B	C	SUM	CARRY	SUM	CARRY	SUM	CARRY	SUM	CARRY
0	p	0	50.65	d	38.55	d	42.67	d	70.26	d
0	p	1	82.36	39.58	94.52	86.32	88.54	47.21	94.24	57.21
1	p	0	77.44	48.222	102.22	62.15	87.25	54.55	109.62	64.75
1	p	1	54.92	48.222	64.25	62.15	62.11	54.55	64.35	64.75
p	0	0	65.25	d	46.33	d	49.57	d	71.57	d
p	0	1	92.36	49.58	94.64	76.32	81.44	49.17	81.72	61.81
p	1	0	88.44	54.12	101.11	74.75	77.15	81.61	91.58	57.98
p	1	1	52.12	54.12	69.25	74.75	72.21	81.61	94.21	57.98
0	0	p	39.25	d	81.22	d	71.8	d	61.24	d
0	1	p	85.88	67.31	98.54	71.24	91.27	64.25	90.37	60.25
1	0	p	88.44	64.27	49.67	84.24	67.25	88.01	105.27	57.64
1	1	p	52.12	64.27	72.55	84.24	65.25	88.01	81.33	57.64

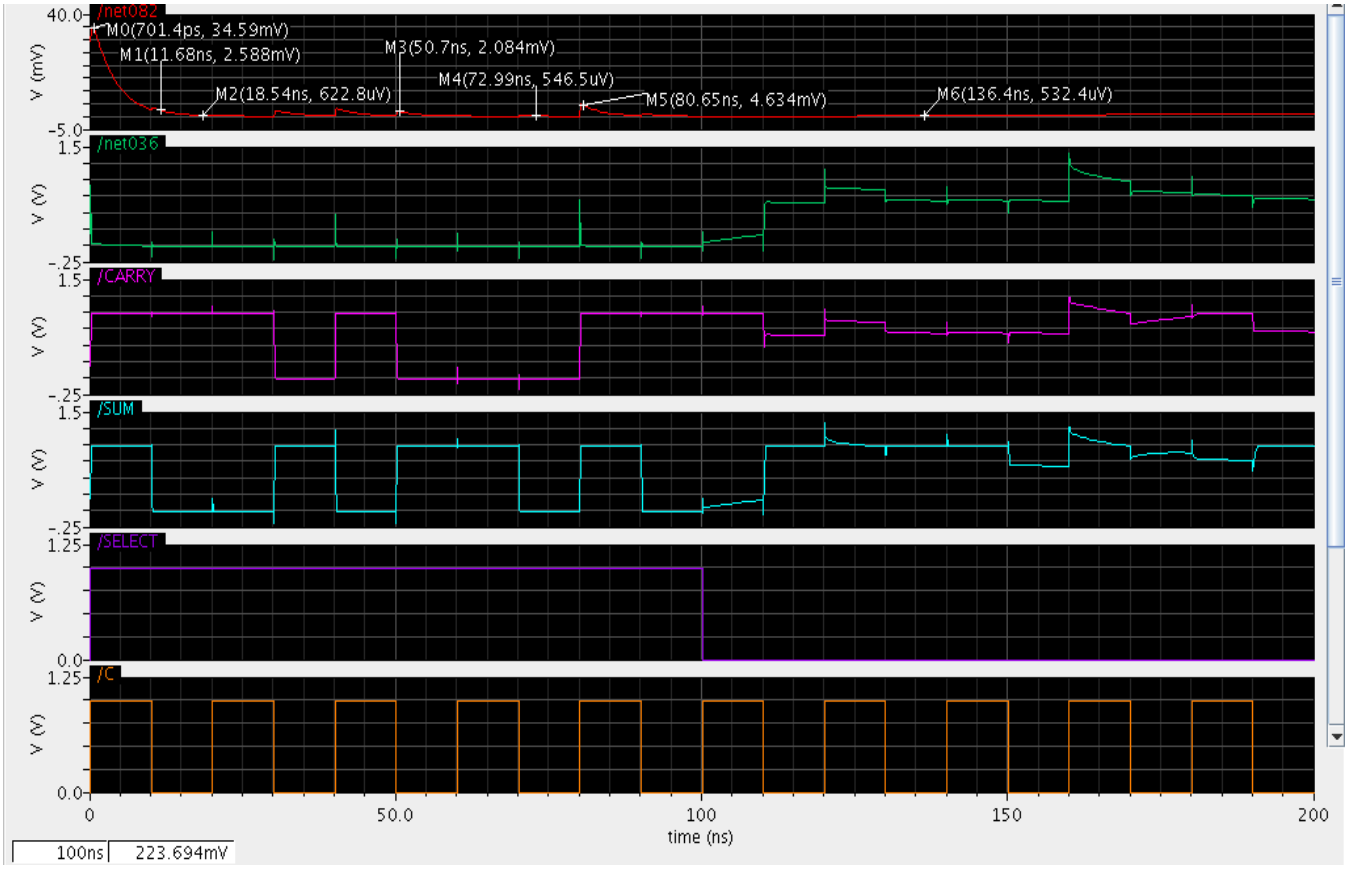

Figure 10: Showing ground bounce noise in design2 with stacking power gating technique with delay

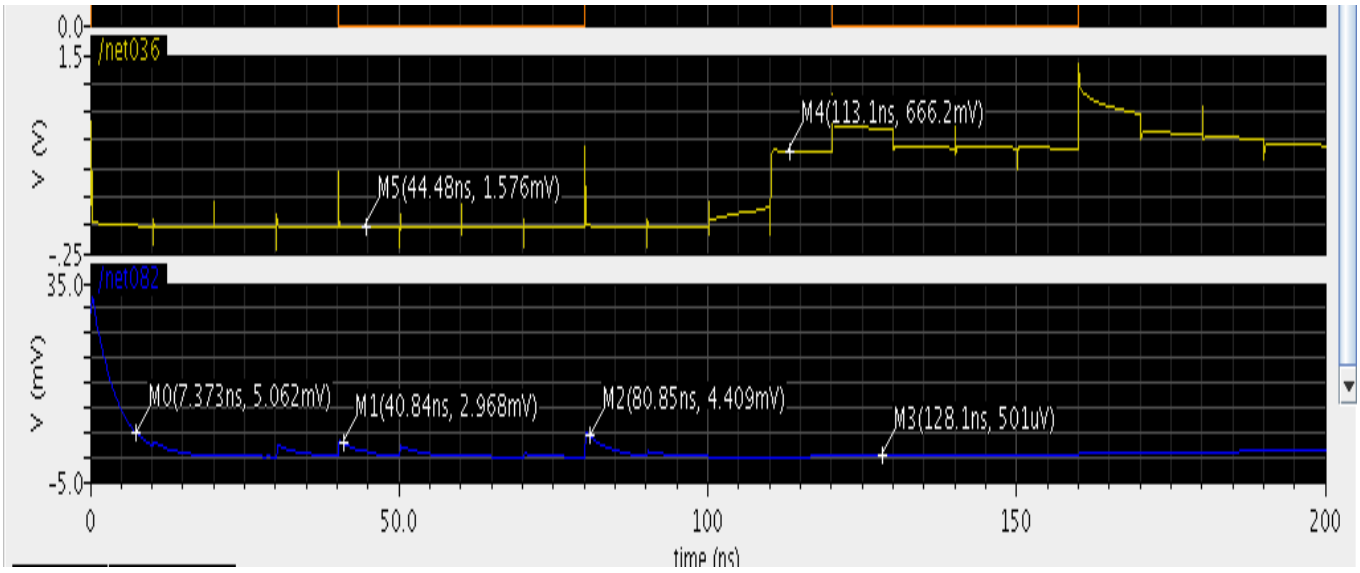

Figure 11: Showing ground bounce noise in design2 with stacking power gating technique without delay

III. CONCLUSION

In this paper 1-bit full adder cell with power gating technique is implemented where a sleep transistor is added between actual ground rail and circuit ground. The device is turned off during sleep mode to cut-off the leakage path. For optimal performance, stacking power gating technique has been implemented where SELECT input to stacked sleep transistor with delta T delay further minimizes the leakage power and ground bounce noise. The comparison of active power, standby leakage power is done and it's observed that power is

greatly reduced as we move from conventional CMOS full adder cell to Modified Design2. The leakage power is reduced by 79 % (Design1), 85% (Design2) and 92% (Design2 with stacking power gating) in comparison to the conventional 1 bit full adder cell. Active power is reduced by 35.47% (Design1), 66.31% (Design2) and 59.48% (Design2 with stacking power gating) in comparison to conventional 1 bit full adder cell.
The ground bounce noise is compared for Modified Design2 without delay and with delay and it is reduced in the latter case. The implemented 1-bit full adders are designed using 90nm technology and operated supply voltage of 1V.

REFERENCES

[1] Rabaey J. M., A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits, A Design Perspective*, 2nd Prentice Hall, Englewood Cliffs, NJ, 2002
[2] Pren R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1079–1090, July 1997.
[3] S.G.Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies. New York: Springer-verlag, 2006.
[4] K.Bernstein et al., "Design and CAD challenges in sub-90nm CMOS technologies," *in Proc. int. conf. comput. Aided Des*.,2003, pp.129-136. A. Karnik, "Performance of TCP congestion control with rate feedback: TCP/ABR and rate adaptive TCP/IP," M. Eng. thesis, Indian Institute of Science, Bangalore, India, Jan. 1999.
[5] S.Mutoh et al., "1-v power supply high-speed digital circuit technology with multithreshold-voltage CMOS."*JSSC*, vol.SC- 30, pp.847-854, Aug.1995.
[6] K. Kawasaki et al., "A sub-us wake-up time power gating technique with bypass power line for rush current support," IEEE J. Solid-State Circuits, vol.44, no. 4, pp.146–147, Apr. 2009.
[7] M. V. D. L. Varaprasad, Rohit Bapna, Manisha Pattanaik, "Performance Analysis of Low leakage 1-bit Nano-CMOS Based Full Adder Cells for Mobile Applications, " *Proceedings of*
International Conference on VLSI Design & Communication Systems, pp.233-238, January 2010.
[8] R.Bhanuprakash, Manisha Pattanaik and S.S.Rajput "Reduction of Leakage Current and Ground Bounce Noise Using High Performance Stacking Power Gating Logic Circuits, "proceedings
of IEEE TENCON Singapur,pp 1-6,2009.
[9] Kaijian Shi, David Howard "Sleep Transistor Design and Implementation – Simple Concepts Yet Challenges To Be Optimum" VLSI Design, Automation and Test, 2006 International Symposium.

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