Analysis and optimization of Boundary-scan Test Circuit Designed for FPGA

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Abstract—Boundary scan is a widely adopted DFT (Design for Test). According to the characteristic of FPGA application, Boundary-scan has rapidly become the technology of choice for building reliable high technology electronic products with a high degree of testability. Due to the low-cost and IC level access capabilities of boundary-scan, its use has expanded beyond traditional board test applications into product design and service in this paper a test procedure for analysis of linear-feedback shift register and feedback shift register for FPGA application is proposed. The proposed method show significant power savings.

Keywords— Built in self Test, linear-feedback shift register, feedback shift register, Power.

INTRODUCTION

Boundary-scan, as defined by the IEEE Std.-1149.1 standard, is an integrated method for testing interconnects on printed circuit boards (PCBs) that are implemented at the integrated circuit (IC) level. The inability to test highly complex and dense printed circuit boards using traditional in-circuit testers and bed of nail fixtures was already evident in the mid eighties. Due to physical space constraints and loss of physical access to fine pitch components and BGA devices, fixturing cost increased dramatically while fixture reliability decreased at the same time.

TESTING THE INTERNAL CIRCUITS OF THE SYSTEM:

The concept of scan design can also be used in testing the connections between chips on a PCB, leading to a technique called boundary scan. Scan-chain flip-flops are included on the external pins of each chip. To test the PCB, a test vector is shifted into the scan chain. Once the loading is completed, the vector is driven onto the external outputs of the chips. The scan-chain flip-flops then sample the external inputs, and the sampled values are shifted out to the test equipment.

Further it is easy to verify that all of the connections between the chips, including the chip bonding wires, package pins and PCB trace, are intact. To detect different kinds of faults, various test vectors are used. For example broken connections, shorts to power or ground planes, and bridges between connections.

SCAN DESIGN AND BOUNDARY SCAN:

Modifying the registers a chain like structure of long shift registers are formed called as scan chain. Test vectors can be shifted into the registers in the chain, under control of the test mode input, thus making them controllable. To make them
observable stored values can be shifted out of registers.

![Connection of modified registers in a scan chain](image)

Fig 1. Connection of modified registers in a scan chain.

Above structure allows us to control and observe the combinational blocks between registers. We can test each combinational block separately. This process consists of shifting test values into the register chain until the test vector for each block reaches the input registers for that block.

Further the system is allowed to run in its normal operational mode for single clock cycle, clocking the output of each block into the block’s output registers. Test vectors are applied to the external inputs of the system and the external outputs of the system are observed, in order to test any combinational input and output circuits. Finally, the result values are shifted out through the register chain. The test equipment controlling the process compares the output values with the expected results to detect any faults. This sequence is repeated until a fault is detected, or until the entire test vectors have been applied to all of the combinational blocks. Observability is provided, this makes achieving high fault coverage feasible, especially for large circuits. The main disadvantage of scan design is the overhead, both in circuit area and delay.

**BUILT-IN SELF TEST (BIST):**

We seen developing of test vectors during design of a system and applying the vectors to various components to test them. The components cannot be tested at full operating speed, since test vectors for each cycle of system operation must be shifted in over many clock cycles. These problems are avoided using built in self test techniques. Where the test circuits are added that generate test patterns and output responses are analyzed. Since BIST is embedded in the system it can generate the test vectors at full system speed. Thus it reduces the time taken for test. BIST hardware can also generate multi-cycle test sequences. The BIST hardware remains available during the operational lifetime of the system, and when the system is in the field it can be used for testing purpose. But the disadvantage is that it requires larger area. When designing a BIST implementation there are two main aspects to be considered: how to generate the test patterns and the other is how to analyze the output response to determine whether it is correct. Test patterns can be generated by one of the most common method called pseudorandom test pattern generator.

A seed is the starting point from where the pseudorandom sequences can be repeated. There is a simple hardware structure called a linear-feedback shift register (LFSR) from which the Pseudo-random sequences can be generated. By presetting the flip-flops, the sequence is initiated generating the test value 1111 as the seed.

![Seed test value](image)

Fig 2. generated seed test value

On successive clock cycles, the LFSR generates values in the sequence. Except 0000 the sequence contains all possible 4-bit values. We can modify the LFSR to form a complete feedback shift register (CFSR), and it is used in the applications where it is desirable to include the value 0000 also. This generates all possible values. Thus similar circuits can be designed to generate pseudo-random test vectors of other lengths.

![Generating pseudorandom test vectors](image)

Fig 3. 4-bit generating pseudorandom test vectors

**RESULTS:**
CONCLUSION

The boundary-scan circuit presented in this paper extends the traditional test function. The comparative study of linear-feedback shift register (LFSR) and complete feedback shift register (CFSR) is given. Further optimization in power is calculated.

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