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Study of FPGA based PID controllers

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Abstract— **This paper deals with the performance analysis and implementation of robust PID (Proportional-Integral-Derivative) Controller on FPGA platform. The software implementation has been done using Xilinx ISE 9.1i as a tool. The VHDL algorithm for the proposed implementation has been presented in this paper. This research minimizes the Power Consumption and Delay as compared to conventional PID controllers. Performance analysis of robust PID controller using Xilinx ISE Design9.1i Suite software shows the effectiveness of the proposed method.**

***Index Terms*— ASIC, DSP, FPGA, PID, PWM, SOC, VHDL.**

I. INTRODUCTION

Since the Years , the law of Moore predicts that the complexity in terms of built in circuit transistors doubles every two years, remain verified. The programmable FPGA circuits (Field Programmable Gate Array) could not escape to this law. Since the first FPGA, developed like an evolution, these circuits didn't stop winning in complexity and integrated henceforth until one billion of transistors for the most recent generations. A growth resulted in power calculation due to increase in integration level. The FPGAs have been used then to make the fast samples of ASICs (Application Specific Integrated Circuits)[12] and find since some years their place in many domains of applications.

However, the orders of the industrial processes require more elements of powerful calculations. Thus, the PID controllers represent the majority of the controllers used in the industrial control systems. Due to this fact, it will be necessary to digitalize the PID algorithm [4]. The modern digital control systems require more and more strong and fastest calculation components. This type of elements becomes yet indispensable with the utilization of some new control algorithms like the fuzzy control, the adaptive control, the sliding mode control…

Although the PID controllers are the oldest they represent the most used controllers in the industrial control systems. But robust PID controllers have built a more competition to the conventional controllers. Digital controllers have been widely used over the past five decades due to their simplicity, robustness, effectiveness, and applicability for a broad class of systems [4].

Implementation of digital controllers has gone through several stages of evolution, from the early mechanical and pneumatic designs to the microprocessor based systems but these systems have the drawback of demanding control requirements of modern power conditioning systems will overload most of the microprocessors and the computing speed limits the use of microprocessor in complex algorithms. Microprocessors, Microcontrollers and Digital Signal Processors (DSPs) can no longer keep pace with the new generation of applications that requires more flexible and higher performance without increasing cost and resources [9]. In spite of the numerous control designs, it is estimated that nowadays digital controllers are still employed in more than 95% of industrial processes. An important feature of these controllers is that they do not require a precise analytical model of the system that is being controlled. For this reason, digital controllers have been widely used in robotics, automation, process control, manufacturing, transportation, and interestingly in real time multitasking applications.[2]. Furthermore the tasks are executed sequentially which takes longer processing time to accomplish the same task in Microcontrollers and DSPs. We have used Digital PID controller in our work. PID controllers have evolved from analog controllers to digital controllers.

The analog controllers are mechanical one and digital controller's ranges from microprocessor to SOC (system on chip) platform [2]. The digital domain of control mechanism is less expensive and also it is easy to implement the advanced control algorithm than the analog. Other advantages of digital domain of control strategies include flexibility in changing parameter, lighter weight and greater insensitivity to noisy external signals. As the growing complexity of motor and motion control applications is increases, it becomes apparent that a reconfigurable hardware such as FPGA offers significant advantage over the microcontroller solutions in the areas of performance, flexibility and inventory control advantages such as high speed, complex functionality, and low power consumption. These are attractive features from the embedded system design point of view [3].

Recently, Field Programmable Gate Arrays (FPGA) is becoming alternative solution for the realization of digital control systems. The FPGA based controllers offer advantages such as high speed computation, complex functionality, real time processing capabilities and low

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power consumption [1]. Hardware Description Languages (HDLs) are used to describe hardware for the purpose of Simulation, Modeling, Testing, Design, and Documentation of digital systems. The most popular HDLs are VHDL [(Very High Speed Integrated Circuit) Hardware Description Language], and Verilog. Many of the Electronic Design Automation (EDA) vendors are standardizing on VHDL as input and output from their tools. These tools include simulation tools, synthesis tools, layout tools and testing tools[11].In the past two years, Spartan II and III FPGA families from Xilinx have been successfully utilized in a variety of applications, which include inverters [5][6], communications [7][8], embedded processors [1], and image processing [6].

The application range of FPGA based designs increases every day. This is mainly due to the flexibility and capability to perform parallel tasks. The industry is adopting massively the core-based design methodology for system integration using FPGAs, which leads to the appearance of the System-on-Programmable-Chip (SoPC) platforms [2]. This paper presents a PID core suitable to be introduced in such a system. The simulation of the VHDL code can be performed around the Xilinx design suite [4]. The "System Generator" is a collection of Simulink block sets that permit interaction between hardware and modeled systems. In this paper we consider discrete time PID controller and is implemented in a dedicated FPGA with feedback sensor. The approach can be extended to design other embedded controllers using FPGA. The complete system is implemented by dividing system functions into reconfigurable modules. In general, embedded control designers need to go through three phases in the design of digital control systems: 1) software modeling/simulation in an environment such as Matlab/Simulink; 2) hardware implementation; and 3) co-simulation of the whole system including both hardware and software.

Conventional PID controllers suffered from problem of power consumption and delay due to PWM converters but this paper presents robust PID controller with a sensor which will eliminate the above disadvantages.

II. PID CONTROLLER

A. *Basics*

PID control, shown in fig. 1, is one of the earlier control strategies. Its early implementation was in pneumatic devices, followed by vacuum and solid state analog electronics, before arriving at today's digital implementation via microprocessors or FPGA. The PID algorithm consists of three modes proportional, integral and derivative mode.

It has a simple control structure which was understood by plant operators which they found relatively easy to tune. Since many control systems using PID control have proved its satisfactory performance, it still has a wide range of applications in industrial control [8] and it has been an active research topic for many years.

The general transfer function of the PID controller looks like the following:

$$u = k_p e + ki \int e\,dt + kd\frac{de}{dt} \qquad (1)$$

- Kp = Proportional gain
- Ki = Integral gain
- Kd = Derivative gain

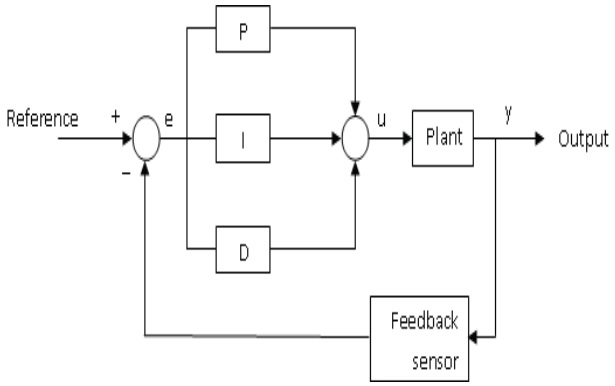

Fig. 1. Closed loop robust PID Controller

The variable (e) represents the tracking error .This error signal is sent to the PID controller, and the controller computes both the derivative and the integral of the error signal. This signal (u) is sent to the plant, and the new output (y) will be obtained. This new output (y) will be sent back to the sensor again to find the new error signal (e). The controller takes this new error signal and computes its derivative and integral again, this process goes on and on until the error signal (e) equals zero [9].

Before implementing PID controller on FPGA, proper gain values must be selected by observing their step responses. After that the selected values are used in VHDL code for PID Controller implementation. The PID Controller has been implemented on Xilinx FPGA using the steps given .

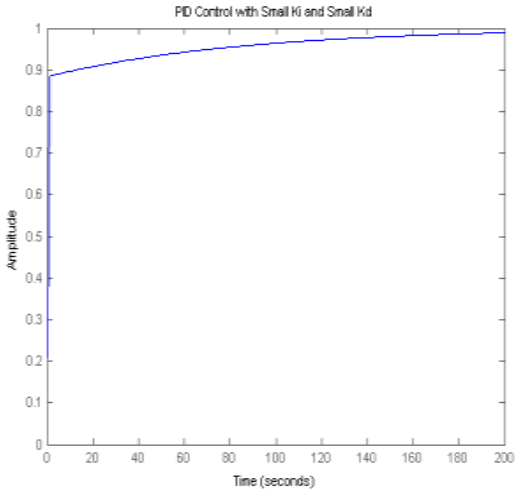

Fig. 2. Step response of PID Controller with small Ki and small Kd.

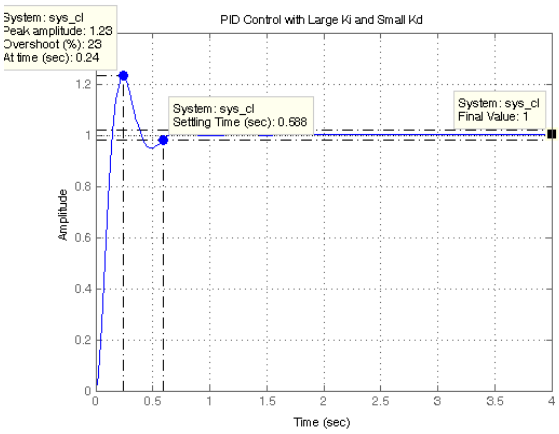

Fig. 3. Step response of PID Controller with large Ki and small Kd.

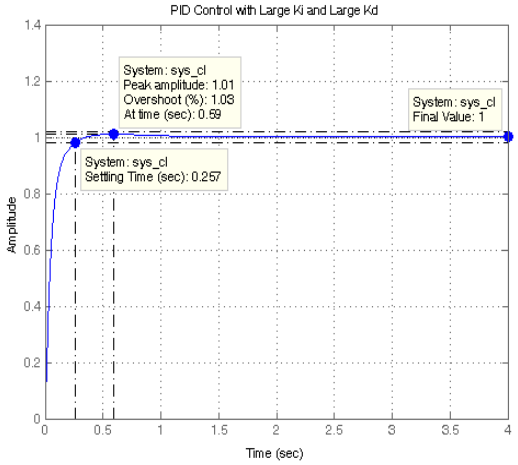

Fig. 4 . Step response of PID controller wth large Ki and large Kd.

After seeing all these responses, the response given in fig.4 is the best one to meet the desired specifications.

B. PID CONTROLLER AND PWM MODULATOR

The PID controller follows the classical structure. It contains two saturation Blocks, one for the integral part and the other for the overall sum (see figure 5). The controller has a pipeline structure of three stages, in other words, it needs three clock cycles to perform all the operations. In order to improve the area and speed, hardware multipliers have been used [12]. These multipliers are included in the Spartan 3 family of Xilinx and subsequent FPGAs. These multipliers have 15 bit input data bus and are signed. This leads to optimum implementation when the fixed point implementation uses less than 15 bit in two's complement.
The PWM modulator admits a two's complement input and transforms it into a PWM signal. The module has two outputs, one the modulated PWM and the other one the sign of the modulation (see figure 6).

The PWM module also generates the enable signal for the control loop. This signal makes the PID controller begin a new cycle and calculate a new PWM input value. The PWM

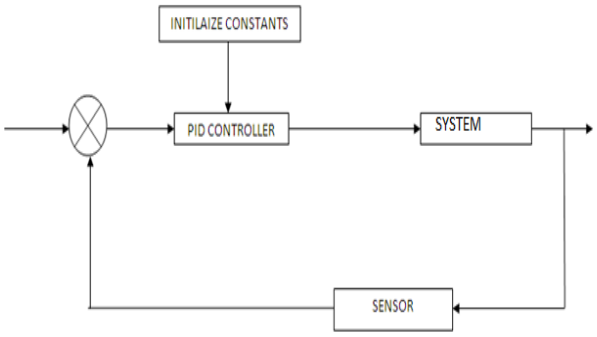

Fig. 5. Block diagram of robust PID controller

has a saturating block; this saturation value is symmetrical for positive and negative values and can be configured.

The ratio between PWM cycles and PID cycles and the number of bits of the PWM input can also be configured. The PWM block also has an on/off input, allowing the disconnection of the modulator and the brake of the motor.

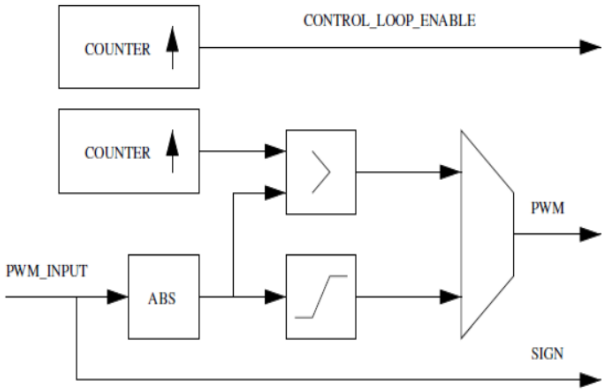

Fig.6. Block diagram of PWM modulator

III. ADVANTAGES OF FPGA BASED DESIGN

Field Programmable Gate Array (FPGA) offers the most preferred way of designing PWM Generator for Power Converter Applications. They are basically interconnection between different logic blocks.

When design is implemented on FPGA they are designed in such a way that they can be easily modified if any need arise in future. We have to just change the interconnection between these logic blocks. This feature of Reprogramming capability of FPGA makes it suitable to make your design using FPGA [1].

Also using FPGA we can implement design within a short time. Thus FPGA is the best way of designing digital PWM Generators [6]. Also, implementations of FPGA-based digital control schemes prove less costly, high speed, complex functionality, and low power consumption and hence they are economically suitable for small designs [1].

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IV. DESIGN PROCEDURE ON FPGA

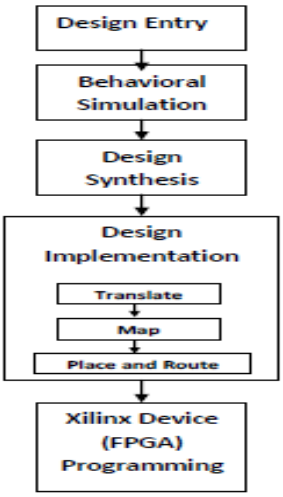

Fig. 7. FPGA Design Flow

The Field Programmable Gate Array (FPGA) ,as the name suggest, is a array of logic cells (or modules) and interconnects, which can be reprogrammed depending upon the requirement of the user. We can design it and make changes in it whenever required. It provides instant manufacturing turnaround and negligible prototype costs which makes it suitable for embedded system design.

V. PROPOSED METHODOLOGY

We are proposing a sensor by eliminating PWM Modulator and A/D Convertor, which can reduce the power consumption and overall Delay for system. Figure shown below shows the comparison between General PID Controller and proposed PID Controller.

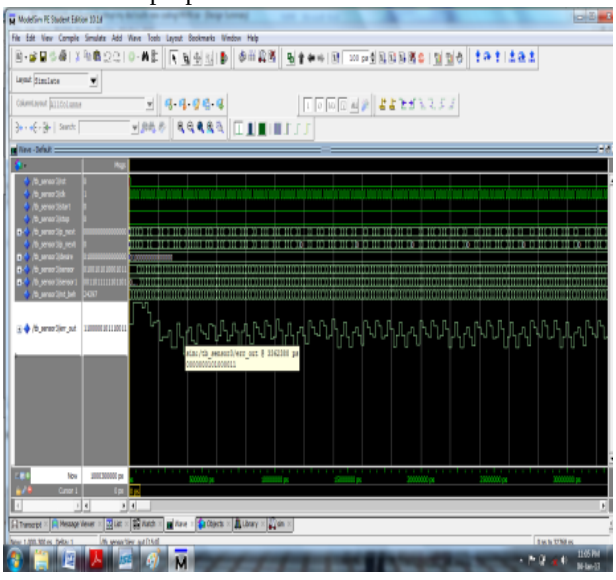

Fig. 8. Simulation Results

VI. CONCLUSION

PID controller has improved response after tuned properly. Various tuning methods can be proposed and used for the tuning of PID controller. The optimum values of PID constants are desirable for smooth control action.

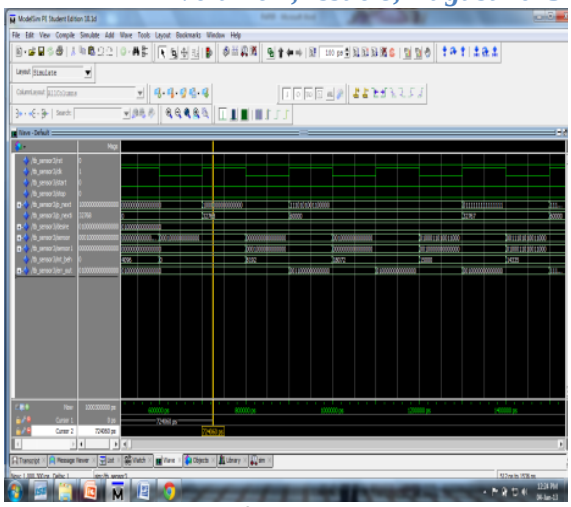

Fig. 9. Error output

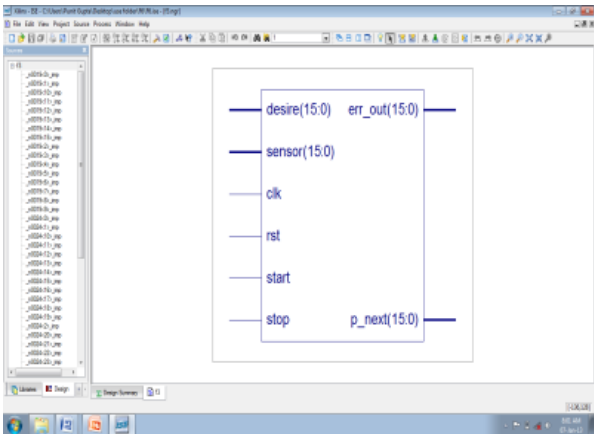

Fig. 11. RTL View of PID controller

Many researchers have proposed various rules of tuning of PID controller. The simulation results are very much satisfactory for the 3rd order system with allowable margin. Steady state error is observed in the response of developed systems that can improve using implementation of suitable noise filter in the feedback.

A digital PID controller implemented in FPGA technology is a configurable controller in terms of latency, resolution, and parallelism. The speed or execution or latency of the controller can be precisely controlled with the amount of reuse of arithmetic elements such as the speed of execution of FPGA based PID controller can be less then 100 ns if desired for high throughput requirements. Implementing PID controllers on FPGAs features speed, accuracy, power, compactness, and cost improvement over other digital implementation techniques. The most promising issue regarding with the FPGAs is the fast time to market operation, speed, accuracy and improvement in cost over other digital implementation techniques.

In this paper, a novel robust PID based controller was presented, for FPGA implementation. Hence the efficient dynamic system implementation is done. We can achieve high speed as well as better performance and low cost as compared to analog counterpart. Delay as well as power consumption is reduced.

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