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An Extremely Low Power Consumption Operational Amplifier with High Phase Margin and Gain in 130 nm Technology

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***Abstract*- This work represents the design of a modified two stage Operational Amplifier in 130nm CMOS technology. The main objective of the design is to make a trade-off between low power consumption and high phase margin with high gain. The Operational Amplifier is more versatile and important building blocks in analog circuit design[1] .Simulation is done in Orcad with 1.2v power supply, simulation results shows that the designed Op Amp consumes very low power 363 µw with phase margin of 81^0.**

Index Terms* - *CMOS, Low Power, Operational Amplifier, Phase Margin.

I.INTRODUCTION

Operational Amplifier (OpAmp) are integral part of many analog and mixed signal systems. OpAmps with vastly different levels of complexity are used to realized function ranging from dc bias generation to high speed amplification or filtering[2].Operational amplifiers are amplifiers that have sufficiently high forward gain[1]. The design of a high performance OpAmp has become a challenge with the continuous reduction in the device length. For most of the analog systems and mixed signal ICs, OpAmps are used for the comparator and switched capacitor based sample and hold circuits. The motivation for the design of OpAmp includes a wide area of application ranging from home appliances to biomedical, communication and signal processing purposes. Op Amp performance parameters are interdependent on each other. Designers always make a tradeoff between performance parameters while designing an OpAmp. The tradeoff is done based on the application area. Speed and DC gain are the deciding factors for any OpAmp to be used for data converters [3], [6]. High phase margin, low bandwidth, high gain and low power OpAmp is required for biomedical application [7]. There are various basic topologies available which can be chosen as the starting point of the design as per specific application area. Fig.1 shows comparison of various topologies based on OPAMP performance parameters.

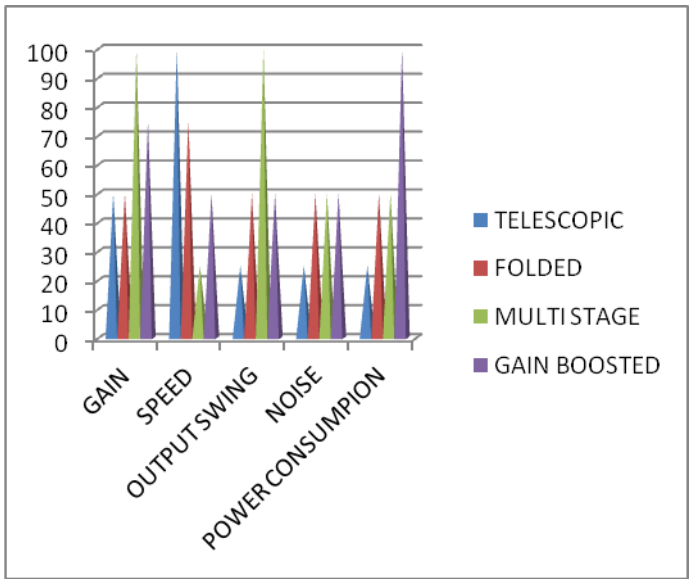
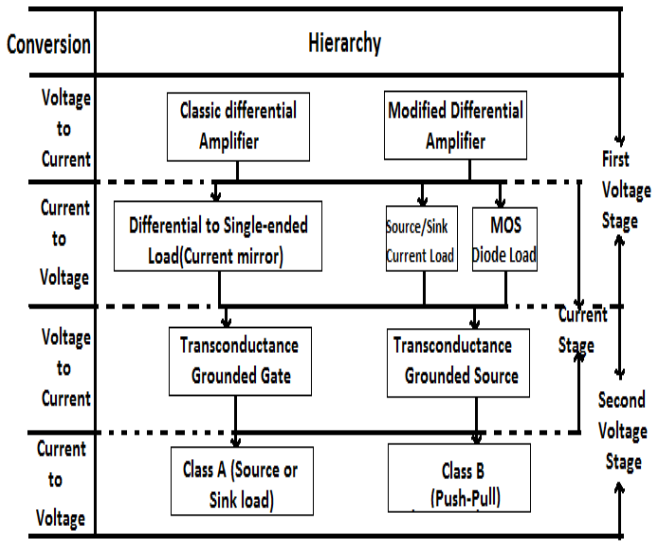


Fig.1 Performance comparison for different topologies of OpAmp

In this paper the OpAmp is designed to achieve high phase margin and minimum power consumption and maximum gain. In order to understand the design of CMOS OpAmp it is worthwhile to examine their characterization.Table-1 gives a hierarchy of CMOS OpAmp. As we know that amplifiers consist of a cascade of voltage to current or current to voltage converting stages. A voltage to current stage is called a transconductance stage and a current to voltage stage is called the load stage. This two-stage OpAmp is so widely used that we will call it classical two stage OpAmp.This classical opamp is shown in [1]Fig.2

Table-1 Classification Of CMOS Operational Amplifier



That is applicable to nearly all CMOS OpAmps.Based on the characterization in Table-1. There is a major two stage OpAmp architecture. It consists of a cascade of V-I and I-V stages as shown in Fig.2

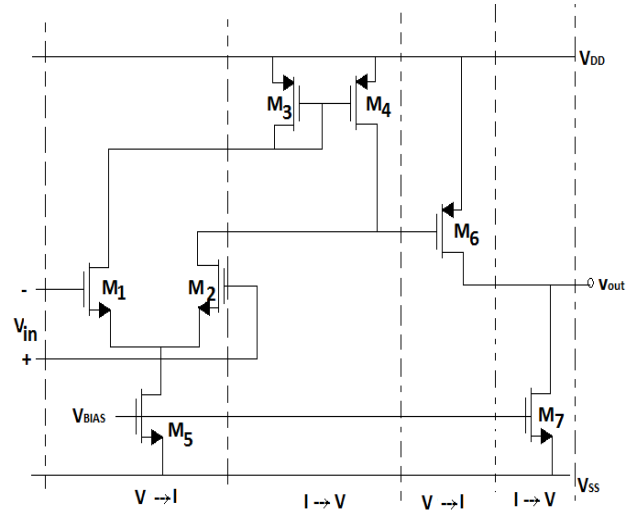


Fig.2 Classical Two Stage CMOS Op-Amp broken into voltage to current and current to voltage stages

OPAMP topology with two gain stages is chosen in which the first stage is converting the differential voltage to current by using the differential amplifier. This differential current is in conjunction with current mirror load recovers the voltage. The second stage is a common source amplifier acting as high output swing stage. The conventional two stage OPAMP circuit is given in Fig.3.

The remaining paper is organized as follows. Section II describes the design of proposed modified OpAmp. The simulation results are listed and discussed in section III ahead with the comparison of previous work in section IV.Finally the conclusions are drawn in section V.

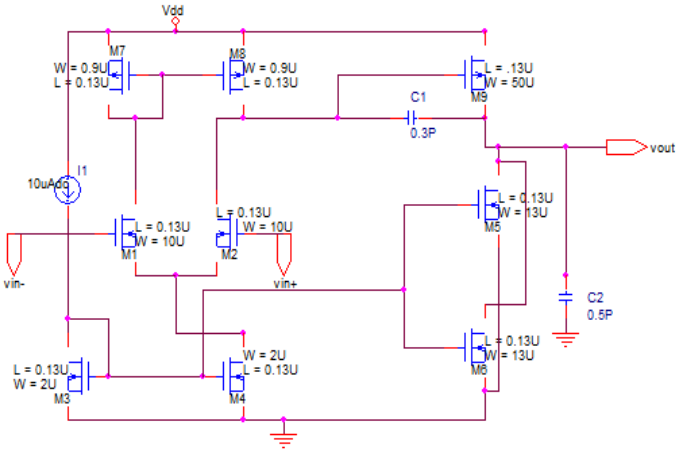


Fig.3 Conventional Two Stage OpAmp

II. MODIFIED TWO-STAGE CMOS OPAMP DESIGN

Conventional two stage OPAMP is used as the starting phase of this design. After the topology selection, specifications are set as per requirement and are shown in Table-2.

Table-2
specifications of OpAmp

Parameters(Units)	Target Specification
Supply Voltage(V)	1.2
Bias Current(μA)	5
Load Capacitor(pF)	0.5
Gain(dB)	>62
Unity Gain Bandwidth(MHz)	>15
Phase Margin(degree)	>70
Power Dissipation(μW)	<500

Model parameters for 130 nm MOS transistors such as mobility, threshold voltage and channel length modulation coefficient are extracted and are listed in Table-3.

Table -3
Model Parameters

Parameters(units)	nmos	pmos
Mobility μ(cm^2/v sec)	390	175
Threshold Voltage V_T(V)	0.39	-0.39
Oxide Thickness T_{OX} (nm)	1.7	1.7
Gamma	0.41	0.41

By following the common design procedure and considering the specified performance and model parameters, the sizes of the transistors and compensation capacitor are determined. The proposed modified two-stage OPAMP is shown in Fig.4.

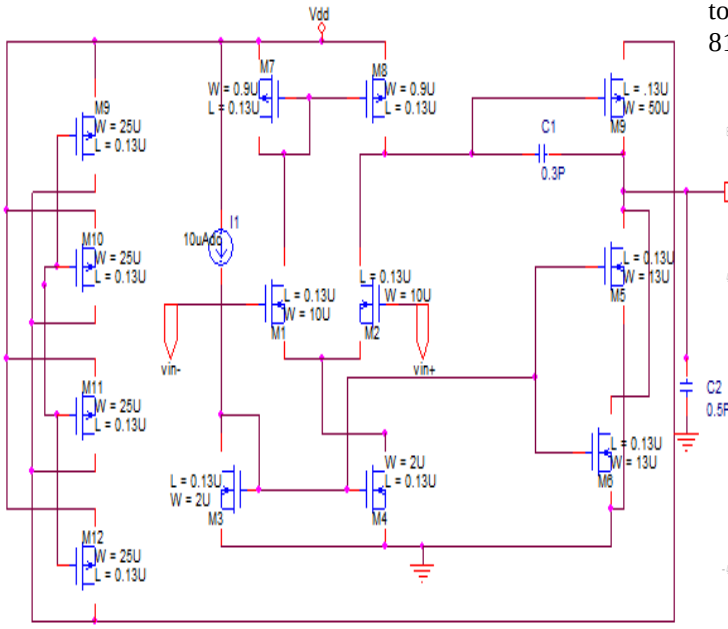


Fig.4 Modified Two Stage OpAmp

The differential input voltage to differential current. PMOS1 and PMOS2 form the current mirror load for NMOS1 and NMOS2, which recovers the amplified differential voltage. PMOS3 and NMOS5 in the second stage, forms the common source amplifier which amplifies the output of the first stage. The compensation capacitor of 0.3 pF is used between the input and output stage to obtain better stability. The gain of the design was achieved around 46.53dB and phase margin was 73° using conventional architecture. In the proposed modified architecture, transistors PMOS4, PMOS5, PMOS6 and PMOS7 are included to enhance the transconductance of the second stage so as to increase the gain. For this purpose their mode of operation has been controlled so that these additional transistors will not operate in saturation region. Hence channel length modulation coefficient of these four PMOS transistors will not lower the gain. NMOS6 is included to enhance the phase margin of the design.

III. SIMULATION RESULTS

The designed circuit is simulated with Orcad Cadence simulator Different test circuits are set for extraction of various performance parameters of the operational amplifier. A comparison of specifications and obtained results is given in Table 4.

AC analysis is performed to obtain gain, -3dB frequency, unity gain bandwidth and phase margin. The simulation result is shown in Fig.4.a. The gain and -3dB frequency of the designed OpAmp is found to be 65 dB and 42.29 KHz respectively. The Unity gain frequency is calculated to be 71.39 MHz The phase margin obtained at the UGB is 81°.

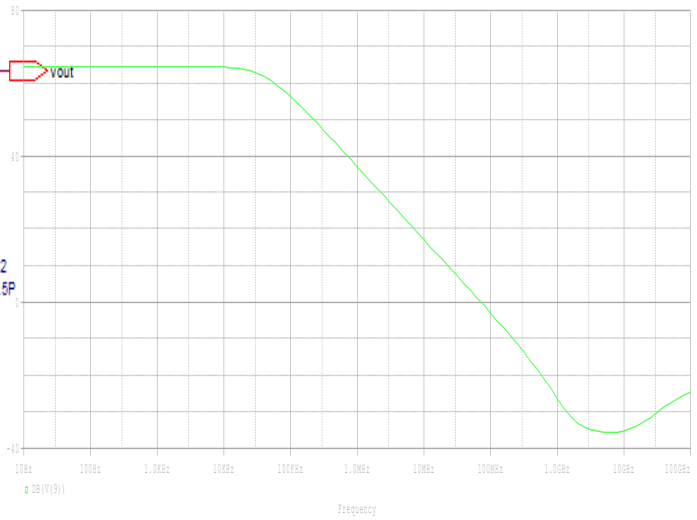


Fig.4.a Gain in dB

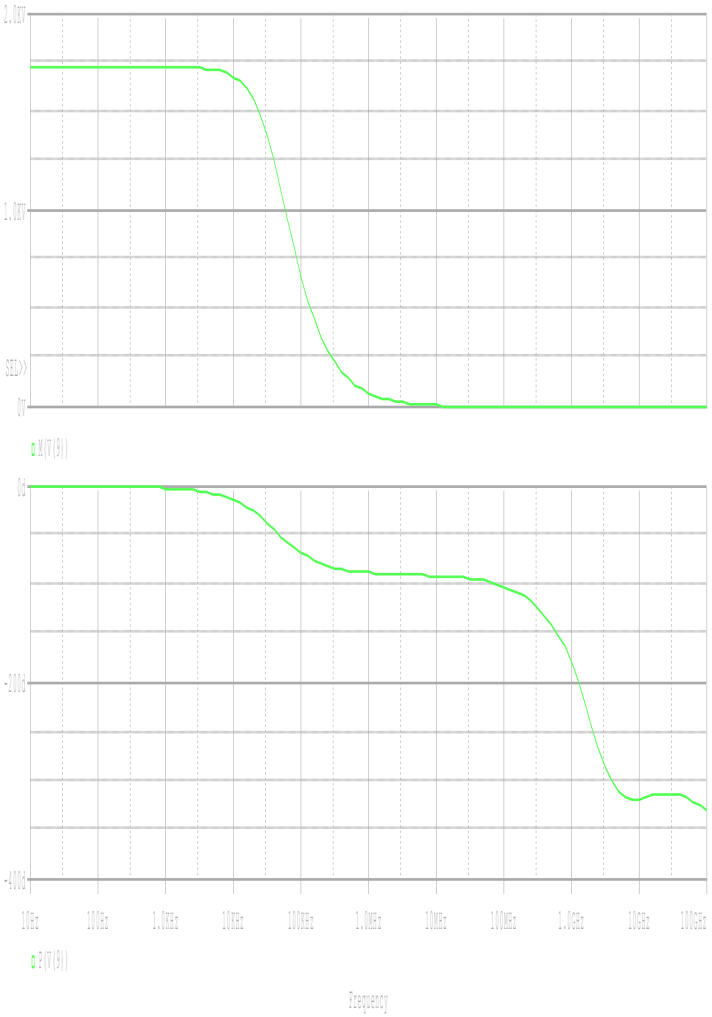


Fig.4b Phase Margin,-3dB and UGBW

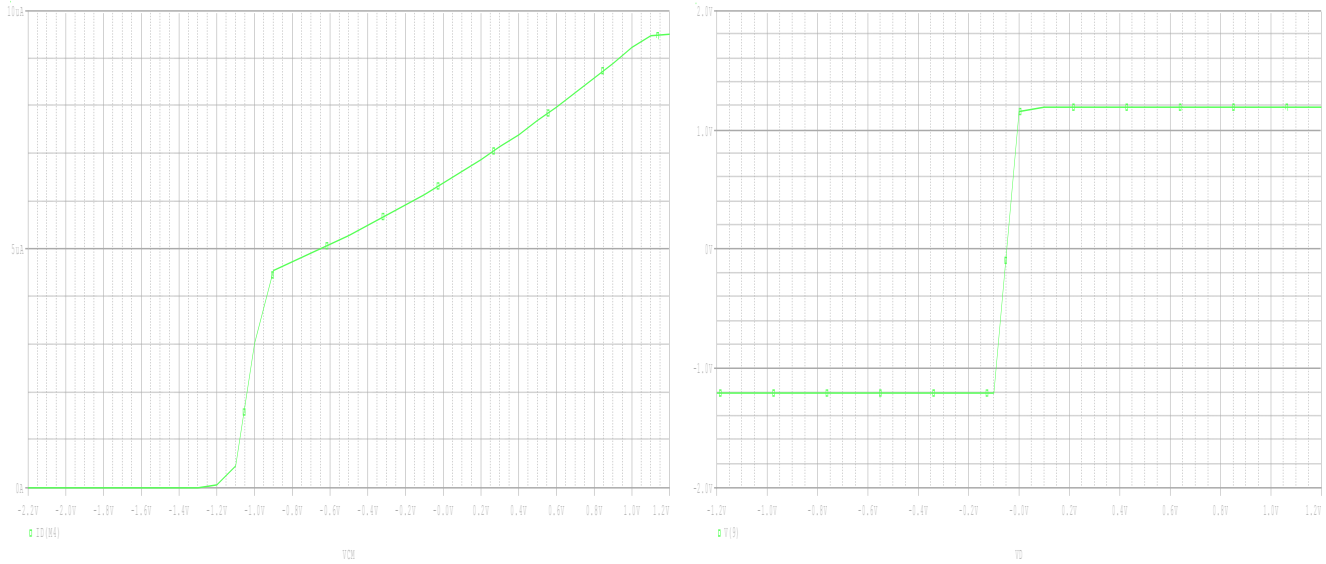


Fig.4 c Common Mode Gain and Differential Mode Gain

Table-4 Comparison With Previous Work

Parameters (Units)	This work	Ref [4]	Ref [6]	Ref [5]	Ref[3]Conventional Differential Amplifier	Ref [3]Double Differential Amplifier
Technology (nm)	130	500	180	180	180	180
Supply Voltage(V)	1.2	2.5	1.8	1.8	1.8	1.8
Gain(dB)	65	81	60.5	70.98	56	>95
-3dB Frequency (KHz)	42.29	-	-	5.41	-	-
Unity Gain Bandwidth (MHz)	71.39	5	1162	15.77	0.09	312
Phase Margin (degree)	81.08	65	68.3	58	65	56
Power Dissipation (µW)	363	378	7210	32.53	700	700

CMRR and PSRR can also calculate from AC analysis. For calculating the CMRR we first plot the differential mode gain plot and after this we plot the common mode gain .Fig. 4c plot is shown for differential mode gain and common mode gain.

IV. COMPARISON WITH PREVIOUS WORK

In this section a comparison of the proposed design has

been done with some previous works [2-5] and is shown in Table 4. Based on the comparison, it can be seen that the deigned OPAMP achieves higher phase margin of 81º with respect to previous works which accounts for better stability also distinguish the design from others. The design achieves acceptable gain while maintaining output swing. The design also exhibits satisfactory statistics with respect to bandwidth and extremely low power dissipation which is.363µW.

V. CONCLUSION

In this paper, the design of fast settling, low power and low offset voltage OPAMP is presented which exhibits high phase margin of 81°. This OPAMP high bandwidth of 71.39 MHz with acceptable gain and CMRR. The simulation results also show a good input common mode range and high PSRR. The simulation is done in Cadence 130 nm technology with 1.2 V power supply and dc bias current of 5 µA.

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