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A study of Low Power Design using CMOS/VLSI Technology for Communication

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Abstract: **The proposed research is aimed to study the low power consumption. The need for low power has caused a major paradigm shift where power dissipation has become as important consideration as performance and area. Power has become one of the most important paradigms of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. Hence to have very low power consumption, this research work is decided to study using CMOS/VLSI technology.**

Keywords: **CMOS, Submicron, Low Power Consumption.**

I.INTRODUCTION

In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth; this is because of the use of integrated circuits in computing, telecommunications and consumer electronics. The major concern of VLSI designer were area, performance, cost and reliability, power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like low power, reliable performance and improvements in the processing technology.

II. NEED FOR LOW POWER DESIGN

There are various interpretations of the *Moore's Law* that predicts the growth rate of integrated circuits. One estimate places the rate at 2X for every eighteen months. Others claim that the device density increases ten-fold every seven years. Regardless of the exact numbers, everyone agrees that the growth rate is rapid with no signs of slowing down. New generations of processing technology are being developed while present generation devices are at very safe distance from the fundamental physical limits. A need for low power VLSI chips arises from such evolution forces of integrated circuits. The Intel 4004 microprocessor, developed in 1971, had 2300 transistors, dissipated about 1 watts of power and clocked at 1 MHz. Then comes the Pentium in 2001, with 42 million transistors, dissipating around 65 watts of power and clocked at 2.40 GHz [1].

While the power dissipation increases linearly as the years go by, the power density increases exponentially, because of the ever-shrinking size of the integrated circuits. If this exponential rise in the power density were to increase continuously, a microprocessor designed a few years later, would have the same power as that of the nuclear reactor. Such high power density introduces reliability concerns such as, electromigration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance.

Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low

power VLSI design has assumed great importance as an active and rapidly developing field.

Another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power. A study by *American Council for an Energy-Efficient Economy* estimated that office equipment account for 5% for the total US commercial energy usage in 1997 and could rise to 10% by the year 2004 if no actions are taken to prevent the trend [2].

III. RECENT TRENDS IN CMOS TECHNOLOGY

The evolution of important parameter such as integrated circuit (IC) complexity, gate length, switching delay, supply voltage with a prospective vision down to the 11 nm CMOS technology.The naming of the technology nodes (130, 90, 65, 32, 22, 16, 11nm) comes from the International Roadmap for semiconductors [ITRS2009]. The trends of CMOS technology improvement continues to be driven by the need to

1. Integrate more functions within a given silicon area
2. Reduce Fabrication cost
3. Increase operating speed
4. Dissipate less power

Table 1 gives an overview of the key parameters for technological nodes from 130nm, introduced in 2001, down to 11nm, which is supposed to be in production in the 2015-2018 timeframe [3] [4].

Table 1. Technological evolution and forecast upto 2015 [4]

Technology node	130nm	90nm	65nm	45nm	32nm	22nm	16nm	11nm
First production	2001	2003	2005	2007	2009	2011	2013	2015
Effective gate length	70nm	50nm	35nm	30nm	25nm	18nm	12nm	9nm
Gate material	Poly	Poly	Poly	Metal	Metal	Metal	Dual?	Triple?
Gate dielectric	SiO_2	SiO_2	SiON	High K	High K	High K	High K	High K
Raw Mgates/mm^2	0.25	0.4	0.8	1.5	2.8	5.2	9.0	16.0
Memory point(μ^2)	2.4	1.3	0.6	0.3	0.17	0.10	0.06	0.06

IV. LIMITATIONS OF SUB-MICRON CMOS TECHNOLOGY

In order to design a CMOS PA, one must first understand the limitations of submicron CMOS technology with respect to PA implementations. The major limitations are low breakdown voltages, low transconductance-to-current ratio, and low substrate resistivity, as will be discussed successively.

a) Low Breakdown Voltages

The gate oxide breakdown occurs when the electric field in the oxide exceeds a certain value (about 0.07 V/°A in silicon dioxide). This process is destructive to the transistor because it results in a permanent short circuit between the gate and the channel. As the gate length in a CMOS technology shrinks, so does the thickness of gate oxide to avoid short channel effects [6]. Thus, the maximum allowable gate voltage for a sub-micron CMOS device is greatly limited. In addition to gate oxide breakdown, the drain-substrate pn junction will conduct a large current if the reverse bias applied to it exceeds a certain value [6]. This breakdown is nondestructive, but limits the maximum PA voltage swing at the drain of the device.

b) Low Transconductance-to-current Ratio

When the velocity saturates, the ratio of the transconductance to the current for a short-channel MOS device is [7]

$$\frac{g_m}{I} = \frac{1}{V_{GS} - V_t} = \frac{1}{V_{ov}}$$

For a bipolar device, this ratio is $1=V_T$, where the thermal voltage V_T is 26 mV. In contrast, the overdrive *V*ov for MOS transistors is typically chosen as several hundred mV. Thus, the transconductance per given current is much lower for MOS devices than for bipolar devices. To accommodate this small transconductance, either the input signal amplitude or the device size of the PA output stage has to be increased. However, either approach will increase the loading for the driving stage, thus resulting in higher power consumption of the driver stage. Increasing the input signal amplitude can also dramatically degrade the PA linearity because the third-order nonlinearity of the device current is directly proportional to the cube of the input voltage amplitude. Thus, higher nonlinearity will be expected for MOS devices than for bipolar devices.

c) Low Substrate Resistivity

In an integrated implementation, a PA resides on the same substrate as other circuit blocks, some of which may be very sensitive. Since many CMOS processes use low resistivity substrates, PA signals can be easily conducted across long chip distance to corrupt adjacent circuit blocks. Thus, substrate isolation is a crucial design issue for integrated PA implementations. In addition, a low-resistivity substrate has a detrimental effect on spiral inductors built above it [8]. This is because the low resistivity allows for creation of eddy currents,

which reduce the effective magnetic field, thus the quality factor of the spiral inductor.

V.CONCLOSION

The basic theory of Low Power Design along with various Limitation has been discussed This paper has illustrated the significance of Low Power design in the communication and the trends in CMOS Technology based on technology information available from integrated manufacturers. This article reviews various strategies for designing low power circuit and system .The article concludes with the future challenges that must be met to design low power, high performance systems.

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