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Low-Testing Time, Low-Power and High-Speed Implementation of 3-Weight Pattern Generation Based On Accumulator Cell

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ABSTRACT: The fault coverage and hardware over head of a circuit is an important problem in VLSI circuits and systems. To overcome this problem pseudorandom Built-in-self-test (BIST) generators have been widely utilized to test VLSI circuits and systems. A Pseudorandom pattern generator is used for generating test patterns. A weighted Pseudorandom Built-in-self-test (BIST) schemes have been utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets a comprising three weights, namely 0, 1, and 0.5 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power. Since accumulators are commonly found in current VLSI circuits, this scheme can be efficiently utilized to drive down the hardware of BIST pattern generation, as well. The test patterns are generated automatically (ATPG) for a benchmark circuit by using 3-weight pattern generation. In this paper maximum numbers of faults are covered with low testing time and low power.

Keywords: - Accumulator cell, BIST- Built In Self-Test, CUT - Circuit under test, VLSI testing, weighted test Pattern Generation

I.INTRODUCTION

The integrated circuits are defined as the numbers of discrete components (transistors, resistors and capacitors) are fabricated on single silicon chip with some set of predefined markings and measurements. The task of testing such integrated circuit to verify correct functionality is extremely complex and often very time consuming. A widely accepted approach to deal with the testing problem at the chip level is to incorporate Built-In-Self-Test (BIST) capability inside a chip. Built- In-Self-Test (BIST) is the capability of a circuit to test itself. BIST is a design technique in which parts of a circuit are used to test the circuit itself. BIST represents a merger of the concepts of built-in test (BIT) and self test.This increases the controllability and the observability of the chip, thereby making the test generation and fault detection easier. Therefore, weighted pseudorandom techniques have been proposed where inputs are biased by changing the probability of a “0” or a “1” on a given input from 0.5 (for pure pseudorandom tests) to some other value. Weighted random pattern generation methods relying on a single weight assignment usually fail to achieve complete fault coverage using a reasonable number of test patterns since, although the weights are computed to be suitable for most faults, some faults may require long test sequences to be detected with these weight assignments if they do not match their activation and propagation requirements. Multiple weight assignments have been suggested for the case that different faults require different biases of the input combinations applied to the circuit, to ensure that a relatively small number of patterns can detect all faults. Approaches to derive weight assignments for given deterministic tests are attractive since they have the potential to allow complete fault coverage with a significantly smaller number of test patterns. In order to minimize the hardware implementation cost, other schemes based on multiple weight assignments utilized weights 0, 1, and 0.5. This approach boils down to keeping some outputs of the generator steady (to either 0 or 1) and letting the remaining outputs change values (pseudo-) randomly (weight 0.5). This approach, apart from reducing the hardware overhead has beneficial effect on the consumed power, since some of the circuit under test (CUT) inputs (those having weight 0 or 1) remain steady during the specific test session. Current VLSI circuits, e.g., data path architectures, or digital signal processing chips commonly contain

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arithmetic modules [accumulators or arithmetic logic units (ALUs)]. This has fired the idea of arithmetic BIST (ABIST). The basic idea of ABIST is to utilize accumulators for built-in testing (compression of the CUT responses, or generation of test patterns) and has been shown to result in low hardware overhead and low impact on the circuit normal operating speed. Accumulator-based test pattern generation scheme was introduced by different authors. It was proved that the test vectors generated by an accumulator whose inputs are driven by a constant pattern can have acceptable pseudorandom characteristics, if the input pattern is properly selected. However, modules containing hard-to-detect faults still require extra test hardware either by inserting test points into the mission logic or by storing additional deterministic test patterns. In order to overcome this problem, the scheme generates test patterns having one of three weights, namely 0, 1, and 0.5 therefore it can be utilized to drastically reduce the test application time in accumulator-based test pattern generation. However, the existed accumulator based 3-weight pattern generation scheme possesses major drawbacks: 1) it can be utilized only in the case that the adder of the accumulator is a ripple carry adder; 2) it requires redesigning the accumulator; this modification, apart from being costly, requires redesign of the core of the data path, a practice that is generally discouraged in current BIST schemes; and 3) it increases delay, since it affects the normal operating speed of the adder. The proposed scheme low-testing time, low-power and high speed 3-weight pattern generation based on accumulator cell have advantages compare with the existed scheme proposed. More precisely: 1) it does not impose any requirements about the design of the adder (i.e., it can be implemented using any adder design); 2) it does not require any modification of the adder; and hence, 3) does not affect the operating speed of the adder.

II. 3-WEIGHT PATTERN GENERATION BASED ON ACCUMULATOR CELL

Current VLSI circuits and systems, e.g., microprocessors, digital signal processors and data path architectures are commonly contain arithmetic modules [accumulators or arithmetic logic units (ALUs)].accumulator cell contains flip-flops and adders. In this the upper D-flip flop uses set as reset and reset as set inputs. The output of upper D-flip flop is given as input of full adder. The output of full adder is connected with another d-flip flop with actual set and reset inputs. Full adder uses 3 inputs, 2 inputs from output of both D-flip flops, and another input is Cin. The sum output of full adder is given as input of D-flip flop.so the out puts of D-flip flop is A[i] and B[i].

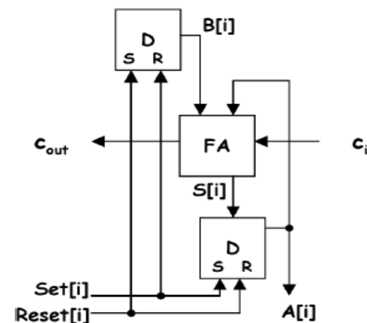

Fig1: Accumulator cell

(i)D-flip flop:

D-flip flop is a sequential logic circuit that stores the 1-bit binary out put data and it is designed by using SR-Latch.The SR-latch is designed by using a bistable element with NAND,NOR or INVERTER.D-flip flop is shown in below figure

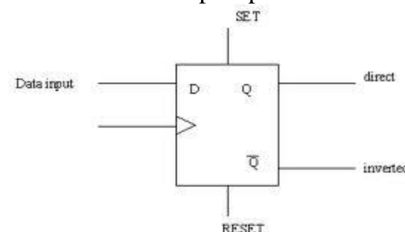

Fig 2:D-flip flop

(ii)Adder:

Adder is a combinational logic circuit that performs binary addition between different binary inputs. Based on number of inputs adders are design. The classification of adders is half adder and Full Adder. The full adder is shown in below figure

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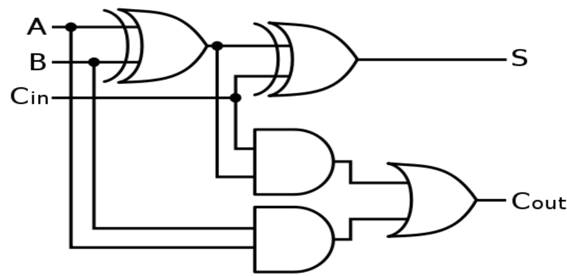

Fig3:Full adder

Truth table for full adder is shown in below:

TRUTH TABLE OF THE FULL ADDER

#	Cin	A[i]	B[i]	S[i]	C_{out}	Comment
1	0	0	0	0	0	
2	0	0	1	1	0	$C_{out}=C_{in}$
3	0	1	0	1	0	$C_{out}=C_{in}$
4	0	1	1	0	1	
5	1	0	0	1	0	
6	1	0	1	0	1	$C_{out}=C_{in}$
7	1	1	0	0	1	$C_{out}=C_{in}$
8	1	1	1	1	1	

III.Operation of accumulator cell in different configurations:

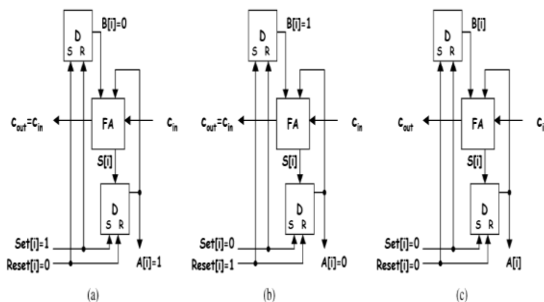

Fig4: accumulator cell configurations

Operation of the accumulator cell:

I). For A[i] =1 , We give set[i]=1 and reset[i]=0 and hence A[i]=1 and B[i]=0. Then the output is equal to 1, and Cin will be equal to Cout.Then Cin is transferred to the Cout.

II). For A[i] =0 , We give set[i]=0 and reset[i]=1 and hence A[i]=0 and B[i]=1. Then the output is equal to 0, and here Cin is equal to Cout. Then Cin is transferred to the Cout.

III). For A[i] = "-", set[i] =0 and reset[i] =0. The D input of the flip-flop of register B is driven by either 1 or 0, depending on the value that will be added to the accumulator inputs in order to generate Satisfactorily random patterns to the inputs of the CUT.

IV.Existed scheme block diagram:

The shown existed scheme generate patterns for different input combinations like set[i] =1 and reset[i] =0, set[i] =0 and reset[i] =1 and set[i] =0 and reset[i] =0.but the complete fault coverage did not achieve

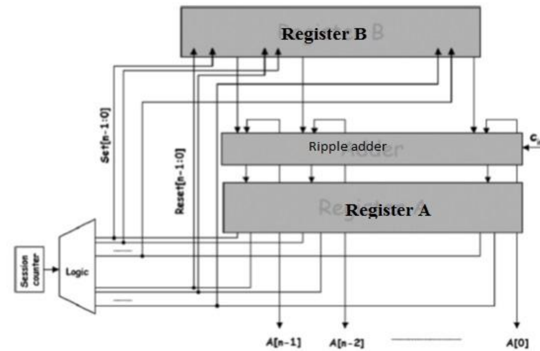

Fig5: existed scheme with ripple adder

with low testing time, low power and low hard ware. And the disadvantages of existed system mentioned below.

(i)Existed scheme disadvantages:

- It can be utilized only in the case that the adder of the accumulator is a ripple carry adder.
- It requires redesigning the accumulator; this modification, apart from being costly, requires redesign of the core of the data path, a practice that is generally discouraged in current BIST schemes.
- It increases delay, since it affects the normal operating speed of the adder.

V.Proposed scheme block diagram:

The proposed scheme was introduced by doing changes in existed scheme, that is in place of ripple adder place carry look ahead adder and achieve the complete fault coverage with low testing time, low power and low hard ware. And the proposed system with carry look ahead adder RTL is show in below figure.

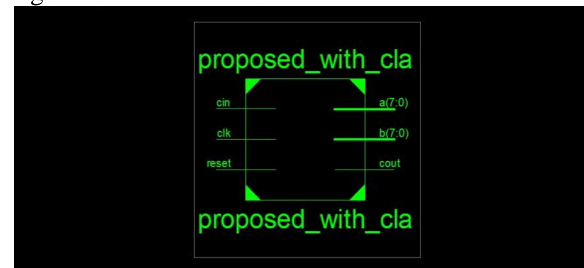

Fig6:proposed scheme with carry look ahead adder.

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The praposed scheme block diagram is shown in below figure.

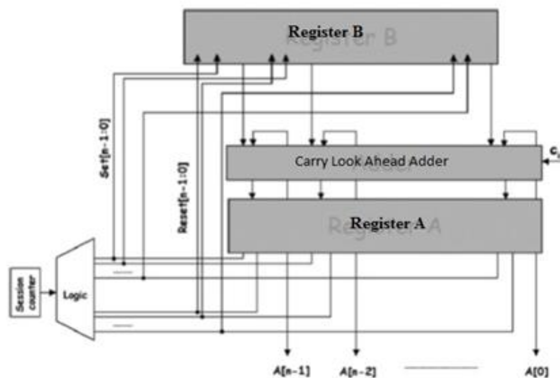


Fig7: proposed scheme with carry look ahead adder

The praposed scheme RTL diagram is shown in below figure.

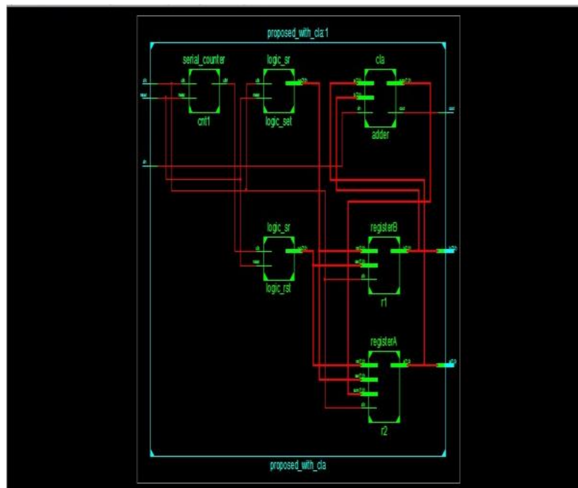


Fig8: Praposed scheme RTL diagram

(i)Proposed scheme advantages:

- It does not impose any requirements about the design of the adder
- It does not require any modification of the adder.
- Does not affect the operating speed of the adder.

(ii)Proposed scheme application:

- Test to integrated circuits and systems.
- Digital electronics and embedded system testing.
- BIST Applications

VI. SIMULATION RESULTS

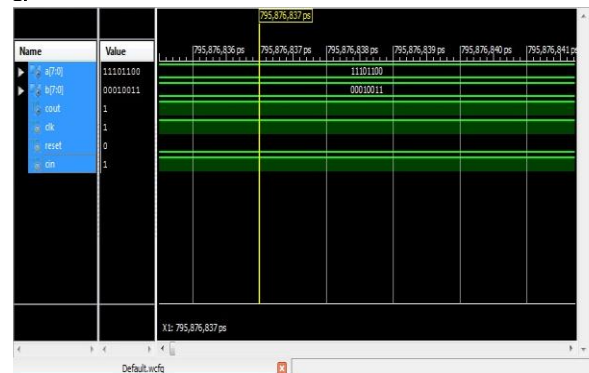
Verilog HDL is an industry standard language used to create analog, digital, and mixed-signal circuits. HDL's are languages which are used to describe the functionality of a piece of hardware as opposed to the execution of sequential instructions like that in a regular software application. Verilog code is generated for this accumulator circuit using 6.4c.Then RTL schematic is produced using XILINK 12.1.These test patterns are implemented in FPGA SPARTAN 3(XC3S400 PQ 208).

The simulation result for the basic accumulator is shown below for given input combinations. They are

If reset=0, set=0 clk=1, cin=cout,

Now the proposed scheme generates patterns for the given input combinations and set given internally by the logic circuit in accumulator cell .if clock=1,reset=0,then cin=cout.

I.



In this simulated wave form the cout should equal to cin,i.e either 0 or 1 and cin transferred to cout.Then a[i] and b[i] produces pattern generations.those pattern generations are usefull for testing fault coverage in integrated circuits and systems.

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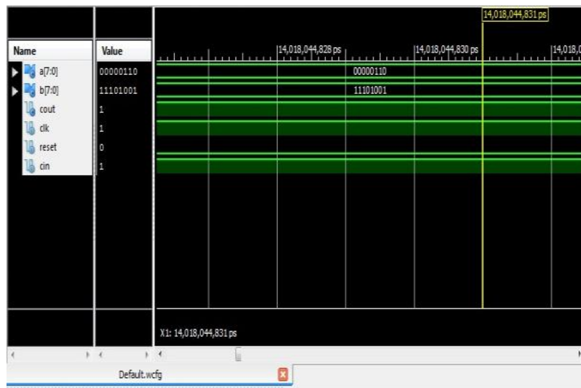
II.



In this simulated wave form the cout should equal to cin,i.e either 0 or 1 and cin transferred to cout.Then a[i] and b[i] produces pattern generations.those pattern generations are usefull for testing fault coverage in integrated circuits and systems.

The proposed paper shows result interms different parameters.and those parameters are shown with comparing of existed scheme results in below figures.

[A].Usage of Hardware components for existed scheme:

S.No	Hardware component	Quantity
1	Counter	3
2	4-bit up counter	2
3	8-bit up counter	1
4	Register	36
5	1-bit register	34
6	8-bit register	2
7	XORs	10
8	1-bit XOR2	2
9	1-bit XOR3	8

[B].Usage of Hardware components for proposed scheme:

S.No	Hardware Component	Quantity
1	Counter	1
2	8-bit up counter	1
3	Registers	20
4	1-bit register	18
5	8-bit register	2
6	XORs	4
7	1-bit XOR2	2
8	8-bit XOR3	2
9		

[C].

- Testing time for existed scheme is 374,628,538,545ps.
- Testing time for proposed scheme is 974,741,255ps.

[D]

- Total registers used for existed scheme is 66.
- Total registers used for proposed scheme is 42.

[E]

- Time delay for existed scheme is3.415ns
- Time delay for proposed scheme is2.365ns

[F]

- Total CPU time to execution completion for existed scheme is 4.87sec
- Total CPU time to execution completion for proposed scheme is 4.76sec.

VII. Conclusion

Accumulator-based 3-weight (0, 0.5, and 1) test-per-clock generation scheme, which can be utilized to efficiently generate weighted patterns without altering the structure of the adder.The test patterns are generated automatically for applied test vectors. But the existed system did not achieve complete coverage so that the proposed scheme,i.e The low testing time, low power and high speed 3-weight pattern generation based on accumulator cell technique can reduce the hardware overhead more than ~50%,hard ware implementation cost, testing time, time delay and fault coverage is more. The fault coverage is more and it is proved by adding carry look ahead adder in place of ripple adder. Finally in this paper maximum fault coverage is achieved.

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