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A Novel Low-Power High-Resolution ROM-less DDFS Architecture

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***Abstract*- A low-power high-resolution ROM-less Direct Digital frequency synthesizer architecture based on FPGA Design is proposed. This paper is equipped to generate a sinusoidal waveform with a new simple design method, which is endowed with high speed, low power and high spurious free dynamic range (SFDR) features.**

The proposed low power methodology is achieved by two methods: first, in a phase accumulator design by selecting a pipelined phase accumulator with 8-bit components that has lowest number of four input LUTs and number of occupied Slices. Second, in the circuit of TSC by proposing the circuit without an external power source.

The output frequency of proposed design is 195.35 kHz using built in clock frequency of 50MHz. However, the maximum operating frequency is 190.93MHz. In addition, the design has frequency resolution of 0.012Hz, which is promising to get very high tuning frequency with SFDR of 42 dBc or 70 dBFS.

***Index Terms*- Direct digital frequency synthesizer (DDFS); Phase Accumulator (PA); Digital to Analogue Converter (DAC); Triangle to Sine converter (TSC).**

I. INTRODUCTION

Direct digital frequency synthesizer is a digital system that generates frequency controlled sinusoidal signal for communication systems [1]. The conventional DDFS uses a ROM table; but large ROM increases the size and the power dissipation. In addition, it reduces the maximum clock frequency. Therefore, most of techniques for the DDFS have focused to reduce the size of the ROM table [2].

Nowadays, A DDS can achieve fast frequency switching in small frequency steps, over a wide band. In addition, it provides linear phase and frequency shifting with good spectral purity. The input to the system is a digital frequency control word, FCW, of length N, leading to an output frequency:

$$f_{out} = FCW.\, f_{clk}/2^N \qquad (1)$$

The output frequency is proportional to fclk. The frequency resolution is defined as $f_{clk}/2^N$. Both the switching speed and frequency resolution are higher than those of a PLL [3].

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A major advantage of a direct digital synthesizer (DDS) is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital processor control. Other inherent DDS attributes include the ability to tune with extremely fine frequency and phase resolution, and to rapidly "hop" between frequencies [4].

In order to achieve higher speed performance and lower power dissipation, CMOS CML is used to implement the logic cells[5]. Achieve an improvement in SFDR compared to the QLIP method, a ROM-less DDFS based on non-equal division parabolic polynomial interpolation method [6]. DDFS system based on Chebyshev polynomial interpolation method is proposed to obtain high speed and good SFDR [7]. A pipelined ROM-less DDFS architecture is built by employing the mixture of trigonometric approximation technique and CORDIC algorithm to reduce the frequency switching latency [8]. A ROM-less DDFS architecture based on a thermometer decoded nonlinear DAC and nonlinear interpolation has been proposed to improve SFDR [9].

The paper is organized as follows: In Section 2. The proposed low power ROM-less DDS based architecture is presented. The implementation strategies are presented in Section 3. While the results and discussions are provided in Section 4. Finally, conclusion is presented in Section 5.

II. PROPOSED LOW POWER ROM-LESS DDS ARCHITECTURE

The block diagram of the proposed low power, ROM-less direct digital synthesizer architecture is shown in Fig. 1. The details of the block diagram are discussed as follow:

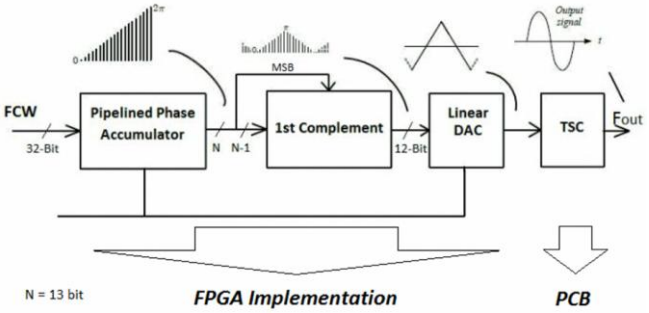

Figure 1. Proposed Low Power ROM-less DDS based on FPGA Design

A. 32-bit pipeline based Phase Accumulator design

Depending on the semiconductor process used to implement the DDFS, the desired speed may be impossible to achieve using a single-stage pipelined PA. A solution for

such a case is to pipeline the PA as m stages of n bits each, such that $mn = N$ (or equivalently $m = N/n$), Each adder outputs $n + 1$ bits: n sum bits, and one carry output bit. These bits are stored in an end register. The n stored sum bits then feed back into the adder, and the latched carry output bit connects to the carry input of the adder in the next pipeline stage [3].

We used a low power 32-bit Phase Accumulator with 4-stage pipelined architecture as shown in Fig. 2. The Accumulator is designed using CLA adder that improves speed by reducing the amount of time required to determine carry bits. The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits [10].

We can calculate the sum of CLA adder using following equations:

The carry C_i is generated by:

$$C_i = G_i + P_i \bullet C_{i-1} \quad (2)$$

Where

$$G_i = A_i \bullet B_i \quad (3)$$

$$P_i = A_i + B_i \quad (4)$$

The sum S_i is generated by:

$$S_i = C_{i-1} \oplus A_i \oplus B_i \quad (5)$$

When we design 8-bit CLA adder so:

$C_1 = G_0 + P_0.\ C_0$

$C_2 = G_1 + G_0.\ P_1 + C_0.\ P_0.\ P_1$

$C_3 = G_2 + G_1.\ P_2 + G_0.P_1.P_2 + C_0.P_0.P_1.P_2$

$C_4 = G_3 + G_2.P_3 + G_1.P_2.P_3 + G_0.P_1.P_2.P_3 + C_0.P_0.P_1.P_2.P_3$

$C_5 = G_4 + G_3.P_4 + G_2.P_3.P_4 + G_1.P_2.P_3.P_4 + G_0.P_1.P_2.P_3.P_4 + C_0.P_0.P_1.P_2.P_3.P_4$

$C_6 = G_5 + G_4.P_5 + G_3.P_4.P_5 + G_2.P_3.P_4.P_5 + G_1.P_2.P_3.P_4.P_5 + G_0.P_1.P_2.P_3.P_4.P_5 + C_0.P_0.P_1.P_2.P_3.P_4.P_5$

$C_7 = G_6 + G_5.P_6 + G_4.P_5.P_6 + G_3.P_4.P_5.P_6 + G_2.P_3.P_4.P_5.P_6 + G_1.P_2.P_3.P_4.P_5.P_6 + G_0.P_1.P_2.P_3.P_4.P_5.P_6 + C_0.P_0.P_1.P_2.P_3.P_4.P_5.P_6$

$C_8 = G_7 + G_6.P_7 + G_5.P_6.P_7 + G_4.P_5.P_6.P_7 + G_3.P_4.P_5.P_6.P_7 + G_2.P_3.P_4.P_5.P_6.P_7 + G_1.P_2.P_3.P_4.P_5.P_6.P_7 + G_0.P_1.P_2.P_3.P_4.P_5.P_6.P_7 + C_0.P_0.P_1.P_2.P_3.P_4.P_5.P_6.P_7$

The input of pipelined Phase Accumulator is 32-bit while the output is truncated to only 13-bit so we get high tuning frequency and low power consumption.

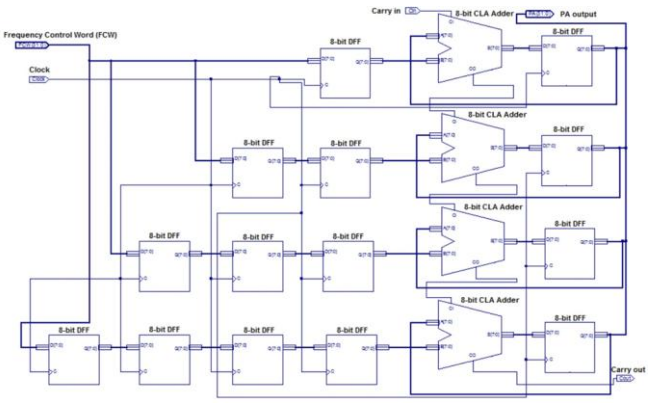

Figure 2. 32-bit pipeline based Phase Accumulator design [10].

We used MSB to design an up-down accumulator to produce the sine function. By using this way, we do not waste two bits to form the quadrant of the sine function as old methods. Making it suitable for up-down conversion, with up conversion we get sine function from 0 to π. Moreover, with down conversion we can get sin function from π to 2π. The operation speed of DDFS can be enhanced. The frequency resolution of proposed 32-bit PA with 8-bit components is 0.012Hz when clock frequency is equal to 50MHz.

B. *1's Complement Processing*

The 1's complement is the best tools to convert the output sawtooth samples into triangle samples. Let us recall the operation of an XOR gate. Note that if one input is 0, the output equals the other input. On the other hand, if one input is 1, then the output equals the complement of the other input. Thus, we can use XOR gates to perform a one's complement on command.

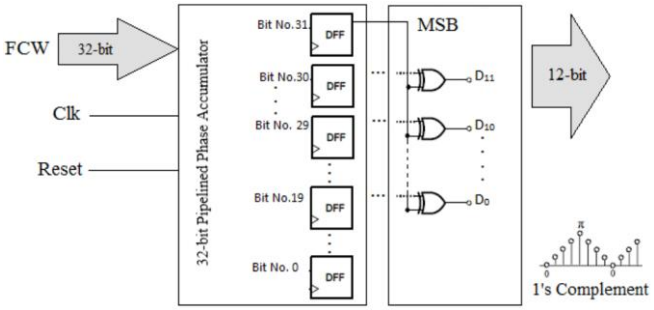

Figure 3. The truncated 13-bit of PA is driven to 1'Complement

As shown in Fig. 3. The truncated 13-bit of pipelined Phase Accumulator output is inputs to XOR gates; we will take the MSB as common input for each XOR gate. While each bit from the other, 12-bit is the second input for XOR gates.

C. *Linear DAC*

The DAC (LTC2624) incorporates a power-on reset circuit. During power-up, the voltage outputs raise less than 10mV above zero scale; and after power-up, they stay at zero scale until a valid write and update take place.

D. *Proposed TSC Circuit*

The traditional approaches in developing triangle-to-Sine converter have been adopted as follows:

1- Diode Shape technique: It has the advantage of elimination of the two transistors, which lead to the elimination two current sources in old circuit [11]. Therefore, this technique does not required DC source.

2- Piecewise linear approximation technique: Resistors with diodes and/or transistors are arranged to approximate a sine curve with a series of straight-line segments. Many different types of arrangements are possible, but an obvious disadvantage is that to accurately [12].

3- Lateral-PNP Transistors in CMOS Process technique: This technique is based on an approximation of a series of hyperbolic functions to a sine function [13].

4- Middlebrook & Richer JFET-based technique: It uses the nonlinear properties of a JFET to produce the sine shaping, using the JFETs symmetry in an elegant and very

distinctive configuration [14].

5- Proposed technique: We have proposed a very simple circuit to convert Triangle wave into Sine wave as shown in Fig. 4. It is based on L-Section RC circuit configuration. This technique does not required DC source, but needs a simple amplifier to validate the low output amplitude.

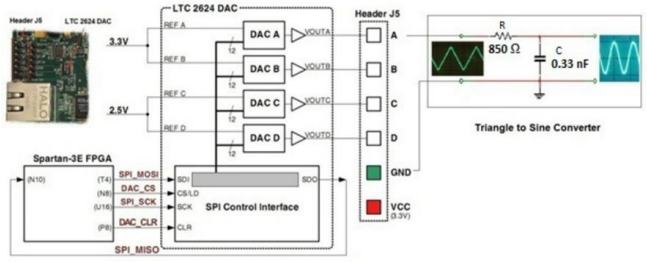

Figure 4. DAC of Spartan-3E FPGA is connected to TSC

III. Design and Implementation of Low Power ROM-less DDS Architecture

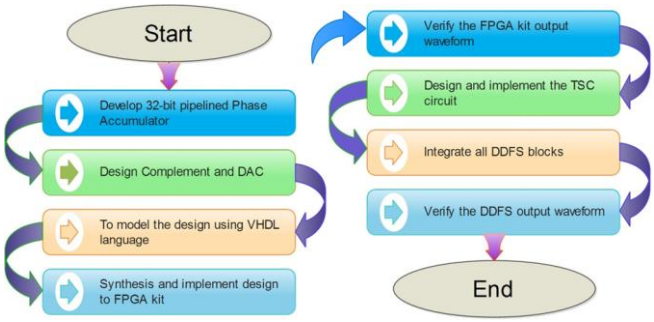

Figure 5. Flowchart for implementing low power ROM-less DDFS.

The proposed work can be performed using the following flowchart as shown in Fig. 5. The methodology of design is simple and meets the need for high-speed, low power and throughput of direct digital frequency synthesizer.

A. *Implementation of Low Power 32-bit Phase Accumulator*

We have designed and compiled the 32-bit pipelining PA using VHDL Hardware Description Language targeting for Xilinx Spartan 3E FPGA kit [10]. The Register Transfer Level (RTL) and of the 32-bit PA is shown in Fig. 6.

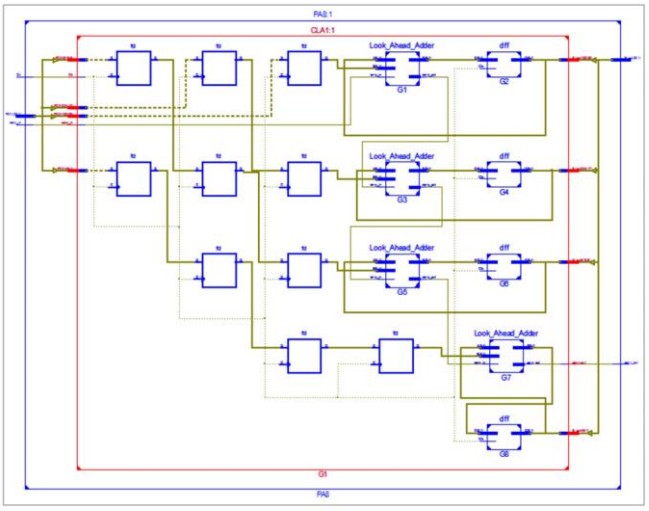

Figure 6. The Register Transfer Level (RTL) of the 32-bit PA [10].

The design summary of pipelined PA with 8-bit components using Spartan 3E FPGA is shown in Table 1. The design uses 64 of slice Flip Flops, 149 of 4 input LUTs, 86 of occupied Slices, and the Average Fan-out of Non-Clock Nets is 2.45 only. Note that the Table 1 is a picture captured from Xilinx ISE software.

Table 1. Design summary of 32-bit pipelined PA with 8-bit components [10].

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	64	9,312	1%
Number of 4 input LUTs	149	9,312	1%
Number of occupied Slices	86	4,656	1%
Number of Slices containing only related logic	86	86	100%
Number of Slices containing unrelated logic	0	86	0%
Total Number of 4 input LUTs	149	9,312	1%
Number used as logic	125		
Number used as Shift registers	24		
Number of bonded IOBs	67	232	28%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	2.45		

B. *Implementation of Low Power ROM-less DDS*

The hardware used to implement low power ROM-less DDFS was Xilinx Spartan 3E starter FPGA kit DAC (LTC 2624) that has Quad 12 bit DAC. It is a quadrature type 12 bit DAC. Therefore, it has four independent DAC's inbuilt within it. Therefore, we can use one of them at a time.

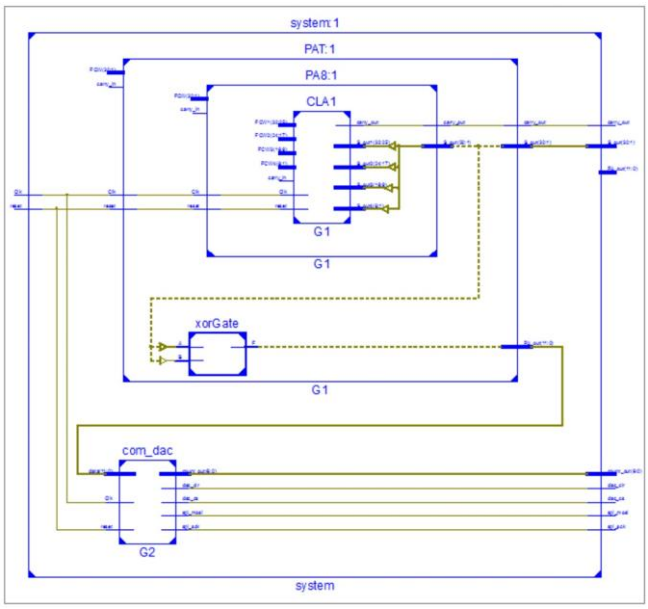

Figure 7. The Register Transfer Level (RTL) of low power ROM-less DDFS

For low Power Operation the DAC (LTC 2624) have 250µA per DAC at 3V. It is a very low power-consuming device. Hence, it is ideal for chip level application.

Table 2. Design summary of low power ROM-less DDFS

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Total Number Slice Registers	53	9,312	1%
Number used as Flip Flops	52		
Number used as Latches	1		
Number of 4 input LUTs	95	9,312	1%
Number of occupied Slices	52	4,656	1%
Number of Slices containing only related logic	52	52	100%
Number of Slices containing unrelated logic	0	52	0%
Total Number of 4 input LUTs	95	9,312	1%
Number of bonded IOBs	46	232	19%
Number of BUFGMUXs	2	24	8%
Average Fanout of Non-Clock Nets	3.73		

The Register Transfer Level (RTL) of the design is shown in Fig. 7, while design summary is presented in Table 2. The design uses 53 of slice Flip Flops, 95 of 4 input LUTs, 52 of occupied Slices, and the Average Fan-out of Non-Clock Nets is 3.73 only. Note that the table 2 is a picture captured from Xilinx ISE software.

IV. Results and Discussions

The gate level simulation plot of the 32-bit PA with 8-bit components is shown in upper Fig. 8. The triangle waveform output of DAC is shown in Fig. 9. While Sine waveform output of TSC circuit is shown in Fig. 10.

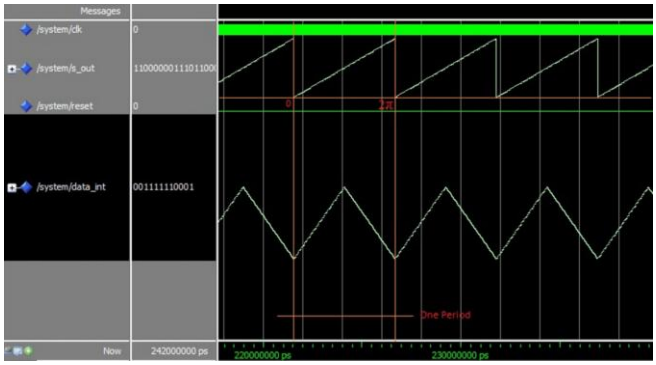

Figure 8. PA and 1's complement outputs f_{clk} =50MHz, FCW=1F0F0F0, f_{out}=200 kHz

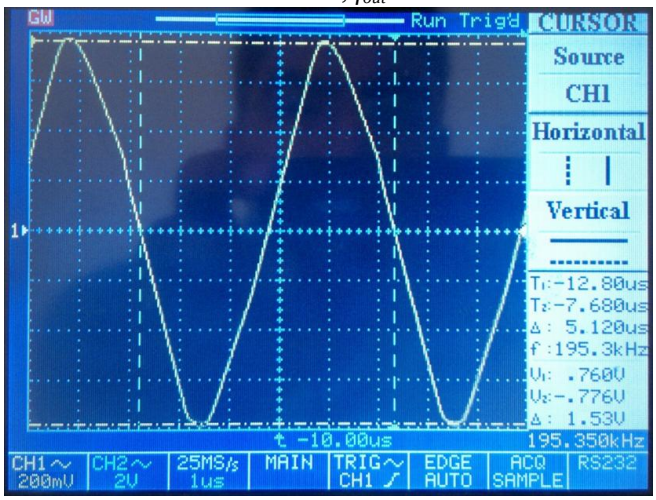

Figure 9. Triangle waveform output of DAC

Let us consider the characteristics of given signal shown in Fig. 9. The measured output frequency of that triangle wave is 195.35 kHz and the peak-to-peak voltage is 1.53v. The shape of output waveform is near to triangle wave but when it add to triangle-to-sine converter, we get the desired sine wave without any distortions.

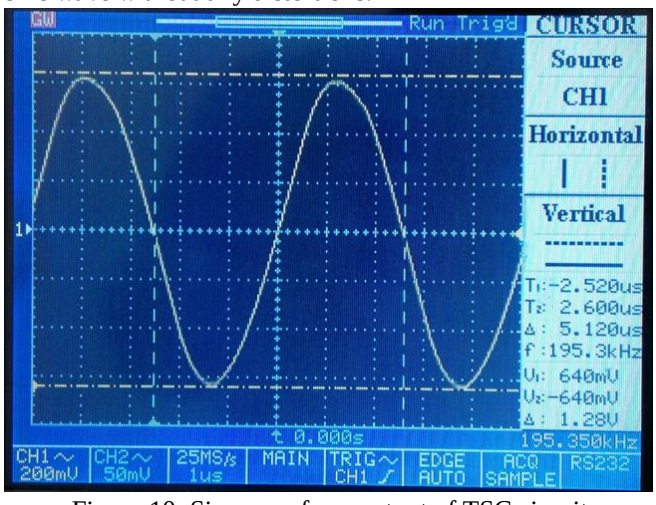

Figure 10. Sine waveform output of TSC circuit

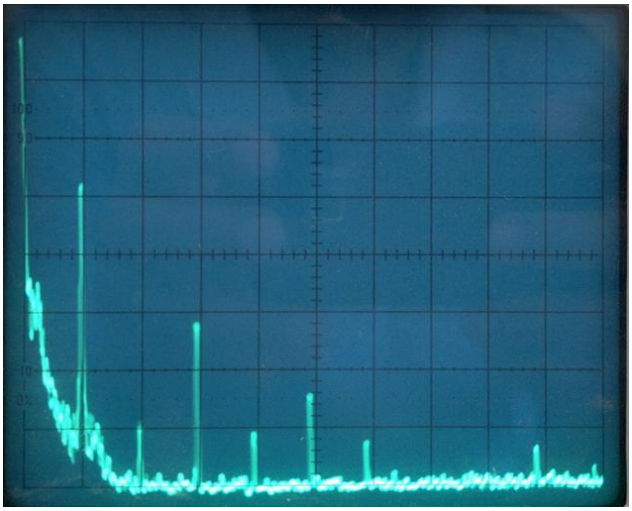

Figure 11. The spectrum analyzer output due to Sine waveform

Fig. 10, shows how we could obtain pure sine waveform by controlling the resistor and capacitor values. By adjusting the resistor value, we have got the desired sine waveform and the amplitude will be controlled. The measured peak-to-peak output voltage of 1.28v is suitable for low power applications.

The spectrum analyzer output due to sine waveform is shown in figure 11. It shows the difference between fundamental and highest next harmonic. The measured SFDR is about *42 dBc* at an output frequency of *195.35 kHz*. The maximum operating frequency of our proposed design prototype is *190.93MHz*, which can be extended to verify the speed requirements. The second harmonic could be eliminated using a suitable low pass filter.

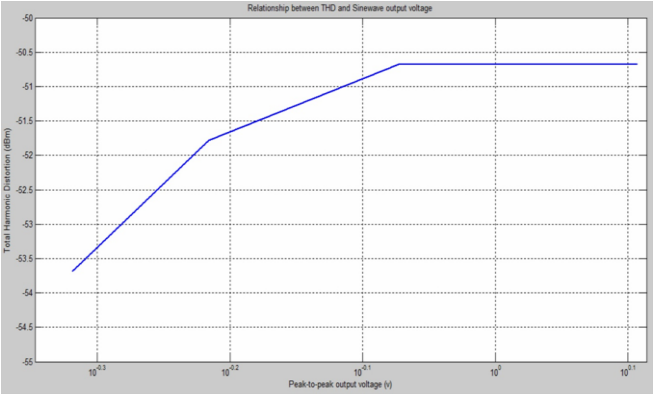

Figure 12. Measured THD for Sine wave output voltage

Total harmonic distortion (THD) analyzers are important tools in the design and construction of high performance frequency synthesizer architecture. Fig. 12 shows the relationship between the measured Sine wave output voltage and its THD. For very low distortion signals, say under 0.05% THD, the significant harmonic content will be in the 2nd thru 5th harmonics and above the 5th, noise tends to dominate. There is tradeoff between the measured output voltage amplitude, SFDR and THD. The higher output amplitude means lower SFDR and higher THD.

V. CONCLUSION

The proposed low power, ROM-less direct digital synthesizer architecture has been successfully designed and simulated. It uses a 32-bit pipelined phase accumulator to improve the operating speed and keep on wide range of frequency control word from 1 to 4294967295. The design features an SFDR that is better than 42 dBc for synthesized frequency. The proposed architecture has output frequency of 195.35 kHz when the built in clock frequency is 50MHz. In addition, it has 0.012Hz frequency resolution to get very high tuning frequency. There is a slight difference of the THD when the output signal frequency was not an integer multiple of the reference clock frequency.

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