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Survey of Reconfigurable Hardwares for Implementing Adaptive filters and study of its applications

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Abstract— this paper gives detailed survey of Reconfigurable hardwares required for implementing Digital signal processing Applications also the brief introduction, Applications and implementation details of Adaptive filter in reconfigurable hardware are briefly elaborated. Adaptive filter is type of digital filter having Self adjusting characteristics. Adaptive filters learn the statistics of their operating environment and continually adjust their parameters accordingly. Adaptive filters are well suited for filtering non-stationary signal environment. Least Mean Square (LMS) Adaptive filters have many applications in signal processing, speech processing as well in communications. Reconfigurable hardware has many advantages over dedicated hardware. Reconfigurable hardwares such as DSP processors, ASIC, General purpose processors and FPGA are well suited for implementing signal processing applications. LMS adaptive filters may be implemented using Field Programmable Gate Arrays (FPGAs) due to some of their attractive advantages that includes flexibility and programmability this paper mainly concentrate on adaptive filters application in communications such as Echo cancellation, channel Equalization , interference cancellation and specially in Smart antenna which is widely used in software defined radio(SDR)

***Index Terms*—LMS, ASIC, FPGA, software defined radio (SDR).**

I. INTRODUCTION

Reconfigurable hardwares have many advantages over fixed or dedicated hardwares. Dedicated hardware provides highest performance with lower power consumption but they lack behind the reconfigurable hardware in flexibility and reusability. Reconfigurable hardware provides reprogram ability and flexibility. Numerous reconfigurable hardware platforms are available to perform the required signal processing, each has its own strengths and weaknesses in terms of performance, programmability and power consumption. The designer must make trade-offs in these three design areas when determining the best digital hardware solution for a signal processing application implementation. Reconfigurable hardware platform includes DSP, GPP, ASIC and FPGA. Each one has its own advantages and disadvantages. Selection of reconfigurable platform for any application depends on the type of application and requirements.

This paper will cover the comparative analysis of selection of reconfigurable platform for digital signal processing application.

DSP is well suited to extremely complex math-intensive tasks, but cannot process high sampling rate applications due to its serial architecture. ASIC can meet all the constraints of digital signal processing, but it does not give design flexibility and requires long design cycle. FPGA is best over ASIC and DSP. FPGA provides high design flexibility, less time-to-market, risk-mitigation and lower system costs advantages, and FPGA has become the first choice for many digital circuits' designers [7].

In this paper, in order to show the performance of FPGA in digital signal processing applications, we implement an LMS based Adaptive filter on FPGA .LMS algorithm, originally proposed by Widrow and others, is widely used for adaptive filter. The least-mean-square (LMS) algorithm is similar to the method of steepest-descent in that it adapts the weights by iteratively approaching the MSE minimum. Widrow and Hoff invented this technique in 1960 for use in training neural networks. Instead of calculating the gradient at every time step, the LMS algorithm uses a rough approximation to the gradient In recent years, adaptive systems have resulted in a variety of applications such as communications, radar, sonar, seismology, mechanical design, navigation systems and biomedical electronics[2]

II. RECONFIGURABLE HARDWARES

Major requirement of implementation of Digital signal processing applications are high computational performance and speed due to their real-time characteristics. Reconfigurable hardware platform is used for implementing digital signal processing applications. Reconfigurable hardwares such as digital signal processor (DSP), general purpose processor, ASIC (Application specific Integrated circuits) and FPGA (Field programmable gate array) are mostly used in for signal processing. Selection of reconfigurable platform varies from application to application.

For Selection of reconfigurable hardware for particular application factors such as speed, performance, Programmability and flexibility in design are considered

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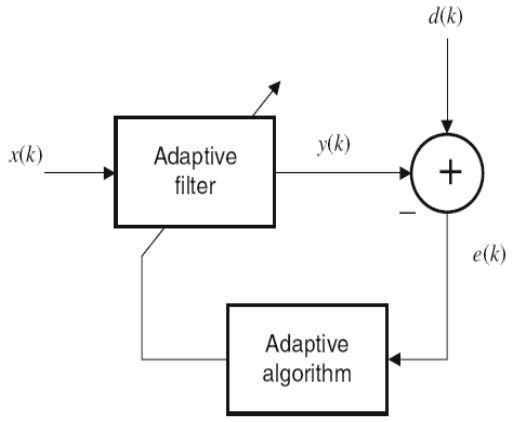
Reconfigurable Platform	Performance	Cost	Power	Flexibility	Programability
GPP	Low	Low	Medium	High	High
DSP	Medium	medium	Medium	Medium	high
ASIC	Very High	High	Low	Low	Low
FPGA	High	Low	Medium	Very High	High

Table 1: Comparison of Reconfigurable platforms

Table.1.shows comparison of various Reconfigurable platforms for implementing DSP applications.
General-purpose processors can execute a wide variety of programs, including DSP algorithms. However, their performance may not meet the application requirements. DSP processors generally achieve better Performance than general-purpose processors, but their architecture may not be optimized for the different requirements that DSP applications may have, such as speed, power, and word length.DSP processors are used where high computational speed and high design flexibility is required ASICs are optimized for a particular DSP algorithm.
These devices can achieve maximum performance and Have minimum power consumption, but they have high Development costs and lack of design flexibility and reprogram ability. Due to the cost and limited Flexibility of an ASIC, this approach may only be Feasible for high-volume designs. ASICs are used in application in which high performance is mandatory and in those applications in which power consumption is major issue.
FPGA allows designers to change the configuration of the hardware at any time. It provides an excellent alternative for performance, power, flexibility, and fault tolerance. Users may select between different trade-offs, such as performance versus fault tolerance, based on the application at hand.
Hence FPGA is Excellent over DSP processor, General purpose processor and ASIC, FPGA platform is chosen where high design flexibility, reprogrammability and fault tolerance is required [4].

III. ADAPTIVE FILTER

A filter is designed and used to extract or enhance the desired information contained in a signal. An adaptive filter is a filter with an associated adaptive algorithm for updating filter coefficients so that the filter can be operated in an unknown and changing environment. The adaptive algorithm determines filter characteristics by adjusting filter coefficients (or tap weights) according to the signal conditions and performance criteria. A typical performance criterion is based on an error signal; the error signal e (n) can be calculated by subtracting desired signal from filtered input signal. Basic structure of adaptive filter is shown in figure.1.



. Fig.1.Basic structure of Adaptive filter

Adaptive filter consist of digital filter having variable filter coefficient and adaptive algorithm[2].
Digital filter with variable filter characteristics may FIR (finite impulse response filter) or IIR (infinite impulse response filter) Selection of digital filter may vary from application to application. But FIR is widely used as filter in adaptive filter because of linear phase response and stability.
Adaptive algorithm is used to adjust or updates filter coefficient when input signal changes
Two types of algorithm used for updating filter coefficients are Least Mean Square (LMS) and the Recursive Least Squares (RLS) algorithms. The choice of algorithm is dependent upon needed convergence time and the computational complexity available, as statistics of the operating environment.
he LMS algorithm is the most widely used and popular adaptive algorithm[3].

This algorithm is described as follows.

$$y(n) = \sum_{i=0}^{M-1} Wi(n) * x(n - i) \quad (1)$$

$$e(n)=d(n)-y(n) \quad (2)$$

$$wi\ (n+1)=wi(n)+2ue(n)x(n-i) \quad (3)$$

In these equations, the tap inputs x(n), x(n-1),……,x(n-M+1) form the elements of the reference signal x(n), in which M-1 is number of delay elements. d(n) is the primary input signal, e(n) denotes the error signal . wi(n) is the tap weight at the nth iteration. Equation 3 shows the weight updation.the tap weights are update in accordance with the estimation error. And the scaling factor u is the step-size parameter. Step size parameter controls the stability and convergence speed of the LMS algorithm. The LMS algorithm is convergent in the mean square if and only if u satisfies the condition: $0 < u < 2$ / tap-input power

IV. FPGA IMPLEMENTATION PROCESS

In this part ,we are going to have a short introduction on FPGA design procedure. A simplified version of design process is given in the flowing diagram

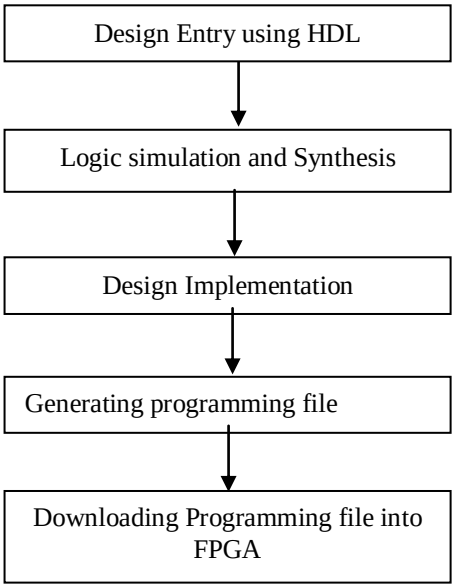


Fig.2.FPGA design Process

FPGA design procedure start with design entry. Different techniques for design entry are Schematic entry, Hardware Description Language entry and combination of both etc. Selection of any technique depends on the design and designer. Behavioral simulation is performed before synthesis process to verify RTL (behavioral) code and to confirm that the design is functioning correctly. Behavioral simulation can be performed on either VHDL or Verilog designs. Logic synthesis process which translates VHDL or Verilog code into a device netlist format. i.e a complete circuit with logical elements for the design. Implementation process starts with Translate which combines all the input netlists and constraints to a logic design file. This information is saved as a NGD (Native Generic Database) file. Map process divides the whole circuit with logical elements into sub blocks such that they can be fit into the FPGA logic blocks.The place and route process places and connects the sub blocks from the map process into logic blocks according to the constraints.

Next procedure after design implementation is generating programming file and downloading programming file into FPGA.

V. APPLICATIONS OF ADAPTIVE FILTER

Adaptive filter have number of application in signal processing, image processing and majorly in communication field. This paper focuses on application of adaptive filter in digital communication. These applications include Channel identification/Equalization, interference cancellation in CDMA, echo cancellation in telephone, Unknown System identification and Smart antenna.

A. Unknown Channel identification

One common adaptive filter application is to use adaptive filters to identify an unknown system, such as frequency response. An unknown communications channel or the frequency response. In the fig.3, the unknown system is placed in parallel with the adaptive filter Clearly, when e(k) is very small, the adaptive filter response is close to the response of the unknown system the same input is applied to both the adaptive filter and the unknown.

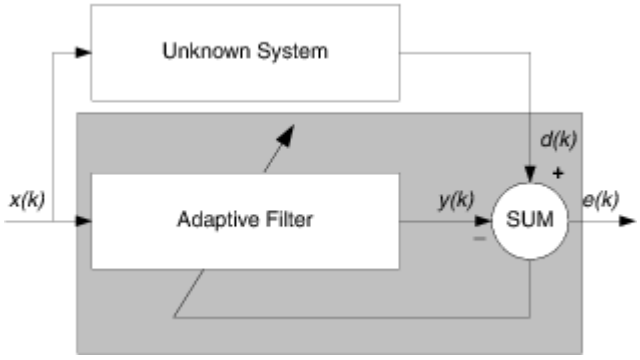


Fig.3.Unknown system identification

A. Adaptive Channel Equalization

To improve the bandwidth of a channel we can attempt to equalize communication channel. Telephone channel is a (stationary) communication channel with a continuous time impulse response, and then when symbols are transmitted the impulse response will cause a symbol to spread over many time intervals, this will introduce Intersymbol interference (ISI). The aim of a data equalizer is to remove this ISI.Compared to simple channel equalization, it should be noted that a data equalizer only requires equalizing the channel at the symbol sampling instants rather than over all time.fig.4.shows use of adaptive filter for channel equalization.

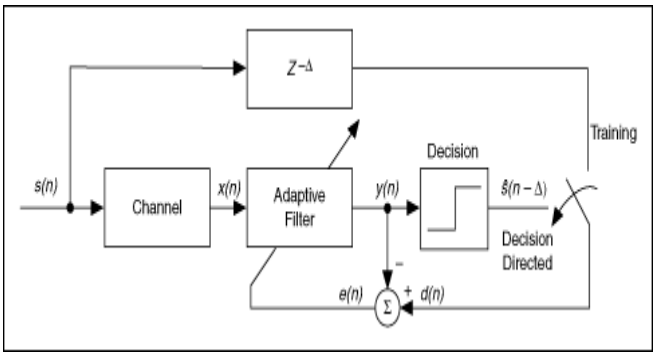


Fig.4. Adaptive filter for channel equalization

B. Adaptive Interference cancellation

In interference cancellation, adaptive filter remove noise from a signal in real time. To remove the noise, feed a signal n'(k) to the adaptive filter that represents noise that is correlated to the noise to remove from the desired signal.

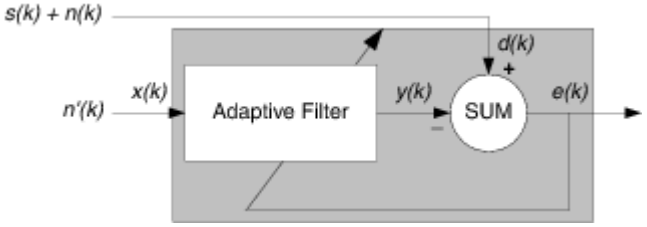


Fig.5. Adaptive interference Cancellation

the input noise to the filter remains correlated to the unwanted noise containing the desired signal, to remove the noise, the adaptive filter adjusts its coefficients to reduce the value of the difference between filtered signal y(k) and desired signal d(k), removing the noise and resulting in a clean signal.

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C. Adaptive filters for Echo cancellation

Echoes arise primarily in communication systems when signals encounter a mismatch in impedance. Figure shows a simplified long-distance telephone circuit. The hybrid circuit at the exchange converts the two-wire circuit from the customer's premises to a four-wire circuit, and provides separate paths for each direction of transmission. for example to allow multiplexing that is simultaneous transmission of many calls. Echos are cancelled by making an estimate of the echo and subtracting it from the return signal, yk.

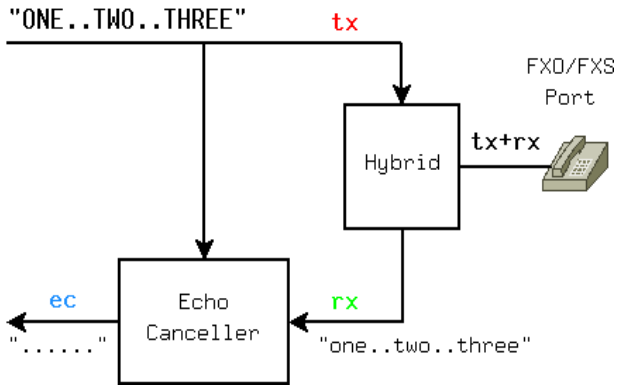

Fig.6.Adaptive Echo canceller.

D. Adaptive filter for Smart Antenna.

Smart antenna or Adaptive Array Antenna systems continually monitor their coverage areas and the system adapts to the user's motion providing an antenna pattern that tracks the user, achieving the maximum gain in the user's direction, and provide theoretically null and practically very low gain to any interference. For this purpose smart antenna base station combines an antenna array with a control unit that optimize reception and radiation patterns dynamically in response to the signal environment, i.e., mobile vehicle moving about the coverage area[8].

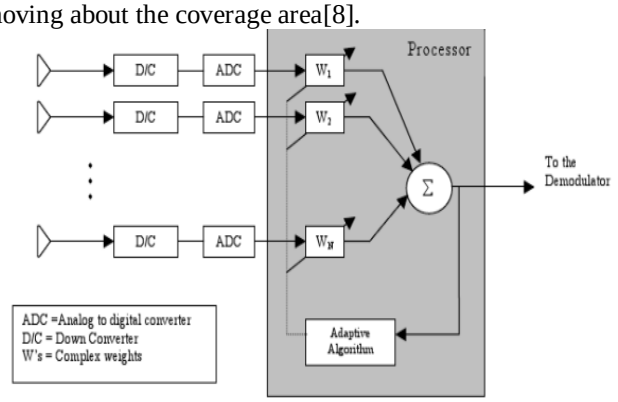

Fig 7: Block diagram of Adaptive array systems.

In fig 7, Adaptive filter is used for estimating the direction of arrival of all the incoming signals including the interfering signals and the multipath signals. The desired user signal is identified and separated from the rest of the unwanted incoming signal by using adaptive filter. Beam is steered in the direction of the desired signal and the user is tracked as he moves while placing nulls at interfering signal directions by Constantly updating the complex weights.

VI. CONCLUSION

Survey of various reconfigurable hardwares has been done in this paper. From that it can be concluded that FPGA is best choice in terms of cost, performance and flexibility for implementing digital signal processing application. Adaptive filter have many application in the field of signal processing and communications which are briefly elaborated in this paper.

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