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LOW POWER MULTIPLE SCAN CHAIN TEST FOR CIRCUIT WITH IMPROVED DELAY FAULT COVERAGE

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Abstract— **Very Large Scale Integrated circuits (VLSI) plays a wide role in electronic circuit design. The circuit has to be checked before launching in market. These are tested by applying test patterns to the Circuit Under Test (CUT). The tested results are compared with the benchmark circuits. This can be done by simulation. Three types of test vector generation, they are Exhaustive, Functional, and Structural. For testing the transition fault, scan based techniques are used. To generate the test pattern and to find the transition fault coverage, an accumulator based weighted pattern generation is being used. The two popular tests set namely broadside and skewed load test are used in it. Each test sets has its own drawbacks and many practical issues are associated with pattern generation and their applications. The combinational circuit should be tested under test vectors and low power consumption has to be achieved. This work can be done by HDL simulator and can be implemented in FPGA.**

***Index Terms*— Fault coverage, Broadside and skewed load test, VLSI Testing,An Acccumulator Based Weighted Pattern Generation**

I. INTRODUCTION

The test patterns are applied to the scan circuits in order to detect the delay faults, and reduce the power consumption weighted pseudorandom techniques have been proposed where inputs are biased by changing the probability of a "0" or a "1" on a given input from 0.5. Scan chain operate in shift, functional and hold mode [2]. Two test pattern can be applied to the scan circuits, the test pattern represented as S1R1, S2R2. The first pattern of the test is S1R1 and The second pattern of the test is S2R2 The scan circuit, two types of tests sets are available that is skewed load tests [3] and broadside tests [4]. In broadside test the first pattern is applied in functional mode, the second test pattern obtained by first pattern. In skewed load test the first pattern is applied in shift mode, the second test pattern obtained by single shift of first pattern.

The advantages and disadvantages of the two test vectors are presented in Table 1.

Table 1. Broadside and Skewed load

Comparison Item	Broadside	Skewed load
Fault Coverage	Lowest	Higher
Test Set Size	Largest	Smaller
Scan-Cell Type	Standard	Standard
Hardware Overhead	Lowest	Higher

The method of [5] restricts to partiotion the flip flops such that scan chain with first flip flop operate in shift mode while the second flip flop opeate in functional mode during the first pattern of the test. The method [6] proposed the enhanced scan test. It test is easy. This test method make the extra tristate holding logic to add the hardware overhead. The tristate holding logic is replaced to tristate holding latch. The latch is applied in the scan circuits which can store two bits instead of one bits.In both [5] and [6] the goal is to increase the transition fault coverage.

The method of [7] uses multipattern tests each pattern allocates a different mode to all the flip flops. The multipattern test generate the test sets to detect the transition fault coverage. Two test sets are generated namely, Launch-on-Shift (LOS) and Launch-on-Capture(LOC). The LOS and LOC test sets are differ in their methods. The new hybrids of LOS and LOC tests that launch transitions using both launch mechanisms are introduced. The new transition tests are used to detect the transition fault coverage without significant test length tets length penalty. In Scan based testing, the test data will be bring to the primary inputs apply the capture cycle for recover the fault coverage.

II. AN ACCUMULATOR BASED WEIGHTED PATTERN GENERATION

Weighted pattern testing is performed by weighting the signal possibility (probability that the signal is a1) for each input to the CUT. There are two issues in weighted pattern such as, testing are what set of weights to use and how to generate the weighted signals. For computing weight sets, many techniques have been projeced. It has been shown that in most of the circuits, multiple weight sets are necessary to achieve plenty fault coverage. For Scan Based, the weight sets must be stored on-chip and control logic is needed to switch linking them which can result in a lot of overhead. In order to decrease the hardware overhead for weighted pattern testing, researchers have looked for competent

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methods for on-chip generation of weighted patterns. The three weighted pattern comprising 0, 0.5, 1. The weighted pattern based on the full adder truth table, presented in table in 2.

Table 2. Full Adder Truth Table.

A	B	C_{IN}	C_{OUT}	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	1	1	1

To proposed the weighted pattern generation technique is based on the accumulator cell presented in Fig.1, it consist of full adder cell and D type flip-flop with asynchronous set and reset inputs whose output is also drive to one of the full adder inputs. In fig.1, to assume, without loss of generalization, the set and reset are active high signals. In the same Fig.1, the relevant cell of the driving register B[i] is also shown. For this accumulator cell, one out of three configurations can be utilized.

- For A[i] == 1 is required. Set[i] =1 & Reset[i] = 0 hence A[i] = 1 & B[i] = 0. Then output =1.
- For A[i]=0 is required Set[i] = 0,Reset[i] = 1,A[i] =0, B[i] =1.Then output = 0.
- For A[i] =‘--‘ is required Set[i]=0,Reset[i]=0, register B is driven by either 1 or 0, depending on the value that will be added to the accumulator inputs in order to generate satisfactorily random patterns to the inputs of the CUT.

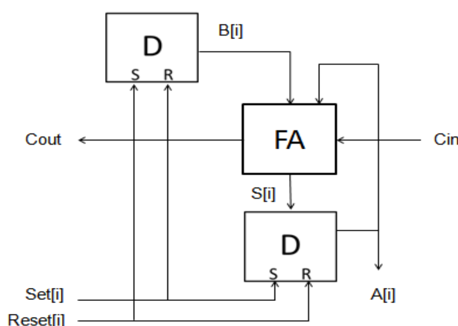

Fig 1: Accumulator Cell

III. SCAN BASED FOR MIXED TEST SET

The test generation pattern used for detect the transition fault coverage that produces the mixed test sets such as broadside and skewed load test. A mix of broadside and skewed load test yields developed analytical decision compared with a single test type.

This process starts from a mixed test set generated for fault detection. It uses two procedures to obtain new tests that are useful for diagnosis starting from existing tests. Both procedures allow the type of a test to be modified from broadside to skewed-load and from skewed-load to broadside. The first procedure is fault independent. The second procedure targets specific fault pairs.

A two-pattern test S1R1 and S2R2 is applied by scanning in S1 and then applying the primary input R1 and R2 in two successive clock cycles. The circuit operates in functional mode in order to allow fault effects to be captured in the flip-flops during the second clock cycle, and then be scanned out. Flexibility with depends upon the mode of operation of a scan chain under the first pattern. The three modes of operation considered in this brief are defined as follows:

The functional mode of operation is indicated by mi = func. In this mode scan chain captures the corresponding substate of the next-state obtained under the first pattern.

The shift mode of operation is indicated by mi = shft. In this mode scan chain captures a shifted version of si, 1, where si,1 is shifted by one bit. States are to be shifted to the right. The scan-in value that determines the left most bit of si, 2 can be determined arbitrarily.

The hold mode of operation is indicated by mi = hold. In this mode scan chain does not capture new values after the first pattern.

Table 3. Control Inputs

ME	SE	m_{i0}	m_{i1}	D_j
0	0	x	x	Y_j
0	1	x	x	Y_{j-1}
1 x		0	0	Y_j
1	x	0	1	Y_{j-1}
1	x	1	0	y_j

In scan based design, each scan chain has its own pair of control inputs that can determine its mode of operation during the first pattern of a test. To avoid the need for direct access to the n pairs of control inputs, the control inputs can be connected to a scan chain. Their values can be loaded in parallel with the scan-in operation that brings the circuit into state S1 for a test. S1R1 and S2R2.

A. FORMING A MIXED TEST SET

The procedure accepts a test set denoted by T_{init}, which may be T_{brd_skw} or a mixed test set. The procedure which is used will produces a test set denoted by T_{mixed}. The test set T_{mixed} is initially empty. The set of intension faults, initially

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consists of all the transition faults. The procedure starts by reordering T_{init} such that tests with subordinate numbers of uses of the shift mode appear earlier in the test set. This order will allow the procedure to decrease the use of the shift mode more considerably for tests with superior numbers of uses of this mode.

The numbers of tests in the mixed test sets never exceed that in $T_{brd_skw.}$ They are occasionally smaller if the tests with the modified settings detect more faults. The average switching activity of the tests in T_{mixed_func+I} and $T_{mixed_shft-.I}$ is lower than in T_{brd_skw} due to the decrease in the fraction of belonging where the shift mode is used. It is significantly lower for $T_{mixed_hold+.I}$ due to the wide ranging use of the hold mode. The maximum switching activity is reduced in many cases as well.

Low transition test patterns reduce the number of transitions in the scan-in vectors, and consequently the shift-power component caused by scan-in transitions. These methods have no undeviating control over the number of transitions in the scan-out vectors, thus, general reduction in power cannot be guaranteed. Further more, these methods do not address peak-power problems during the capture cycle. To improve the space and time efficieveness of storage and query systems in various scientific and commercial applications the date rearrangment techniques are applied. Run-length encoding is a prominent approach of compression in many areas, whose performance is significantly enhanced by achieving longer and fewer runs through data reordering.

The size of the test set produced by the test generation procedure grows slower than linearly with n. After static test compaction the increase in test set size with n is closer to the linear increase that is typical of compacted n-detection test sets. For an individual fault, the n-detection test set may contain a mix of broadside and skewed-load tests to reach the target of n detections. For the higher values of n, static test compaction typically improves the quality of the test set while reducing its size significantly. The strategy consists of a test generation procedure without test compaction heuristics and a static test compaction.

Table 4. Example Test

	Initial test			Modified Test		
M	Shft	Shft	Shft	Func	Hold	Shft
S1	1001	10110	01000	1001	10110	01000
S1	0100	11011	00100	0000	10110	00100

The test sets under the shift, functional, and hold mode. The initial test under the shift mode. The modified testing to replace the shift to functional mode and shift to hold mode. In shift mode shift the one bit position. The functional mode captures the corresponding the substrate of the next State obtained under the first pattern. In hold mode does not captures the new values after the first pattern. The different mode to applied in the scan chain to detect the transition fault coverage and reduce the power consumption.

IV. SIMULATION WORK

Generate the test patterns to find the transition fault coverage an accumulator based weighted pattern generation is being used. The test pattern generation by using weighted pattern generation. The simulated result shown in Xilinx software.

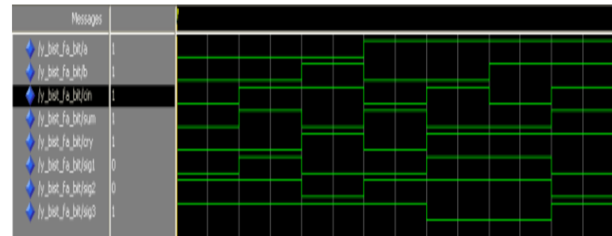

Fig 2. Full Adder component

In fig 2, the output is based on the full adder truth table. The input is A, B, Cin. and output is SUM, Cout. In Fig 3, the input is given to the set, reset and Cin then A and B is automatically Generated. Therefore Cin= Cout. The Carry input transfer to the Carry Output based on the An Accumulator Based Weighted Pattern Generation.

Generation the test pattern by using weighted pattern generation will achieve the transition fault coverage and reduce the power consumption under the test vectors. This can be obtained by Xilinx Simulation.

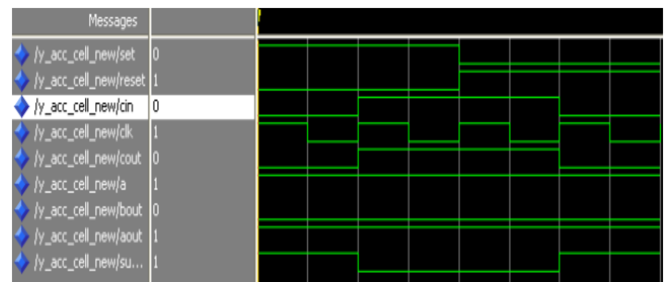

Fig 3. Weighted Pattern Generation

V. CONCLUSION.

In this paper generate the test pattern by using an accumulator based weighted pattern generation, as shown in Simulation results. Generate the weighted pattern method will detect the transition fault coverage and reduce the power consumption under the functional mode. The combinational circuits will be tested to detect the transition fault coverage and reduce the power consumption.

VI. FUTURE WORK.

Future work can be extended to all the types of sequential circuits with respect to the three weighted pattern. Functional mode also applied to the same sequential circuits still power taken by the generated test patterns can be reduced by using faster adders like carry lookahead adders.

VII. ACKNOWLEDGMENTS

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