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Design of Current Pulser for Electrochemical Based Semiconductor Device Processes

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Abstract - **A Current pulser with sharp rise and fall time has been developed for conducting electrochemical processes in the field of semiconductor device technology. Starting with the block diagram of the basic unit of the pulser, it has been designed and developed such that the rise and fall times are in the range of nanoseconds and the pulse width may vary in the ranges of 50-100 nS. A variable delay circuit is designed with the help of logic gates by using the property of propagation delay accumulation of logic gates in a circuit for having the facility of variable pulse width. A presettable counter has also been designed to count the number of pulses for controlled process of electrochemical etching and deposition.**

Keywords **– etching, propagation delay, pulser, variable delay**

I. Introduction

In recent years, centering on the aspects of high-speed driving, high-peak current pulse, miniaturization, high stabilization, many circuit modes have been developed, especially in high-peak current and narrow pulse. As of nowt, the pulse with low dithering, short rise time, nanosecond level and high-peak current can be obtained by using avalanche transistor [1–2], high power field effect transistor [3], high speed silicon controlled rectifier, and step recovery diode [4]. Narrow pulse may be achieved by using avalanche transistor, but single transistor cannot provide high-peak current. If several avalanche transistors are used in parallel connection, high-peak current may be achieved, but the time synchronization of switching process and equivalence distribution of current may be the problems. Otherwise, double peaks or bounce-back will appear in output pulse, and it is difficult to adjust the output pulse width continuously [5]. Though SCR can generate high-peak current pulse, pulse width almost cannot be adjusted in narrow ranges because it depends on SCR's discharging speed and storing energy capacitance. SRD can also generate narrow pulse, but the power is too low [6]. While power metal-oxide semiconductor field effect transistor belongs to the element of voltage controlling power, which has many traits such as high input impedance, low driving current, high voltage endurance, high-peak working current, high output power, perfect linearity of striding conductance, fast switching speed and without second breakdown phenomenon [7-9].

The wafer is fixed on a teflon holder with silver conducting paste. The etchant used here is a commercial platinum

solution based on sulphuric acid. The bath temperature is held constant at 40^0 C and a magnetic stirrer agitates the solution. The experimental setup is shown in fig. 1.

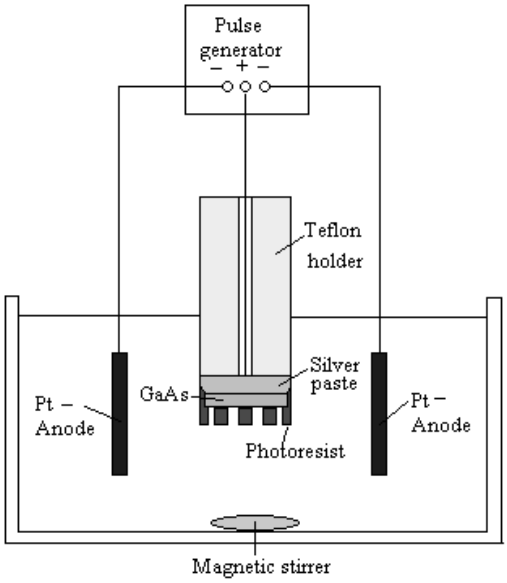

Figure 1: Experimental set-up

In contrast to GaAs etching using an anodization step, the pulse etching method requires no such additional surface treatment prior to etching. In this etching process, immediately after the wafer has come into contact with the platinum solution current pulses are applied. The long time between the single pulses is necessary to regenerate the platinum solution so that saturation effects are avoided.
The limekiln process is inherently difficult to operate efficiently because of complex dynamics and multi-variable process with and long time delays. It becomes hazardous and explosive in nature if it is operated beyond the set – point. The goals of limekiln automation includes improved lime quality, increased production, improved fuel efficiency, increased refractory life, improved kiln information gathering and processing.

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II. Design of Current Pulser

A square wave is received from the initial stable source i.e. crystal oscillator. The square wave is then fed to divide by N counter. Here we are using divide by 2 to get the desired PRF as 5KHz from a source of 10 KHz. The output is given to PLL with VCO for frequency synthesis. PLL helps in the reduction of jitter. The output from PLL is fed to the delay network.

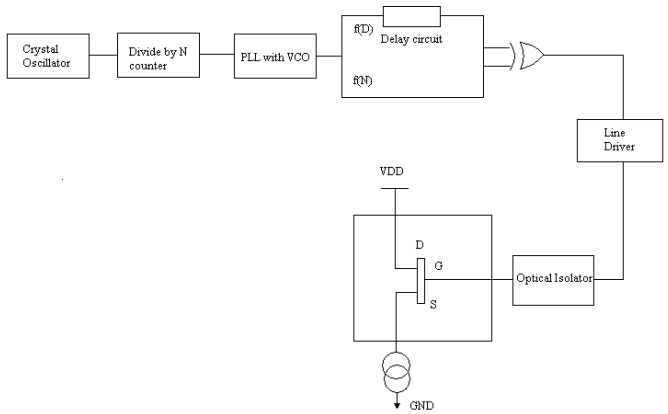

Figure 2: Block diagram of current pulser

In delay networks, the propagation delay of inverter gates is used and made variable by using analog switches. The gates are grouped in even numbers so that there is no phase inversion in the output of delay network. The delay of each device adds to the delay of every other device as the signal passes through several devices. Then the two waves, one from the output of PLL and other the delayed pulse are treated as two inputs for the Ex-or gate.

The narrow pulse thus obtained is given to the input of Line driver IC for decreasing the loading effect. The signal is then fed to the optocoupler for isolation with rest of the circuitry. Then the pulse width signal is given to the gate of the MOSFET to attain a high current pulse at the drain terminal of the MOSFET.

III. Design of Presettable Counter

To design the counter, first of all, the thumb wheel, which is one of the input of the presettable counter is set to the desired number of counts. The output of Presettable counter is given to one of the input of OR gate .The other input to the OR gate is the output of Power on Reset circuit, which allows the minimum required delay for the circuit to set up. The output from this OR gate is given to Reset input of S-R flip-flop. The Set input of the flip-flop is governed by manual set for its high or low logic status. Set input of flip-flop is made low manually. As the OR input has high logic if any of the input is high.

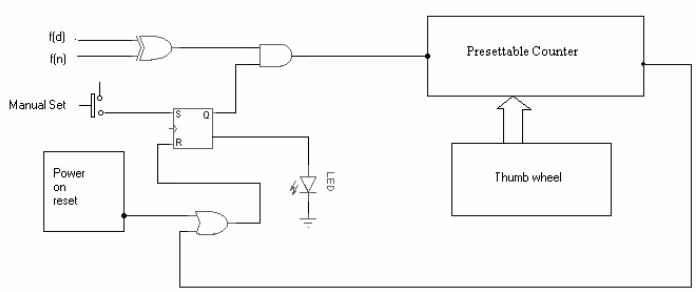

Figure 3: Block diagram of pulse counter

IV. Variable Delay Circuit Design

Since the delay of each device adds to the delay of every other device as the signal passes through several devices, the total delay can be significant in circuits that have critical timing. For designing the variable delay circuit the propagation delay of hex inverter is utilized. There is a single input and a single output. The inverters must be taken in even number to ensure no change in phase of the final output.

When the switches SW1 & SW2 are closed and rest of the switches are opened, the hex inverter gates G1 & G2 are responsible for the net delay. The total delay is then the sum of propagation delay of both the inverters. When SW1, SW3 and SW4 are closed and rest of the switches are opened, then the sum of propagation delay of all the four gates i.e. G1, G2, G3, G4 is the total delay. Similarly When SW1, SW3 and SW5 & SW6 are closed and rest of the switches are opened, then the sum of propagation delay of all the six gates i.e. G1, G2, G3, G4,G5 and G6 is the total delay and so forth so on.

In this way , variable even number of gates can be selected and their propagation delay can be utilized for the required variable delay .

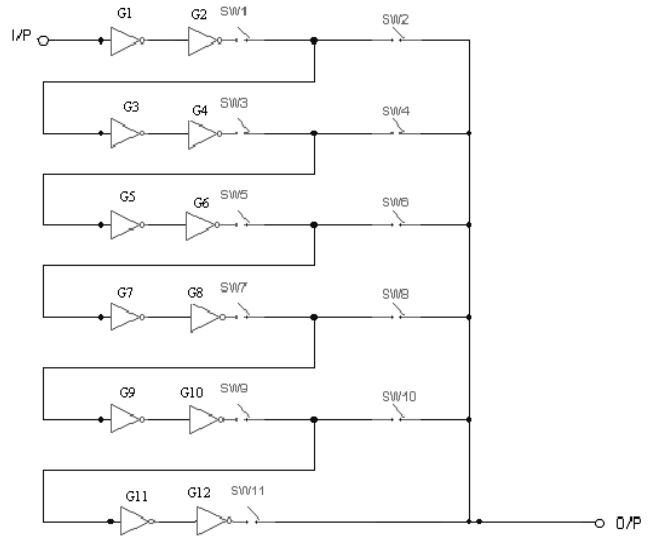

Figure 3 : Design of variable delay circuit

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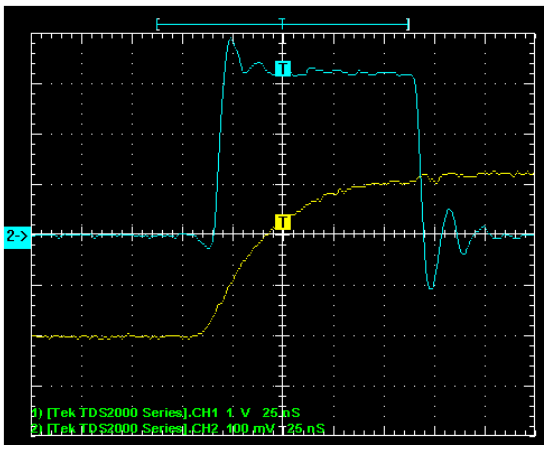

Fig. 4: Comparison between source output (yellow) and the output obtained after VIth hex- inverter IC (cyan).

V. Results and Discussion

Fig. 4 presents the comparison between crystal oscillator output and the effect of the accumulation delay of six hex-inverter ICs. Here the delay is about 100 micro seconds. This delay can be extracted in the form of a pulse with the help of delay circuit as small pulse width of 100 microseconds as shown in fig. 5.

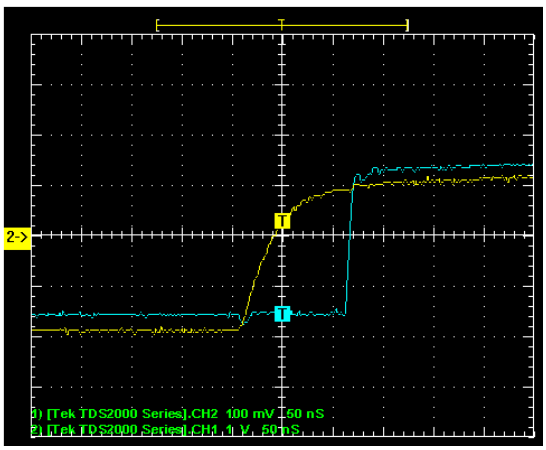

Fig. 5: Narrow pulse obtained at output of ex-or gate in the circuit

VI. Conclusion

The Current Pulser is designed and developed with sharp rise and fall time (in the range of nano seconds) alongwith required range of Pulse width i.e. 50 - 100 ns and required Pulse Rate Frequency of 5KHz. For having the variable pulse width, a variable delay circuit is designed and developed using the property of accumulation of propagation delay of the inverter gates in the circuit. Keeping under consideration, the application of the pulser in the controlled electrochemical processes at nano scale level, a presettable counter is also designed and

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