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Impact of scaling on wearout mechanism which affect CMOS reliability

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Abstract: This paper addresses the impact of physical miniaturization on CMOS reliability constraints. The focus will be mainly on four wearout mechanism namely Negative Bias Temperature Instability (NBTI), Time Dependent Dielectric Breakdown (TDDB), electromigration induced failure, hot carriers degradation The research inside recent ten years pointed out that the HCI, TDDB, and the NBTI are the three major wear-out effects on the CMOS integrated reliability for the long-term operation.

Keywords: CMOS; HCI; TDDB, NBTI, EM.

NOMENCLATURE

- **Negative Bias Temperature Instability** (NBTI*): The* threshold voltage of PMOS may shift when the gate terminal is subjected to negative potential at higher temperature.
- **Time Dependent Dielectric Breakdown** (TDDB)*:* Long time operation under high oxide field causes Time Dependent Dielectric Breakdown in MOS IC's, especially in those with large oxide areas such as DRAM
- **Electromigration Failure:** The increasing current densities in scaled interconnect and contacts initiates electromigration to produce open, short circuits or leakage problems.
- **Hot carrier Degradation:** The energetic hot electrons changes current/voltage characteristics of CMOS by trapping in the oxide layer near drain or entering the interface.

I. INTRODUCTION

The reliability of devices is defined as its ability to fulfill its intended function, under stated conditions for a stated period of time. Reliability associated failures in this case are caused by a failure mechanism This paper mainly focuses on major CMOS reliability constraints related to wafer process technology as they are critical to CMOS operation. This paper discusses the above technological reliability issues in detail, together with the impact of physical miniaturization on them. The paper further provides different measures to pacify them. The rest of the paper is organized as follow-Section II addresses the negative bias temperature bias instability, including the impact of scaling on it, and the major measures taken to prevent it. Section III to Section V in a similar way deal with 'time dependent dielectric breakdown', 'electromigration induced failure', 'hot carrier degradation' Finally, Section VI summarizes the paper.

II. NEGATIVE TEMPERATURE BIAS INSTABILITY (NBTI)

NBTI refers to the shift in the PMOS threshold voltage when the gate terminal is subjected to negative potential at elevated temperature for a prolonged period of time. The degradation is attributed to breaking of Si-H bonds at the Si/SiO_2 interface and the resultant diffusion of hydrogen species into the gate oxide. Unlike other degradation processes the NBTI is a self annealing process and the broken bonds recover when the applied potential is removed.

Among various NBTI degradation models presented in the literature, the Reaction Diffusion model (R-D model) illustrated in Fig.1 is consistent with experimental results. The model considers that negative potential applied at the gate produce interface traps N_{IT} at Si/SiO_2 interface. The electro-chemical reaction break Si-H bonds to produce hydrogen leaving behind an interface trapes . The released hydrogen species diffuse in the oxide layer toward gate electrode to increase threshold voltage. The R-D model is based on following two equations.

$$\frac{dN_{IT}}{dt} = k_f\left(N_o - N_{IT}(t)\right) - k_r N_{IT}(t) N_H o(t)$$

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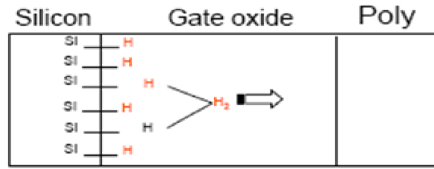

Inteface trap creation

$$\frac{N_{IT}}{dt} = D_H \frac{dN_H}{dx}$$

where N_o is the initial number of Si-H bonds, kf and k_r are forward and reverse reaction rates, $N_H{}^o$ is the concentration of hydrogen at Si/SiO_2 interface and D_H is the diffusion coefficient of hydrogen. Under normal conditions the forward and reverse reaction rates are much larger than the net interface generation rate N_{IT}. The trapes generated diffuse through oxide layer and effects the PMOS threshold voltage.

A. Impact of scaling

The aggressive scaling of oxide thickness without a corresponding reduction in the power supply voltage has increased oxide electric field significantly. For NBTI with H_2 diffusion the $N_H{}^o$, k_r and D_H in eq.1 are not affected by field variation as they are restricted to formation and diffusion of neutral hydrogen species. The field variation will only come through field dependent kf which can be written as :

$$k_f = k_o \times T \times p \times \sigma \times e^{-(E_{Fo} - \alpha E_{oz})/k_B T}$$

The forward reaction rate have three fold dependence on the electric field E_{ox}. Firstly the number of charges already present at the Si/SiO2 are p, and can be written as:

$$Q(p \times q) = C_{ox} \times (E_{ox})$$

$$p \propto E_{ox}$$

Secondly the charges generated tunnel inside the Si-H bond to approximately 1.5-2A depending on transmission co-efficient T. The transmission co-efficient depend exponentially on the electric field.

$$T \propto exp^{\gamma T^{E_{oz}}}$$

Finally the barrier potential E_{Fo} required to generate interface trap decrease by factor $a.E_{ox}$ with applied electric field. And most importantly thinner poly-silicon gate have brought the Si/SiO2 interface closer to the gate, so the hydrogen diffusion front reaches poly-interface within the stress phase and causes higher V_T shift.

B. Mitigation

Nitrogen presence near the oxide/substrate interface en-hances the NBTI degradation due to ease of hydrogen diffusion in nitrided oxide. The NBTI degradation decreases by adopting plasma nitridation instead of oxide nitrides . In plasma nitridation the nitrogen diffuses from oxide/gate end toward oxide/substrate interface. The decreasing nitrogen concentrations near the gate restrict hydrogen diffusion and improve NBTI immunity

Secondly the time power exponent n in threshold voltage shifts $AV_T = t^n$ have a range of values 0.25-0.30. The exponent variation is due to delay in measurement after removing stress and varying diffusion coefficient of hydrogen species in amorphous oxide. The hydrogen diffusion in amorphous oxide have a range of values due to variable hoping distances and timings. The interface trape generation rate in amorphous oxide is written as .

$$N_{IT} = \left(k_f N_o / k_r\right)^{1/2} (D_H t)^{n'}$$

and the diffusion coefficient of hydrogen in amorphous oxide is given by.

$$D_H = D_{Ho} (\omega t)^{n - \frac{\alpha}{4}}$$

where with a = 0.1 — 0.2, results in a lower power exponent range 0.225-0.20. The lowering of the power exponent suggest that NBTI performance can be improved by using more amorphous oxide with deeper trapping level and longer release time .

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III. TIME DEPENDENT DIELECTRIC BREAKDOWN (TDDB)

In TDDB the dielectric material isolating gate and substrate suffers from short circuit failure due to intense electric field applied across them . TDDB is a two step linked process consisting *wearout* and *thermal runway*. In the first step charge traps accumulate in bulk oxide and silicon/oxide interface, with the passage of time their density reaches to a critical value. The step is followed by sufficient local electric field and current that causes thermal runaway and melting of microscopic regions. Thus wear out is a global while runaway is a local phenomena.

The specific operative mechanism and the equations that define TDDB are still matter of controversy, however main TDDB models include the E-model, 1/E model and current dependent power law model. The E-model based on the thermo-chemical mechanism states that the TDDB follow field driven thermo-chemical breakage of Si-Si bond in SiO_2. The decomposition and hence time to fail has exponential dependence on the applied oxide field as follow:

$$MTFF = Aexp(-\gamma E)exp\left(\frac{E_a}{kT}\right)$$

where A is a constant, *7* is field acceleration parameter, E is oxide field, E_a is activation energy, k is Boltzmann constant and T is absolute temperature. The activation energy is linearly dependent on oxide field and the field acceleration parameter decrease with increasing temperature.

In daily reliability work the linear E-model is used and is fine upto oxide field of 4.8MV/cm, however the model ignore role of tunneling current and is un-adequate for ultra thin oxides .

The 1/E model states that the TDDB is a current driven mechanism caused by Fowler-Nordheim tunneling current and anode hole injection in SiO_2 layer. The model can be expressed as:

$$MTTF = Aexp\left(\frac{G}{E}\right)exp\left(\frac{E_\alpha}{kT}\right)$$

Where G is a constant. The model behaves well at higher stress values however ignores the thermal/diffusion that takes place in all material over time even in the absence of electric field.

Although voltage is the driving force for current but the leakage current also depend on oxide thickness, trap density, and defect generation rate. In order to include effects of all these parameters, a newly proposed model cover overall response of the system in the form of mean value of average leakage current I_{avg}. The model states that TDDB of thin gate oxide with thickness range of 1.7nm-6.8nm decreases inversely as power law rather than exponential of the mean value of the average leakage current during the constant voltage stress and selected temperature range as below:

$$MTTF = \frac{A}{I_{avg}^n} exp\left(\frac{E_\alpha}{kT}\right)$$

Where A is a constant and the value of exponent n increases from *1* to about *10* when oxide thickness reduces from 6.8nm-1.7nm. The power law prediction of TDDB reduction with scaling is in accordance with the percolation theory.

A. Impact of scaling

Historically the TDDB have received little reliability attention due to dielectric thickness and lower operating field. However MOS scaling increased the electric field E across the gate oxide films that reduces the TDDB activation energy Ea by following relation

$$E_\alpha = \Delta H_o - \alpha \times E$$

Where AH_0 is the enthalpy of activation and a is the effective dipole movement. Additionally under high electric field, frequent charges mobility increases oxide temperature that results in lower field acceleration parameter 7. The strong dependence of activation energy and acceleration parameter on oxide field reduces the TDDB with oxide scaling.

Additionally the TDDB dependence on oxide scaling comes from defects in oxide layer and tunneling currents flowing through it. The TDDB relation to them is given by.

$$TDDf = \frac{N_{BD}}{kJ}$$

Where N_{BD} is the number of defects needed for dielectric to breakdown, k is a constant and J is the tunneling current through oxide layer. percolation model states the breakdown only occur if a connecting path is

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formed across the gate oxide. The formation of such a path is a function of defect density and oxide thickness. For a given defect density the path formation is more likely for thinner oxides thus reducing TDDB.
Direct tunneling current starts for ultra thin oxide below 4nm and increase by one order of magnitude for every 0.2-0.3nm reduction in oxide thickness. Additionally at very low oxide thickness the electronic wave function of silicon conduction band may become large enough to reduce the tunneling barrier.

B. Mitigation

Introduction of high k dielectric minimize the unacceptable leakage current in the oxide layer. Silicon nitride have a dielectric strength is about 10 MV/cm and is alternative for silicon dioxide layer. The Silicon nitride at SiO2/ poly interface minimizes defect generation by restricting boron penetration from highly doped gate material and have excellent thermal compatibility with Si substrate.

Zirconium and Hafnium silicate ($ZrSi_xO_y$ and $HfSi_xO_y$) with 3-8% of Hf or 2-5% Zr are suitable for replacing SiO_2 in future ultra scaled gate oxide. The silicates have higher dielectric constant, lower leakage current and are stable in direct contact with the Si . The modification is achieved by adding Zr and Hf to the SiO2 and then following the rest of the CMOS processing procedure.

IV. ELECTROMIGRATION INDUCED FAILURE

The electromigration is characterized by metal ion drift in an interconnect with high current density. The high energy electrons force metal ions to move in their own direction mainly due to momentum exchange. The material flux Cause voids formation at their previous

Positions and protrusions at the collection points. As a result short and open circuit faults are produced the interconnects as shown on the fig 3.

For CMOS devices the material migration is more obvious at the silicon interconnect junction. The effective drift velocity of material flux derived in *Blench Model* is given as

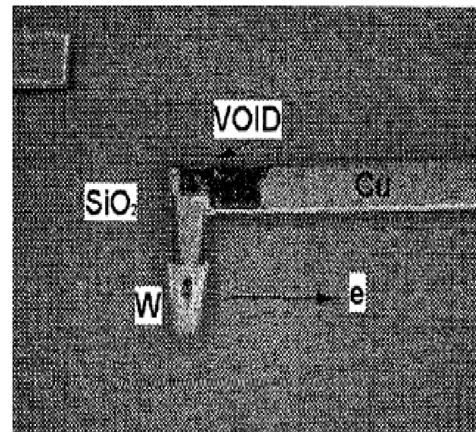

Fig. 3. Electromigration damaged 0.28μm wide line. Arrow show the electron direction

$$v_d = \frac{J}{n} = \frac{D_{eff}}{kT}\left[ej\rho Z_{eff} - \Omega\frac{\Delta\sigma}{\Delta x}\right]$$

density, D_eff is the effective diffusion coefficient, k is the Boltzmann's contant, T is the absolute temperature, $Zeff$ is the effective charge number, e is the absolute value of electron charge, j is the current flowing, p is the metallic resistivity, a is the atomic volume and ^ is the electromigration induced stress gradient along the length of the interconnect.

A. Impact of scaling

The increasing chip density and growing performance have increased the current density in scaled interconnects. Eq.14 shows that atomic flux J in narrow interconnect increase with increasing current density j at constant temperature. Additionally the line width dependence of the material migration comes from diffusion constant D_eff. The D_eff is a sum of diffusion in bulk, grain boundary and line width at the interface.

$$D_{eff} = n_b D_b + \left(\frac{\delta_{gb}}{d}\right)\left(1-\frac{d}{w}\right)D_{gb} + \delta_i\left[\frac{2}{w}+\frac{1}{h}\right]$$

where n_b is the fraction of atoms in the bulk, S_{gb} is the effective thickness of the grain boundaries, d is the grain size and S_i is the effective conductor width at the

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interface. The smaller grain sizes in scaled lines results in higher diffusions and current density. The higher diffusion rate increases the drift velocity that causes a decrease in the MTTF.

For the worst case of non-scaled voltage the decreasing line width result in increasing current density exponentially, and from Black's equation the lifetime dependency on current density j is written as

$$MTFF = \frac{A}{j^n}.exp\frac{E_\alpha}{k.T}$$

B. Mitigation

The electomigration is due to push of electrons in high current density interconnects. By keeping the current density below the maximum allowed density number of electrons colliding metal ions decrease thus the problem of electromigration is alleviated.

Increasing copper concentration in Al (Cu) lines can alleviate the material migration issue. For interconnect with smaller line width the activation energy of Cu is nearly equal (about 1eV) to Al (Cu) but the absolute lifetime of Cu lines is about 50 *x* that of Al(Cu) interconnects. The MTTF improvement is due to the higher resistivity to electromigration and higher melting point. Furthermore good selection and deposition of the passivation over the metal interconnect reduces the electromigration damage by limiting extrusion and suppressing surface diffusion.

The material flux depends on the length of the line that allows electromigration to occur. Any line shorter than *Blench length* will not suffer from electromigration. The improvement in electromigration resistivity is due to reversed mechanical stress buildup. the stress cause a reverse migration process to compensate the material flux . To avoid the electromigration in line the product of wire current and wire length must be smaller than process technology dependent threshold value $(JI)_{th}$.

V. HOT CARRIERS DEGRADATION

Hot carriers are energetic electrons and holes in the channel and pinch off region of a transistor that effect transistor on state and off state currents. Initially the carriers gain enough kinetic energy in excess of thermal energy to enter substrate region. If they continue to gain more energy (3.2-3.8 eV) they are injected into the oxide layer. The substrate current produce impact ionization and finally CMOS latchup while the carriers injected to oxide layer lead to the formation of oxide states and trapped oxide charges.

The well known hot carrier degradation model is Lucky electron model. According to the model the Lucky electron gain sufficient energy from the field to become hot and their momentum is directed toward oxide. The electrons moves away from channel that results in a reduced MOSFET on state current and higher off state current

A. Impact of scaling

The hot carrier degradation strongly depends on the channel length at constant supply voltage

$$MTFF = A \times \left(L_{eff}\right)$$

Where A is a constant and L_{eff} is the channel length. The channel length depency can be derived from modification in Lucky electron model. According to Lucky electron model for a given values of pinch off potential V_{dsat}, drain potential $V_{ds} - V_{dsat}$ and gate thickness the impact ionization rate a is given by:

$$\alpha = \frac{i_{sub}}{I_d} = exp[-1/(V_{ds} - V_{dsat})]$$

the model argue that a is independent of gate length at constant $-l/(V_d - V_{dsat})$. However it is found that a increases with scaling the gate length to sub-microne level because the carriers gain energy from drain field as well as channel electric field i-e electric field between source edge and pinch off region [23]. The drain field is independent of channel length but channel electric field E_{ch} increases with decrease in channel effective length L_{eff} by following the relation.

$$E_{ch} = (V_{dsat} - V_s)/L_{eff}$$

The channel electric field increases the electron velocity in the channel. The increase in carrier velocity enhances temperature distribution in the channel and the pinch-off regions that increases the impact ionization rate both in NMOS and PMOS by following equation.

$$\alpha = exp(-\pi/kT)$$

Additionally the drain field increase with scaling the gate oxide thickness by following eq

$$E_m = (V_d - V_{dsat})/l = (V_d - V_{dsat})/\left(0.22T_{ox}^{1/3}x_j^{1/2}\right)$$

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Where Xj is the drain pn junction depth and T_{ox} is the oxide thickness. The hot carrier reliability of scaled CMOS degrades even at supply voltage of $V_d = 1.0V$ due to higher drain field the impact ionization rate dependence on oxide thickness and gate length at peak substrate current and constant V_d-$V_{dsat.}$

B. Mitigation

The lateral field along the channel E_{ch} decreases by introduction of a Lightly Doped Drain *LDD* region which make use of a lightly doped region (n~) between the channel and the drain n+ region . However voltage drop in the LDD lateral resistance degrade current reliability. In order to minimize the side effects modified LDD structures such as Inverse-T gate LDD *ITLDD,* Large Tilt Angle Implant Drain *LATID* and Buried LDD can be efficiently used.

The hot carrier reliability significantly improves by lowering the power supply voltage in accordance with V_{dsat}. For halving the channel length the V_{dsat} may only to be reduced by less than 0.5V in future MOSFETs so V_{cc} reduction of 0.5V will guarantee hot carriers reliability.

VI. CONCLUSION

In this paper we have discussed that aggressive miniaturization of CMOS will cause higher sensitivity to defects. The ultra scaling of gate oxide will increase field intensity that will enhance NBTI and TDDB issues. plasma nitridation and use of amorphous oxide decreases the NBTI and the introduction of Zr or Hf silicate minimize the TDDB. The use of Cu in the Cu(Al) and optimizing gate length mitigates the open and short faults due to electromigration in the shrinking lines. The use of LDD and modified LDD structures reduce the hot carrier's impact ionization rate and oxide trape generation in scaled CMOS. Finally highly pure material, annealing and proper shielding minimize the soft errors. The above scaling constraints and their solutions reveal that inspire of aggressive downsizing the CMOS reliability constraints are manageable even MOSFET gate length is be scaled to the atomic limits . The advent of new technology and improvement in the architecture design and process development will enhance CMOS performance even at gate length of 10-20nm. The current silicon CMOS is the most successful 'nano device' and no realistic replacement of the silicon devices could be thought even if the scaling reaches to the downsize limits.

REFERENCES

[1] ITRS, "The International Roadmap for Semiconductor (ITRS) 2007", http://www.itrs.net/Links/2007ITRS/Execsum2007.pdf.

[2] M.Alam and S.Mahapatra, "A comprehensive model of PMOS NBTI degradation", Microelectronics Reliability, vol.45, pp. 71-81, 2005.

[3] A. E. Islam, H. Kufluoglo, D. Varghese, S. Mahapatra, and M. A. Alam, "Recent Issues in Negative-Bias Temperature Instability: Initial Degradation, Field Dependence of Interface Trape Generation, hole Trapping Effects, and Relaxation", IEEE Transaction on Electronic Devices, vol. 54, no.9, 2007.

[4] Dieter K. Schroder, "Negative Bias Temperature Instability: What do we understand?", Microelectronics reliability, vol.47, issue 6, pp. 841-852, 2007.

[5] Hau-Riege, Ch.S, "An Introduction to Cu Electromigration", Microelectronic Reliability, vol 44, pp. 195-205, 2004..

[6] F. Chen, R. P. Vollertsen, B. Li, D. Harmon and W. L. Lai, "A new empirical extrapolation method for time dependent dielectric breakdown reliability projection of thin SiO2 and nitrided oxide dielectric.", Microelectronics Reliability, vol. 42, pp. 335-341, 2002.

[7] Sharma, Rajnish; Kumar, Ashok; Anthony, John. "Advances in high k dielectric gate material for future ULSI devices", JOM, Vol. 53, pp.53-55(3),June 2001

[8] G. L. Rosa and S. E. Rauch III, Channel hot carrier effect in n-MOSFET devices of advanced submicron CMOS technologies, Microelectronics Reliability, pp. 552-558, 2007.

[9] J.M. Rafi and F. Campabadal "Hot carrier degradation in deep submi-crometer nMOSFETs: lightly doped drain vs. large angle tilt implanted derain" Journal of Solid State Electronics, vol.45, pp. 1391-1401 (2001).

[10] K.OJeppson and C. M Svesson, "Negative bias stress of MOS devices at higher eletric fields and degradation of MOS devices", *Journal of Applied Physics,* vol. 48, pp. 2004-2014, 1977.

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