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Optimization And Performance Analysis Of A Low-Voltage High Speed CMOS Double -Tail Comparator

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Abstract:-**In recent years, there has been an increasing demand for high-speed digital circuits at low power consumption. The need for ultra-low-power, area efficient, andhigh speed analog-to-digital converters is pushing toward theuse of dynamic regenerative comparators to maximize speed andpower efficiency. In this paper, an analysis on the delay of thedynamic comparators will be presented and analytical expressionsare derived. From the analytical expressions, designers canobtain an intuition about the main contributors to the comparatordelay and fully explore the tradeoffs in dynamic comparatordesign. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional doubletail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the designand by adding few transistors, the positive feedback duringthe regeneration is strengthened, which results in remarkablyreduced delay time. Post-layout simulation results in a 0.18-μmCMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clockfrequency of the proposed comparator is 500 MHz at supply voltages of 0.8 V, while consuming 141.91μW.**

Keywords:-DOUBLE-TAIL COMPARATOR, DYNAMIC CLOCKEDCOMPARATOR, HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS (ADCS), LOW-POWER ANALOG DESIGN.

I. INTRODUCTION

In electronics field, acomparatoris a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals $V_+$and $V_-$and one binary digital output V_0 . The output is ideally

$$V_0 = \begin{cases} 1, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases}$$

A comparator consists of specialized high-gaindifferential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters (ADCs)

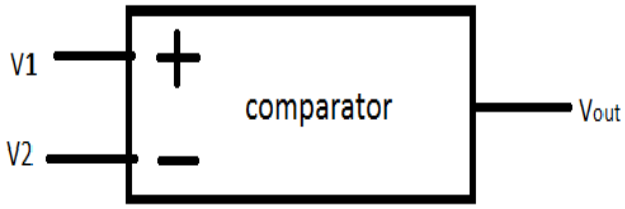

Fig 1. Schematic of basic comparator

The comparator is basically compare the two voltage or current signal. In the figure 1. shows that basic operation of the comparator, In this apply the two voltage signal (V_+andV_-) at the inputs .The comparator compare these two inputs with each other and gives output with respect to which one has higher potential. The output of the comparator isalways in the digital form or binary form, 1 or 0.

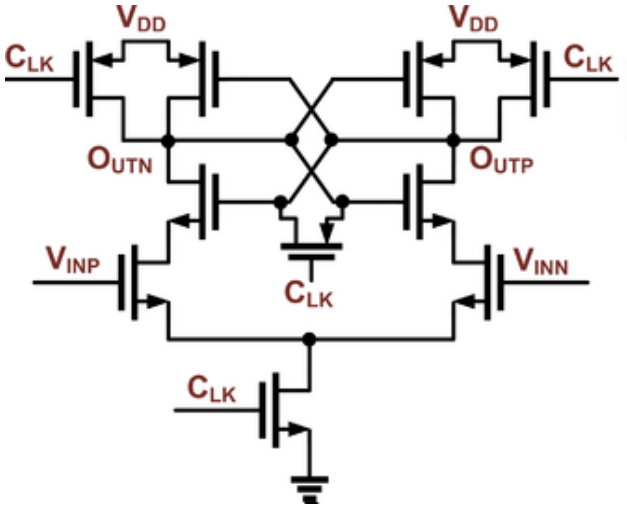

Fig 2.Latched dynamic comparator

A part from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. Additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. Despite the effectiveness of this approach, the effect of component

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mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator proposed in this research work is based on designing a separate input and cross-coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. A comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in, a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. By adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

1.2Differential voltage

The differential voltages must stay within the limits specified by the manufacturer. High-speed comparators differential voltage ranges substantially lower than the power supply voltages (±15 V vs. 36 V). Rail-to-rail comparators allow any differential voltages within the power supply range. When powered from a bipolar (dual rail) supply Specific rail-to-rail comparators with p-n-p input transistors allow input potential to drop 0.3 volts below the negative supply rail, but do not allow it to rise above the positive rail. Specific ultra-fast comparators allow input signal to swing below the negative rail and above the positive rail, although by a narrow margin of only 0.2 V. Differential input voltage (the voltage between two inputs) of a modern rail-to-rail comparator is usually limited only by the full swing of power supply.

1.3Power reduction in comparator circuits

It is not only the delay parameter which is improved in the modified proposed comparator, but the energy per conversion is reduced as well. In conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the *V*DD. However, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required. This can be seen when being compared with conventional topologies

1.4Kickback noise

Principally in latched comparators, the large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of thecomparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which maydegrade the accuracy of the converter. This disturbance isusually called “kickback noise. It has been shown that the fastest and most power efficient comparators generate more kickback noise. Although it improves the double-tail topology in terms of operation speed and thus energy per comparison, the kickback noise is increased in comparison to conventional double-tail structure. The peak disturbance as a function of differential input voltage of the comparator in three studied architectures. While double tail structure takes advantage of input-output isolation and thus the minimum kickback noise, the conventional dynamic comparator and our proposed structure has nearly similar kickback noise. However, in our proposed comparator since control transistors are not supposed to be as strong as the latch transistors in conventional dynamic comparator, it is possible to determine the size of those transistors in a way that keeps the advantages of the speed enhancement and power reduction, while reducing kickback noise.

1.5Clocked regenerative comparators

Clocked regenerative comparators have found wide applicationsin many high-speed ADCs since they can make fast decisions due to the strong positive feedback in there generative latch. Recently, many comprehensive analyses have been presented, which investigate the performance ofthese comparators from different aspects, such as noise, offset and random decision errors, and kick-back noise. In this section, a comprehensive delay analysis is presented; the delay time of two common structures,i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

1.6Need for double tail comparator

- To maximize sampling frequency
- For fast operation even at small supply voltages
- It compare the two voltage or current signal
- It reduce the power consumption and delay time
- It reduce the offset voltage

1.7Applicationsof comparator:-

Comparator are widely used in

- It is used for analog to digital conversion
- Comparator is used for compare the two voltage or current signal
- It is used in memory sensing circuits
- Comparator is also used as data receivers

I PROPOSED WORK

The schematics of different blocks of comparator design are designed on the TANNER tool by using 180nm technology.

1.8Conventional dynamic comparator

The schematic diagram of the conventional dynamic comparatorwidely used in A/D converters, with high input impedance, rail-to-rail output swing, and no staticpower consumption is shown in Fig. 3

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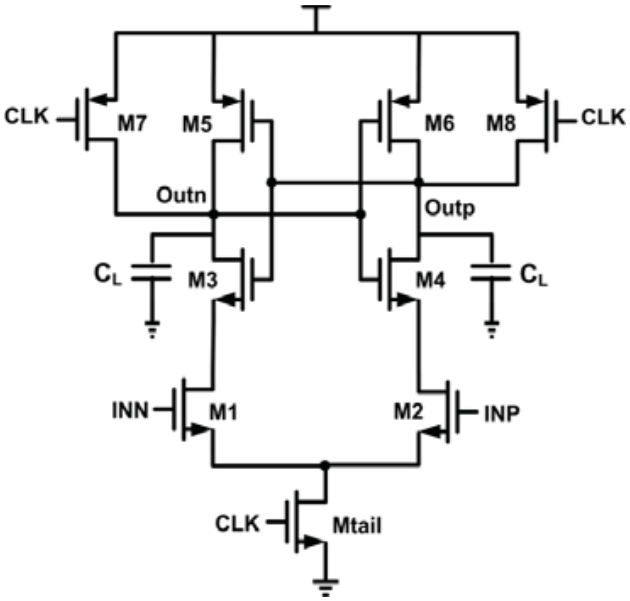

Fig. 3. Schematic diagram of the CMOS conventional dynamic comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig.1. The operation of the comparator is as follows. During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Outnand Outpto VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 andM8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp(discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn(discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5) and M4, M6). Thus, Outnpulls to VDD and Outpdischarges to ground. If VINP < VINN, the circuits works vice versa.

II SIMULATION RESULTS

Double tail comparator designs based on low power and high speed techniques and simulated in TANNER tool. All the results are obtained in 180nm CMOS process technology.

1.9 Simulation waveforms of the dynamic comparator designs

The v(fp) and v(fn) are the input V_{DD} of comparator and v(outp), v(outn) are the output of comparator. Where the v(clk) indicate to the reset(clk = 0) and set(clk =1) set the phase. Thesimulation waveforms of comparator is shown in Figure 4.

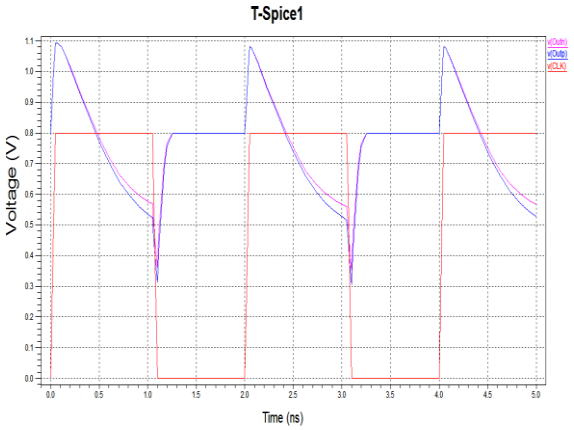

Fig. 4. Output waveforms of CMOS conventional dynamic comparator

2.0Simulation propagation delay for high to low transition

From Figure 5. It is clear that as input inp is more positive than inn, so output ‘outp’ will discharge faster than ‘outn.’ The propagation delay for high to low transition (t_{pHL}) is calculated from difference between 50% value of CLK and the 50% value of Output Outp.

t_{pHL}=1.07ns-0.030=1.04ns

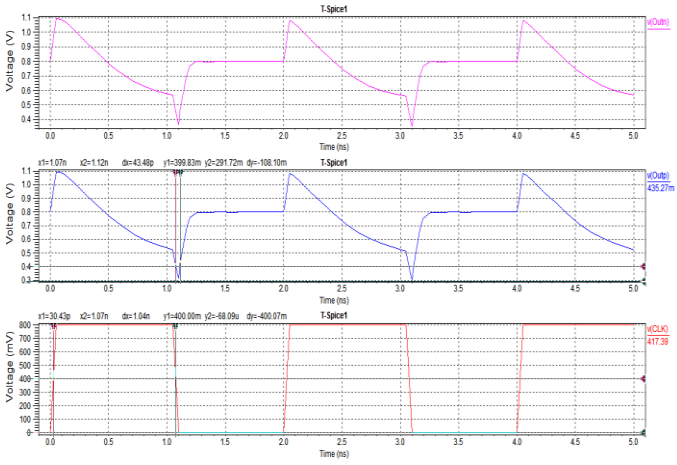

Fig. 5. Waveform shows output Outp, Outn and clk when inp is 5mV more than inn

2.1 Simulation propagation delay for low to high transition

it is clear that as input inp is more positive than inn, so output outp will discharge faster than outn. The propagation delay for low to high transition (t_{pLH}) is calculated from 50% value of CLK and the 50% value of Output Outp.

t_{pLH} =1.08ns -1.07ns=0.01ns

Total propagation delay
(t_{PD})= (t_{pHL}+ t_{pLH})/2= (1.04+0.01)/2= 1.04/2=0.525ns

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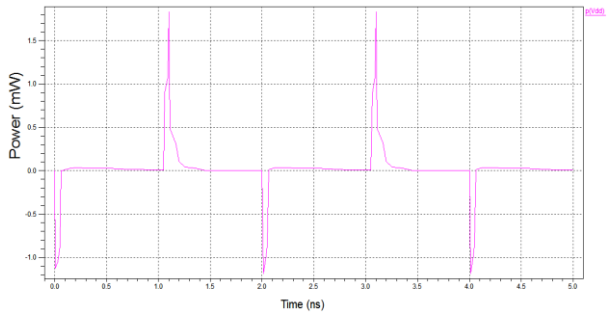

Fig. 6. Power Consumption result of CMOS conventional dynamic comparator

Power Results

Power Results

Vdd from time 1e-010 to 1.2e-008

Average power consumed -> 2.662130e-005 watts

Max power 2.032697e-003 at time 3.1e-009

Min power 7.515019e-007 at time 3.69545e-009

2.2 Conventional double-tail dynamic comparator

A conventional double-tail comparator is shown in Fig.7. This topology has less stacking and therefore can operate at same supply voltages compared to the conventional dynamic comparator. But the power consumption is less and having high speed than conventional comparator

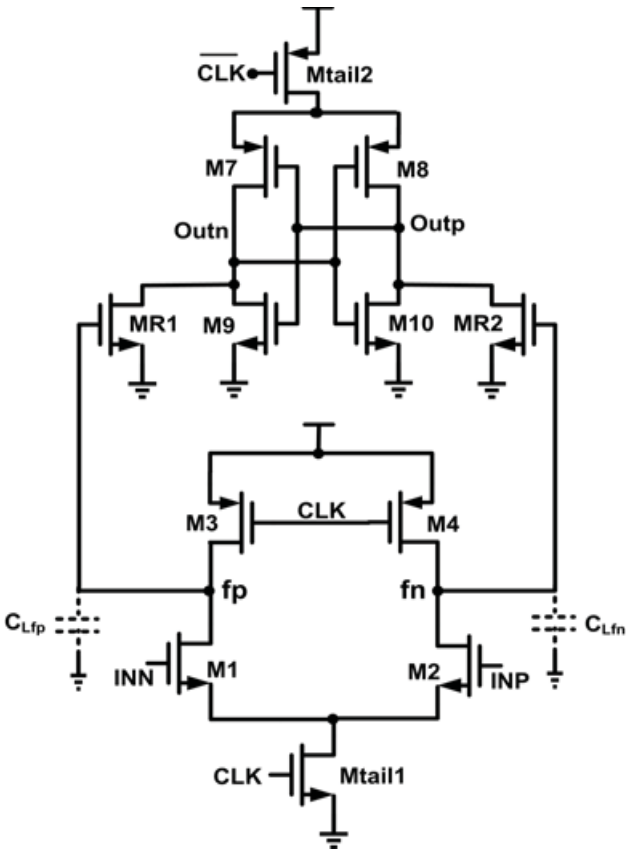

Figure. 7. Schematic diagram of the CMOS double-tail dynamic comparator

A conventional double-tail comparator is shown in Fig.7. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset. The operation of this comparator is as follows. During reset phase (CLK = 0, Mtail1, and Mtail2 are off),transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK =VDD, $Mtail_1$ and $Mtail_2$ turn on), M_3-M_4 turn off and voltages at nodes fn and fp start to drop with the rate defined by Mtail1/Cfn(p) and on top of this, an input-dependent differential voltage Vfn(p) will build up. The intermediate stage formed by MR_1 and MR_2 passes Vfn(p) to the crosscoupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise

III SIMULATION RESULTS

Double tail comparator designs based on low power and high speed techniques and simulated in TANNER tool. All the results are obtained in 180nm CMOS process technology.

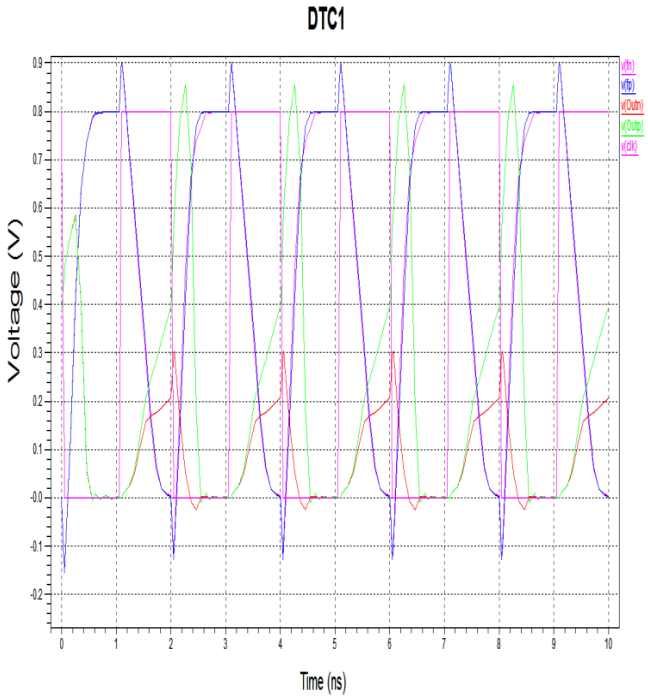

Fig. 8. Output waveforms of CMOS double-tail dynamic comparator

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2.3 Simulation waveforms of the double tail dynamic comparator designs

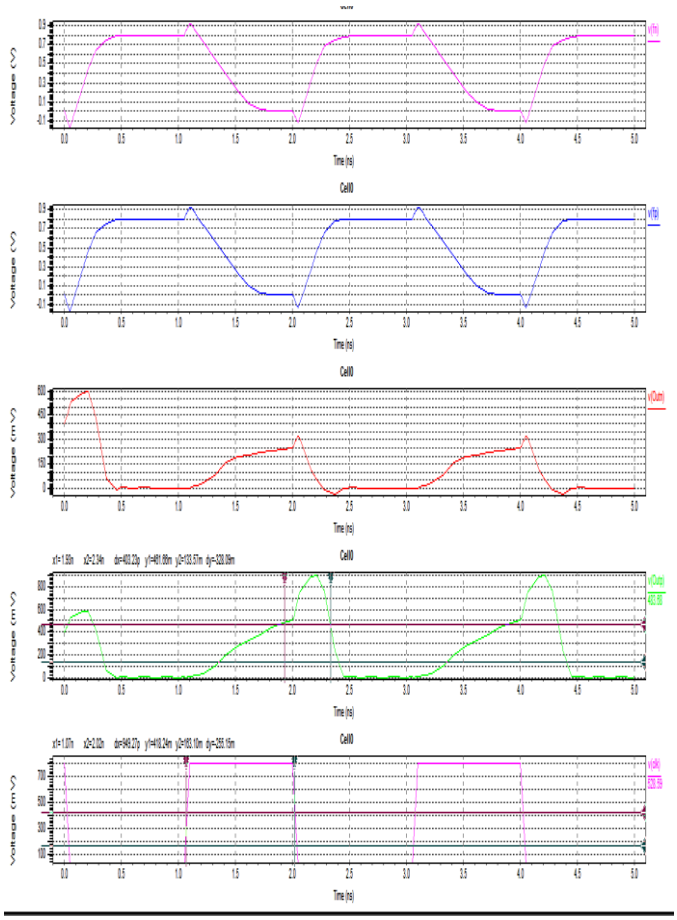

Fig. 9: Waveform shows output Outp, Outn and clk when inp is 5mV more than inn

2.4 Simulation propagation delay for low to high transition

From Figure 9, it is clear that as input inp is more positive than inn, so output outp will charge faster than outn. The propagation delay for low to high transition (t_{pLH}) is calculated from difference between 50% value of CLK and the 50% value of Output Outp.

t_{pLH}= 1.93ns-1.07ns=0.86ns

2.5Simulation propagation delay for high to low transition

Similarly, the propagation delay for high to low transition (t_{pHL}) is calculated from difference between 50% value of CLK and the 50% value of Output Outp.

t_{pHL}= 2.35ns-2.02ns=0.33ns.

Total propagation delay

(t_{PD})=(t_{pHL}+t_{pLH})/2=(0.33+0.86)/2= 1.19/2=0.59ns

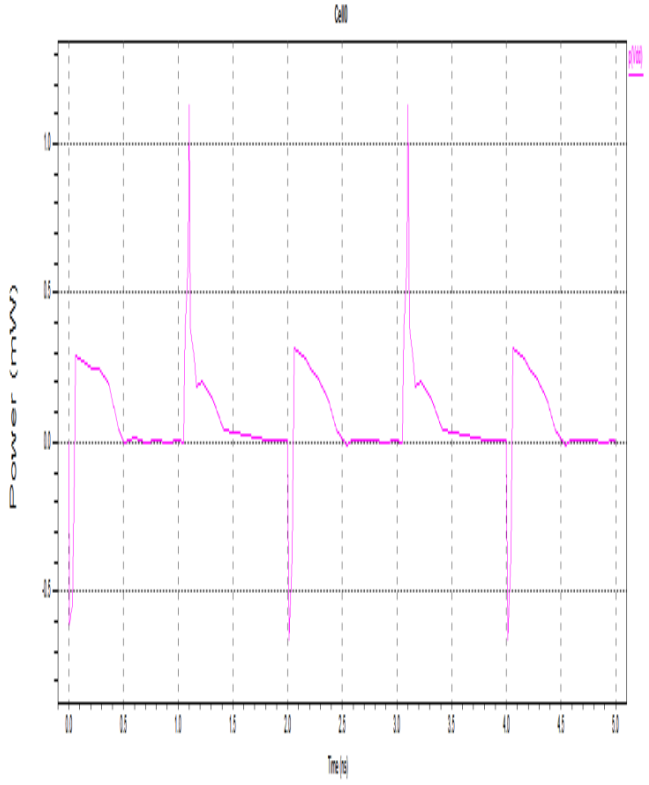

Fig.10. Power Consumption result of CMOS double-tail dynamic comparator

Power Results

Vdd from time 5e-011 to 5e-009

Average power consumed -> 8.465283e-005 watts

Max power 1.128760e-003 at time 3.1e-009

Min power 8.133613e-007 at time 9.01658e-010

2.6 Proposed double-tail dynamic comparator

The schematic diagram of the proposed dynamic double-tail comparator shown in fig 11. Due to the better performance of double-tail architecture in low-voltage applications, theproposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase V_{fn} and V_{fp} in order to increase the latch regeneration speed. For this purpose, two control transistors have been added to the first stage in a cross-coupled manner. The performance of the proposed double tail comparator is better than as compare to conventional double tail comparator. The proposed double tail comparator has high speed and consumes the less power

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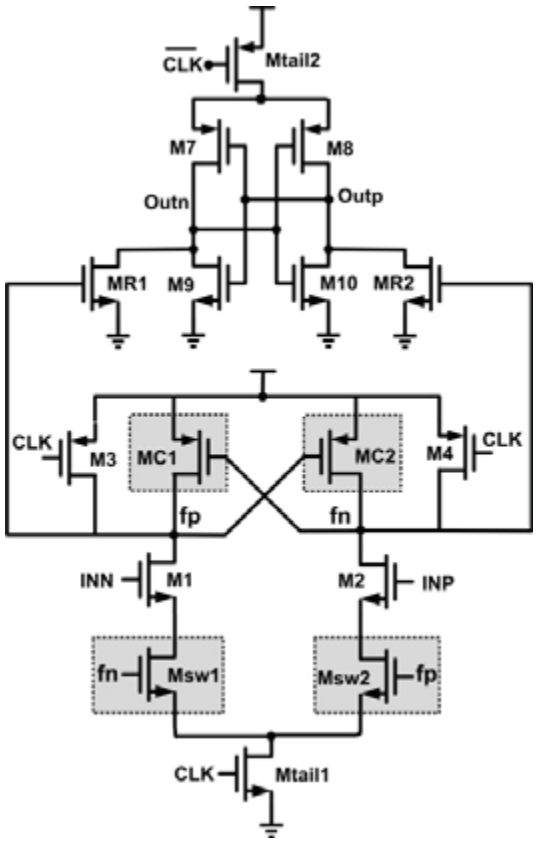

Fig. 11: Schematic diagram of the proposed CMOS double-tail comparator

The operation of the proposed comparator is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which Vfn/fp is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (M_{c1}) turns on, pulling the other node fp back to the V_{DD}. Therefore by the time passing, the difference between fn and fp ($V_{fn/fp}$) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea,one of the points which should be considered is that in thiscircuit, when one of the control transistors (e.g., M_{c1}) turns on, a current from V_{DD} is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [Msw1 and Msw2, as shown in Fig.11. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD. (during the reset phase), both switches are closed and fn andfp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

IV SIMULATION RESULTS

Double tail comparator designs based on low power and high speed techniques and simulated in TANNER tool. All the results are obtained in 180nm CMOS process technology.

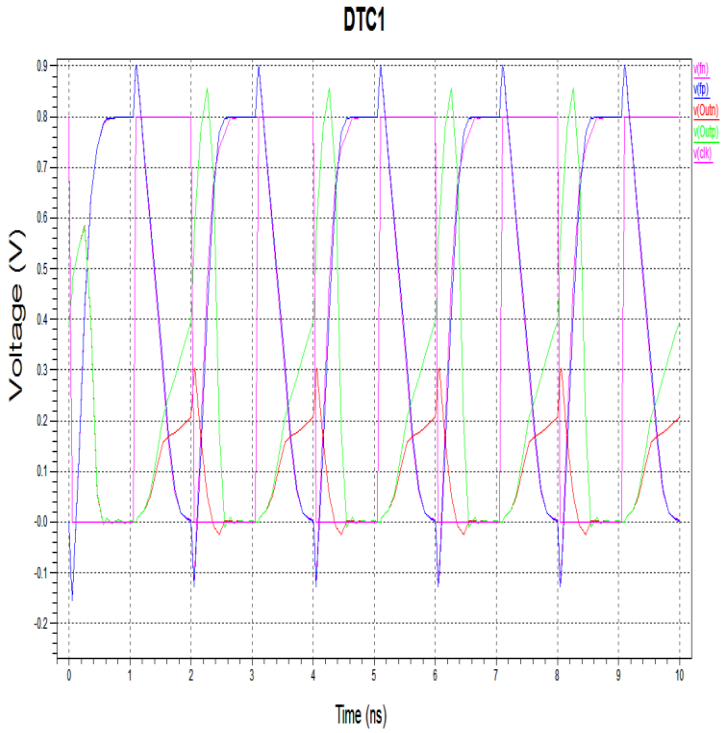

Fig. 12 Output waveforms of proposed CMOS double-tail dynamic comparator

2.7 Simulation propagation delay for low to high transition

From Figure 12, it is clear that as input inp is more positive than inn, so output outp will charge faster than outn. The propagation delay for low to high transition (t_{pLH}) is calculated from difference between 50% value of CLK and the 50% value of Output Outp.

t_{pLH}=412.44ps-26.01ps=386.43ps=0.386ns.

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2.8 Simulation propagation delay for high to low transition

The propagation delay for high to low transition (t_{pHL}) is calculated from difference between 50% value of CLK and the 50% value of Output Outp.
t_{pHL}=1.22ns-1.08ns=0.14ns

Total propagation delay

$(t_{PD})= (t_{pHL}+ t_{pLH})/2= (0.14+0.386)/2= 0.263$ns

2.9 Simulation waveforms of the double tail dynamic comparator designs

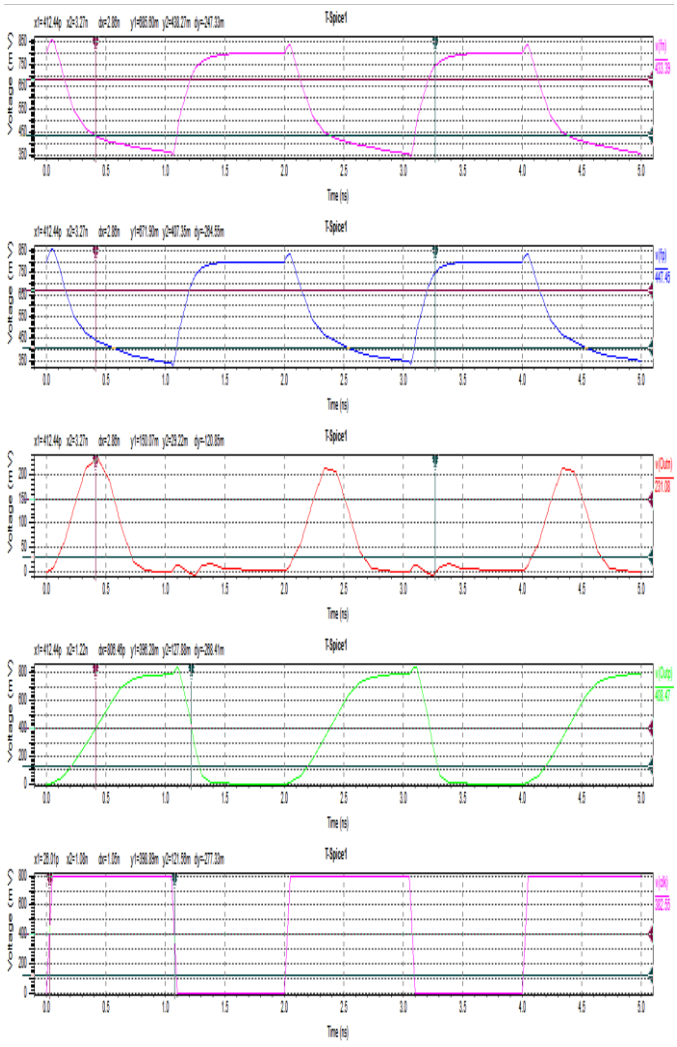

Fig. 13: Waveform shows output Outp, Outn and clk when inp is 5mV more than inn.

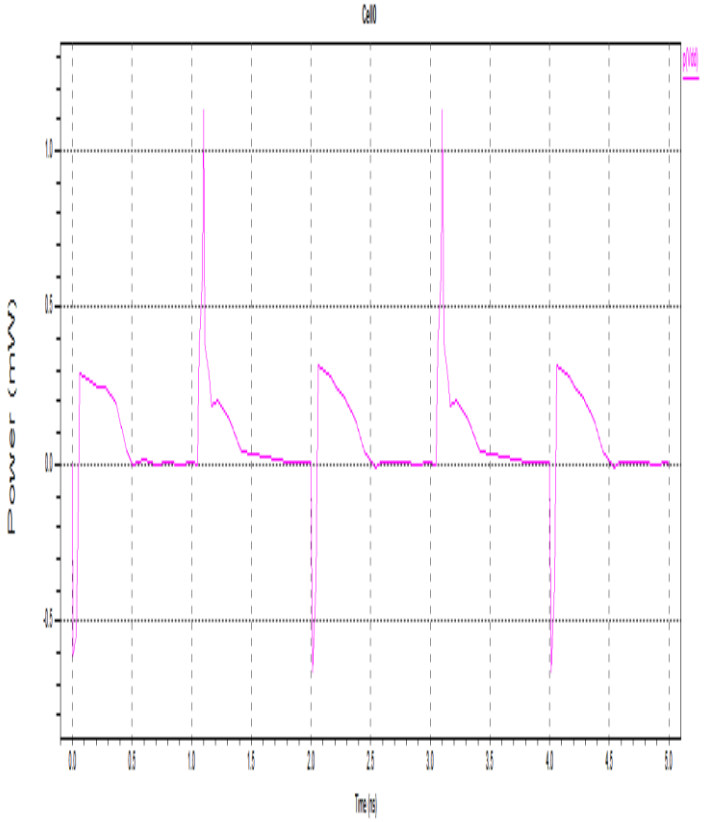

Fig. 14: Power Consumption result of proposedCMOS double tail comparator

Power Results

Power Results
Vdd from time 5e-011 to 5e-009
Average power consumed -> 1.419180e-004 watts
Max power 1.341023e-003 at time 5e-011
Min power 1.232521e-005 at time 4e-009

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Table 1: Comparison of designed dynamic comparators

Comparator Structure	Conventional Dynamic Comparator	Double-tail dynamic Comparator	Modified low power double tail dynamic comparator
CMOS Technology	180nm	180nm	180nm
Supply Voltage	0.8V	0.8V	0.8V
Propagation Delay	0.525ns	0.59ns	0.263ns
Average Powerdissipation	266.21 µW	846.52 µW	141.91µW
Energy per conversion (J)	0.072p	0.053p	0.038p
Frequency used per conversion	500MHZ	500MHZ	500MHZ

V. CONCLUSION & FUTURE WORK

3.0Conclusion

The need for high speed low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic comparators to maximize speed and power efficiency. In this thesis work, I presented the design and analysis of three CMOS dynamic comparators at 180nm technology node. From the analysis of designed CMOS conventional dynamic comparator, Double tail dynamic comparator and modified high speed double tail comparator; designers can obtain an intuition about the main contributors to the comparator propagation delay and power consumption. Based on the presented analysis, a new modified high speed CMOS dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for fast operation. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Optimum transistor sizing plays very important role in determine the overall propagation delay and average power dissipation for all the dynamic comparators. It is shown that in the modified dynamic comparator delay time is significantly reduced. The propagation delay for conventional dynamic comparator is 0.525ns at supply voltages of 0.8V and clock frequency of 500MHz while consuming 266.25µW while for double dynamic comparator propagation delay is 0.59ns and power consumption is 846.52 µW. The propagation delay for modified high speed comparator is 0.263ns while consuming only 141.91µW. So, modified high speed double tail dynamic comparator has significant improvement in propagation delay and power consumption.

3.1Future Scope

New circuit topologies can be devised for further improving the speed and power consumption. I have input referred output voltage and energy per conversion. The designed circuits can be further optimized by generating the optimized layouts, focussed only at minimizing propagation delay, in future analysis the more parameters can be included like kickback noise voltage.

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