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Lowpower CAM for ATM switch with improved VPI/VCI translation

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***Abstract*— CAM provide highspeed search function in one clock cycle.We proposed an Asynchronous Transfer Mode Switch by using high speed low power CAM.CAMs can be used in Asynchronous Transfer Mode (ATM) switching network components as a translation table. Since ATM networks are connection-oriented, be set up across them prior to any data transfer. There are two kinds of ATM virtual circuits: Virtual Path (identified by a virtual path identifier or VPI) and Channel Path (identified by a channel path identifier or VCI). Parity bit and an effective gated power techniques allocates less power to match decisions involving a larger number of mismatched bits.These scheme results in a significant CAM power reduction.This provides a performance advantage over other memory search algorithms. It will reduce the peak current , average power consumption (36%),boosted search speed (39%) and improved process variation tolerance.**

***Index Terms*-ATM, content addressable memory(CAM),match-line, Low power design,memory architecture,leakage currents.**

I. INTRODUCTION

Unlike standard computer memory (random access memory or RAM) in which the user supplies a memory address and the RAM returns the data word stored at that address, a CAM is designed such that the user supplies a data word and the CAM searches its entire memory to see if that data word is stored anywhere in it.If the data word is found, the CAM returns a list of one or more storage addresses where the word was found (and in some architectures, it also returns the data word, or other associated pieces of data).Thus, a CAM is the hardware embodiment of what in software terms would be called an associative array. The data word recognition unit was proposed by Dudley Allen Buck in 1955. A major interface definition for CAMs and other Network Search Elements (NSEs) was specified in an Interoperability Agreement called the Look-Aside Interface (LA-1 and LA-1B) developed by the Network Processing Forum, which later merged with the Optical Internet working Forum (OIF). Numerous devices have been produced by Integrated DeviceTechnology, CypressSemiconductor, IBM, Broadcom and others to the LA interface agreement. On December 11, 2007, the OIF published the serial lookaside (SLA) interface agreement. CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all search applications. There are cost disadvantages to CAM however.CAM uses additional circuitry and extra circuitry.The additional circuitry increases the physical size of the CAM chip which increases manufacturing cost. The extra circuitry also increases power dissipation since every comparison circuit is active on every clock cycle.Consequently, CAM is only used in specialized applications where searching speed cannot be accomplished using a less costly method.One successful early implementation was a General Purpose Associative Processor IC and System. A CAM cell serves two basic functions: bit storage (as inRAM) and bit comparison (unique to CAM).There are three types of core cells are used such as NAND cell ,NOR cell and Hyprid type cell[2].

II.CAM BASICS

We now take a more detailed look at CAM architecture. A small model is shown in Figure1.It consist of core cells,searchline ,matchline, MLSA and an encoder. Searchdata register is used to get the input from the user,and then it will be compared with the memory bank through search line.Matchline sensing amplifiers are used to sense the voltage variations from the matchline.Encoder is used to identify the location of the output[2].

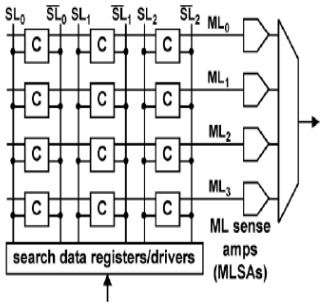

Fig.1 Basic CAM Structure

III.SEARCH SPEED BOOSTING

Auxiliary bit is used to boost the search speed of the CAM.The parity bit based CAM design is shown in Fig. 2(b) consisting of the original data segment and an extraone-bit segment, derived from the actual data bits.In Conventional CAM additional bits are used to filter some mismatched

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CAM words before the actual comparison.These additional bits are derived from the databits.In Fig.2.(a).the number of '1's from the stored words are counted and kept in the countedbitsegment[1].

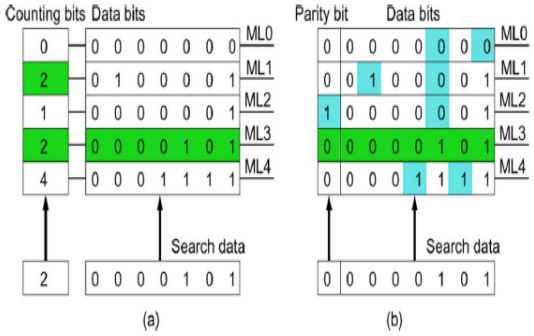

Fig.2.Conceptual View of (a)Conventional CAM,(b)Parity bit based CAM

When a search operation starts, number of "1"s in the searchword is counted and stored. These additional bits are compared first and only those that have the same number of "1"s (e.g., the second and the fourth) are turned on in the second sensing stage for further comparison. Derivation of additional bits in this scheme will reduces the search speed.For increasing the search speed of the CAM Paritybits are used.In Fig.2.(b)original data segment and an extraone-bit segment were derived from the actual data bits. In this the odd parity and an even parity will be calculated.However these paritybits reduces the sensing delay and boost the search speed.

IV.EFFECTIVE GATED POWER TECHNIQUE

The CAM architecture with an effective gated power technique is depicted in Fig.3.That will be organised into words(rows) and bits(coloumns).It uses P-type NOR CAM and an ML structure.Transistors M1-M4 will be acting as a comparison unit and the cross coupled inverters will be act as SRAM storage. These are powered by two separate metal rails, namely V_{DDML} and the V_{DD} .The V_{DDML} is controlled by a Power transistor Px. Leakage current is one of the sources of power dissipation in low power VLSI design. Due to the charging and discharging of matchline the leakage is getting stronger. As shown in Fig 3.the gated power transistor is controlled by a feedback loop,it will auto turn off the power supply,when the voltage on the matchline will reaches the certain threshold level.By the introduction of the power transistor Px, the driving strength of the 1-mismatch case is about 10% weaker than that of the conventional design and thus slower.

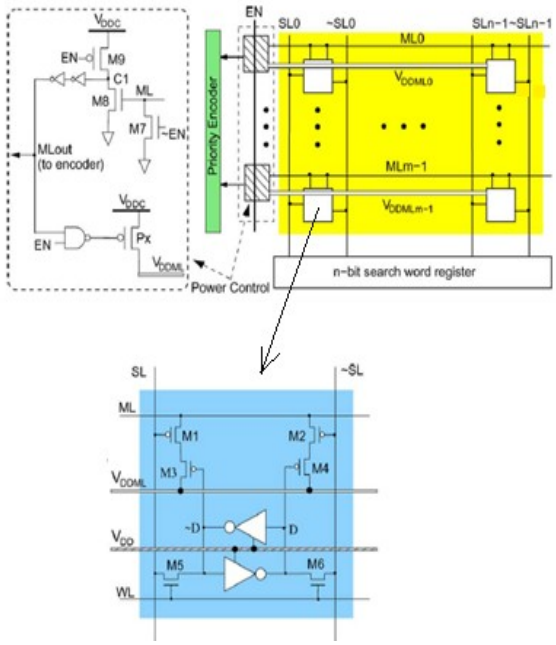

Fig.3. CAM architecture with an effective gated power technique.

As combining this sense amplifier with the parity bit scheme the overall search delay is improved by 39%[1]. This CAM architecture offers both low-power and high-speed operation.This will be used for Networking Applications.

V.ATM SWITCH

CAMs can be used in Asynchronous Transfer Mode (ATM) switching network components as a translation table. Since ATM networks are connection-oriented, be set up across them prior to any data transfer. There are two kinds of ATM virtual circuits: Virtual Path (identified by a virtual path identifier or VPI) and Channel Path (identified by a channel path identifier or VCI)[10].

VCI/VPI values are localized;each segment of the total connection has unique VPI/VCI combinations.Whenever an ATM cell travels through a switch,itsVPI/VCI value has to be changed into the value used for the next segment of connection. This process is called VPI/VCI translation. Since speed is an important factor in ATM network,the speed at which this translation occurs forms a critical part of the network's overall performance.

CAM can act as an address translator in an ATM switch and perform the VPI/VCI translation very quickly. During the translation process, the CAM takes incoming VPI/VCI values in ATM cell headers and generates addresses that access data in an external RAM (since standard CAMarchitectures cannot support the required capacity, a CAM/RAM combination enables the realization of multi- megabit translation tables with fully-parallel search capability).This application is shown in Fig.4

VPI/VCI fields from the ATM cell header are compared against a list of current connections stored in the CAM array. As a result of the comparison, CAM generates an address that is used to access an external RAM whereVPI/VCI mapping data and other connection

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information is stored. The ATM controller modifies the cell header using theVPI/VCI data from the RAM, and the cell is sent to the switch.

Asynchronous transfer mode (ATM) was developed primarily from the need of networking equipment to keep up with a large number of different services demanding different, and sometimes unknown requirements.

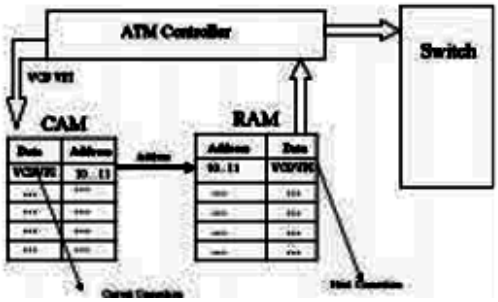

Fig.4.CAM in ATM Switch

ATM CELL ADDRESS

ATM switches, due to their connection based protocol, must translate each ATM cell address at every point along the routing path. As shown in Figure5, each ATM cell address is contained in two fields in a 5-byte header. The Virtual Path Identifier (VPI) is eight to 12 bits wide. Usually described as a 12-bit word. The Virtual Circuit Identifier (VCI) is 16 bits wide.

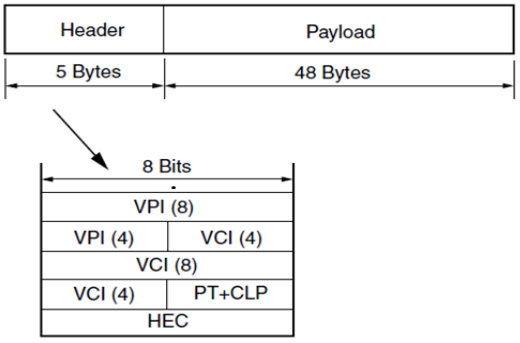

Fig.5.ATM Cell Address

A CAM operates as a data parallel processor. CAMs can be used to design Asynchronous Transfer Mode (ATM) switches. CAMs are an outgrowth of RAM technology.XAPP201 has an overview of CAM blocks versus RAM blocks. It also compares three approaches to designing CAM in Virtex devices. This application note focuses on a large CAM approach for ATM designs.ATM switches, due to their connection based protocol, must translate each ATM cell address atevery point along the routing path.

VI.RESULTS AND DISCUSSION

In this section, performance of the proposed design will be evaluated using the conventional circuit and those in [5], [6] as references. In[5], the power consumption is limited by the amount of charge injected to the ML at the beginning of the search.

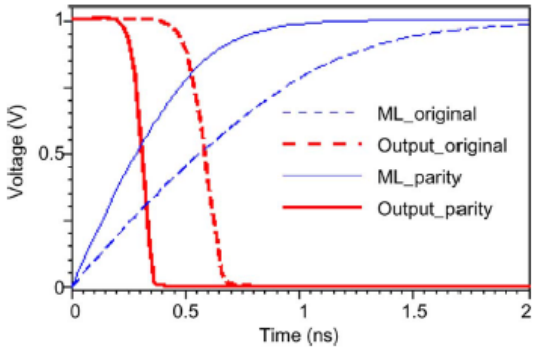

Fig.6. one mismatch ML waveforms of the original and proposed architecture with paritybit during the search operation.

In [6], a similar concept is utilized with a positive feedback loop to boost the sensing speed. Bothdesigns are very power efficient. As will be shown latter, the proposed design consumes slightly higher power consumption when compared
with [5] and [6] but is more robust against PVT variations.

We investigate the ability of the four designs to work at low supply voltage, by re-implementing the designs in [5], [6] and the conventional one into the same 65-nm technology. Designs in [5] and [6] demonstrate poor adaptability to voltage scaling. They can not operate at a supply voltage lower than 0.9 V.

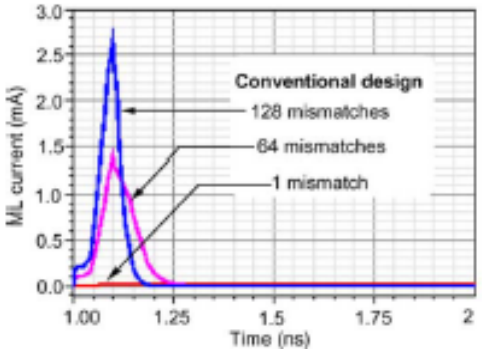

Fig.7.simulated transient current occurred on a row of 128 CAM cells during the compare cycle of the conventional CAM

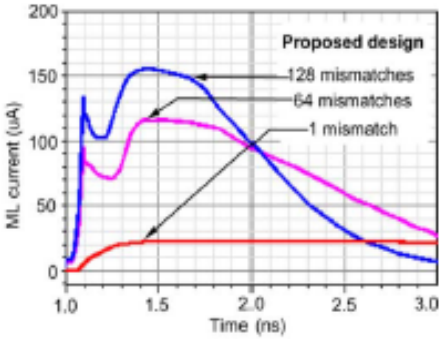

Fig.8.simulated transient current occurred on a row of 128 CAM cells during the compare cycle of the proposed CAM

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On the contrary, when the supply voltage scales to 0.5 V, both the proposed and the conventional design can work well.First, the search energy of the four designs in consideration is presented in Fig. 6. It can be seen that at 1 V supply voltage, [5] and [6]have the lowest energy consumption per search, followed by the proposed design. However, they cause to work when the supply voltage scales down to be low 0.9 V.

Between the conventional and the proposed design, the proposed design consumes 62% less powerconsumption at any supply voltage value.

Second, the sensing delay comparisonis shown in Fig. 9 where the proposed design has 39% improvementwhen compared to the conventional design and is the fastest design.

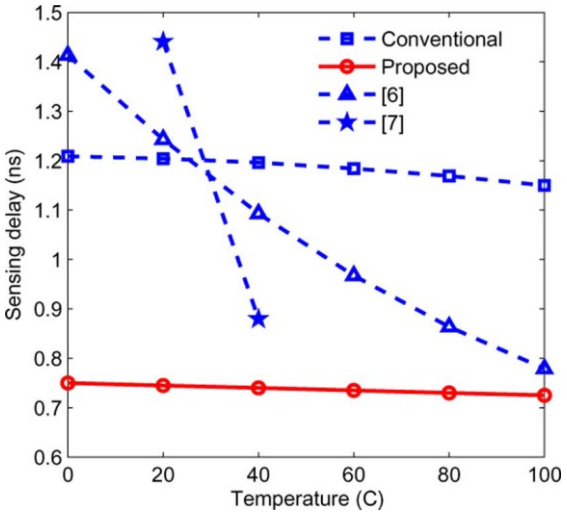

Fig.9. MLsensing delay of the four designs in consideration against temperaturevariations. Sensing delay is defined as the sensing delay of the 1-mismatch ML, i.e., the worst-case scenario.

This figure also suggests that sensing delay increases dramatically when supply voltage enters the near-subthreshold region. Finally,the corresponding leakage currents of the four designs against voltage scaling is are shown in Fig. 10. The proposed design is the second-bestcircuit after the conventional design. Both of them have about 20% and37% lower leakage current when compared to [5] and [6] at 1 V, respectively.This feature confirms that the proposed design is more suitablefor ultra-low power applications in 65-nm CMOS process and beyond.

Dynamic Power Consumption

Because the power-gated transistor is turned off after the output is obtained at the sense amplifier, the proposed technique renders a lower average power consumption. This is mainly due to the reduced voltage swing on the ML bus. Another contributing factor to the reduced average power consumption is that the new design does not need to precharge the SL buses because the EN signal turns off transistor P_x of each row and hence the SL buses do not need to be pre-charged, which in turn saves 50% power on the SL buses. Fig. 8 illustrates the average energy consumption (divided into ML power and SL power) of the proposed design as compared to other three benchmark designs, including all the power overhead of the control circuitry.

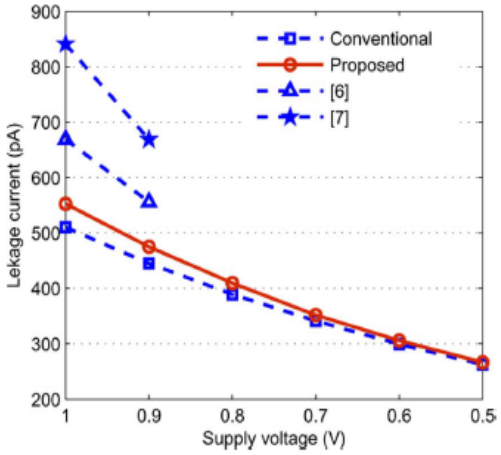

Fig.10. Standby leakage current of the existing and proposed designs in consideration against supply voltage scaling from 1 to 0.5v.

Since [5], [6], and the proposed design do not pre-charge the SLs before each compare cycle, their SLs energy consumption is only half of that of the conventional circuit. As for the ML energy, at 1V supply voltage the proposed design only dissipates 0.41 fJ/search/bit while that of the conventional design is 1.148 fJ/search/bit. Our ML energy consumption is higher than that of [5] (10.8%) and [6] (32%) but as will be shown below, our proposed design is much more robust against process and environment variations.

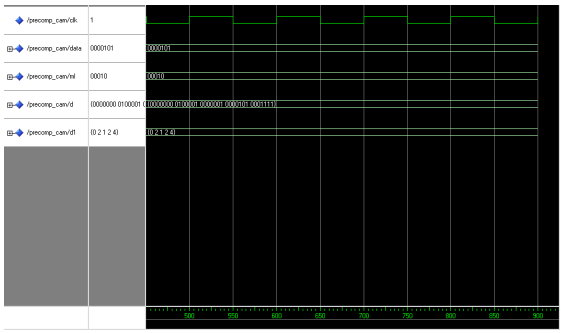

Fig.11.Simulation result for the conventional precomputation CAM

In conventional precomputation CAM the number of one's present in the datalines are counted and then it will be used for further comparison stage.The power consumption is very high and also the search speed is very low.

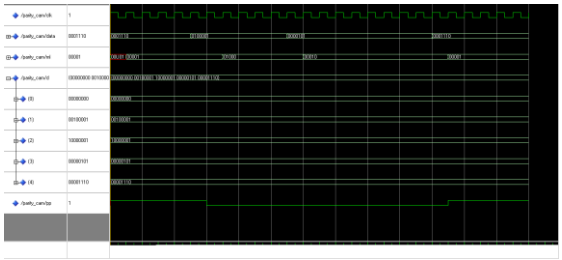

Fig.12.Simulation result for the parity bit based CAM

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In this the odd parity and even parity will be calculated then it will be used for further comparison stage.The power consumption is 36% lesser than conventional precomputation CAM and search speed is boosted 39% higher than precomputation CAM.

VII.CONCLUSION

We proposed a low power CAM for its networking application ATM switch. Now a days, ATM has achieved world-wide acceptance. One of the reasons is that ATM technology influences, and will influence in the next future, many segments of our society ,touching the consumer(interactive multimedia applications and games,etc.),public service(videoconferencing, etc.) and commercial markets (telemedicine, etc.). Low powet CAM with high speed can act as an address translator in an ATM switch and perform the VPI/ VCI translation quickly**.**In this by calculating odd and even parity the search speed will be boosted.By using an effective gated power transistor the power supply will be auto turn offed and thus will save power.It provides several major advantages, namely reduced peak current (and thus IR drop), average power consumption (36%),boosted search speed (39%) and improved process variation tolerance.

VIII. ACKNOWLEDGMENTS

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