International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 3, Issue 4, April 2014

Timing analysis for Deep-Submicron ASIC designs

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***Abstract*— Timing analysis is key factory before and after every physical designing of block level or chip level design. Timing Analysis is a method of verifying the timing performance of a design by checking for all possible timing violations in all possible paths. Determining the operating points as well as the delays of integrated circuits using static timing analysis. This approach is considered superior to testing the design with input vectors. It is much faster because not necessary to simulate the logical operation. It is based on a predetermined set of possible events of process variations, also called corners of the circuit. This paper discussed various key factors of timing analysis and variations in static timing analysis..**

***Index Terms*— Timing verification, Timing optimization, PVT variations, Setup and Hold.**

I. INTRODUCTION

Timing is important because just designing the chip is not enough; we need to know how fast the chip is going to run, how fast the chip is going to interact with the other chips, how fast the input reaches the output etc. Timing Analysis is a method of verifying the timing performance of a design by checking for all possible timing violations in all possible paths. It can be static as well as dynamic .STA is faster than dynamic timing simulation because there is no need to generate any kind of test vectors. Performs two basic tasks, timing verification and timing optimization. [3].

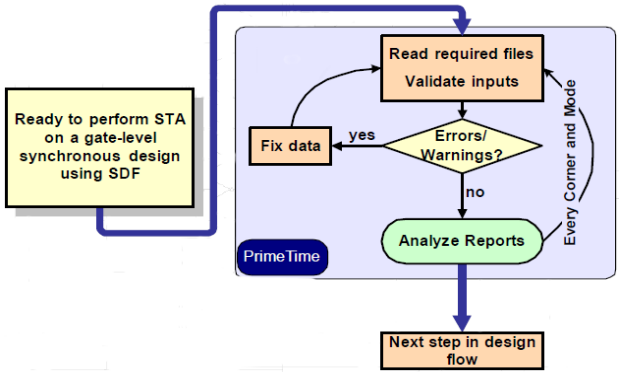


Fig. 1 STA flow [5]

STA at different design phases:

1) At the logical level (gate-level, no physical design yet), STA can be carried out using:
   a) Ideal interconnects or interconnect based on wireload model.
   b) Ideal clocks with estimates for latencies and jitter.
2) During the physical design phase, in addition to the above modes, STA can be performed using:
   a) Interconnect-which can range from global routing estimates, real routes with approximate extraction, or real routes with signoff accuracy extraction.
   b) Clock trees - real clock trees.
   c) With and without including the effect of crosstalk.

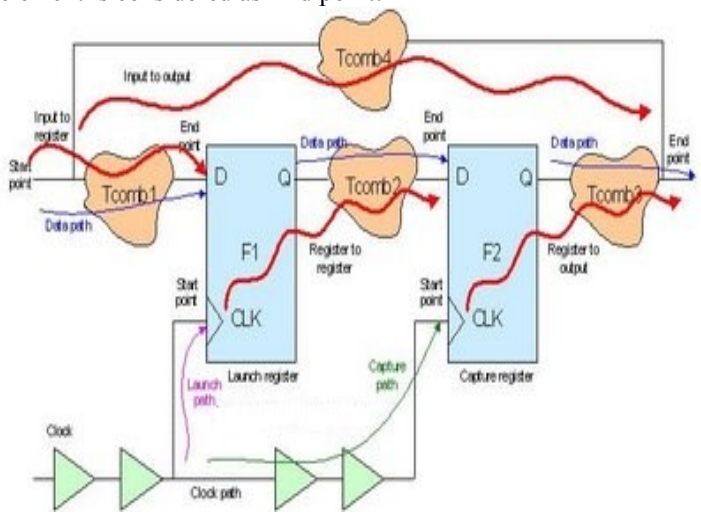
STA inputs are constraint file (.sdc), libraries, netlist and the desired outputs are high quality netlist, check timing. Basic steps of static timing analysis includes breaking of the design into sets of timing paths, calculating delays of each path and checking all path delays to see if the given timing constraints are met.

II. TIMING PATHS

Timing path is defined as the path between start point and end point where start point and end point is defined as follows:

a) Start Point: All input ports or clock pins of a sequential element are considered as valid start point.

b) End Point: All output port or D pin of sequential element is considered as End point.



. Fig. 2 timing paths [5]

Register - Register (Reg - Reg)

To meet the setup time requirement: Trequire>= Tarrival

Tarrival = Tclk1 + TDFF1(clk->Q) + TPATH

Trequire = Tclk2 - TDFF2(setup)

Tslack = Trequire – Tarrival

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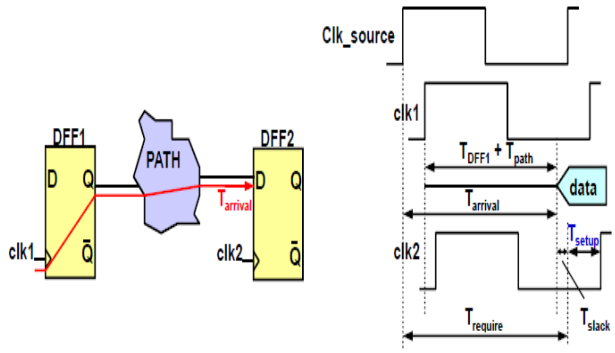

Fig. 3 Reg to Reg path [5]

PI (primary input) to Reg
Tarrival = TPI(delay) + TPATH
Trequire = Tclk1 - TDFF1(setup)
Tslack = Trequire – Tarrival

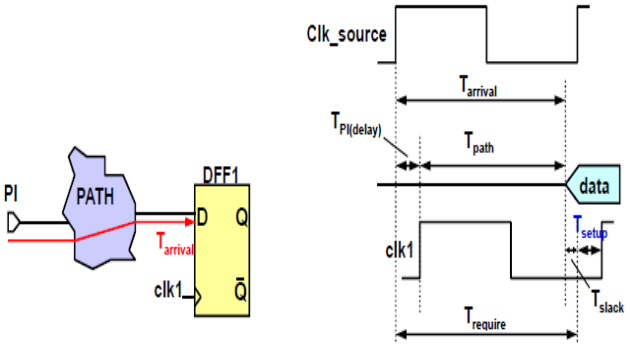

Fig. 4 PI to Reg [5]

Reg to PO(primary output)
Tarrival = Tclk1 + TDFF1(clk->Q) + TPATH
Trequire = Tcycle - TPO(output delay)
Tslack = Trequire – Tarrival

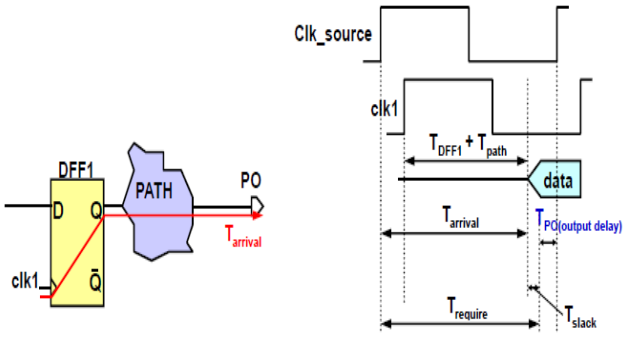

Fig. 5 Reg to PO [5]

PI to PO
Tarrival = TPI(delay) + TPATH
Trequire=Tcycle-TPO(output delay)
Tslack = Trequire – Tarriva

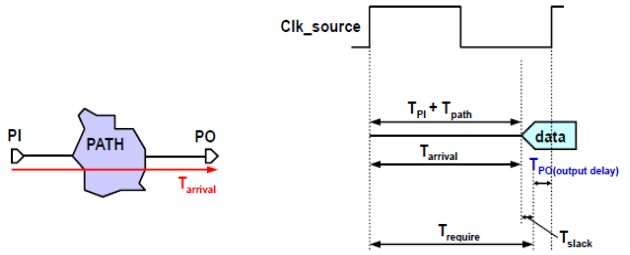

Fig. 6 Reg to PO [5]

III. SETUP AND HOLD TIME

Setup Time: Setup time is the minimum amount of time the data signal should be held steady before the clock event so that the data are reliably sampled by the clock.

Hold Time: Hold time is the minimum amount of time the data signal should be held steady after the clock event so that the data are reliably sampled

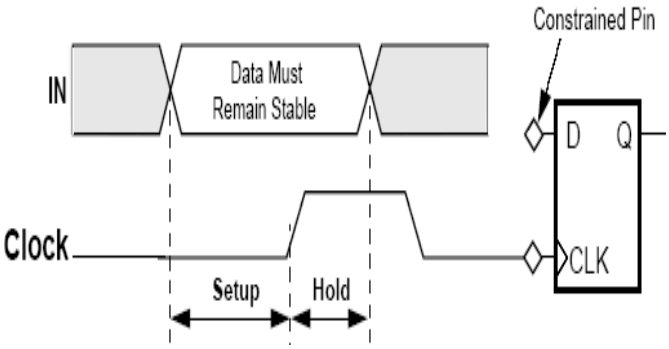

Fig. 7 Setup and Hold timings [5]

Slack: It is difference between the desired arrival times and the actual arrival time for a signal.
Required time: The time within which data is required to arrive at some internal node of the design.
Arrival Time:
The time in which data arrives at the internal node. It incorporates all the net and logic delays in between the reference input point and the destination node. An arrival time defines the time interval during which a data signal can arrive at an input pin in relation to the nearest edge of the clock signal that triggers the data transition.

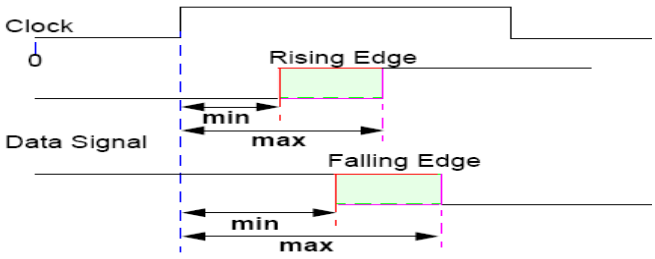

Fig. 8 Clock and Data Signal [3]

Setup Slack = Required time - Arrival time
Hold slack = Arrival time - Required time
Tsetup =RT-AT
Thold=AT-RT

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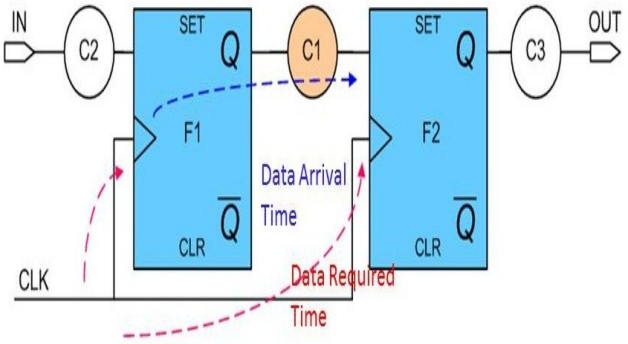

Fig. 9 Clock and Data Signal [5]

IV. PVT VARIATIONS AND STA

The major design challenges of ASIC design consist of microscopic issues and macroscopic issues. The microscopic issues are ultra-high speeds, power dissipation, supply rail drop, growing importance of interconnect, noise, crosstalk, reliability, manufacturability and the clock distribution. The macroscopic issues are time to market, design complexity, high levels of abstractions, reuse, IP portability, systems on a chip and tool interoperability. Timing Analysis (TA) is a design automation program which provides an alternative to the hardware debugging of timing problems. The program establishes whether all paths within the design meet stated timing criteria, that is, that data signals arrive at storage elements early enough valid gating but not so early as to cause premature gating.[2]

Process Variation

This variation accounts for deviations in the semiconductor fabrication process. Usually process variation is treated as a percentage variation in the performance calculation. Variations in the process parameters can be impurity concentration densities, oxide thicknesses and diffusion depths. These are caused by non-uniform conditions during depositions and/or during diffusions of the impurities. This introduces variations in the sheet resistance and transistor parameters such as threshold voltage. Variations are in the dimensions of the devices, mainly resulting from the limited resolution of the photolithographic process. This causes (W/L) variations in MOS transistors.

Supply Voltage Variation

The design's supply voltage can vary from the established ideal value during day-to-day operation. Often a complex calculation (using a shift in threshold voltages) is employed, but a simple linear scaling factor is also used for logic-level performance calculations. The saturation current of a cell depends on the power supply. The delay of a cell is dependent on the saturation current. Throughout a chip, the power supply is not constant and hence the propagation delay varies in a chip. The voltage drop is due to nonzero resistance in the supply wires. A higher voltage makes a cell faster and hence the propagation delay is reduced.

Operating Temperature Variation

Temperature variation is unavoidable in the everyday operation of a design. Effects on performance caused by temperature fluctuations are most often handled as linear scaling effects, but some submicron silicon processes require nonlinear calculations. When a chip is operating, the temperature can vary throughout the chip. This is due to the power dissipation in the MOS-transistors.

V. LIMITATIONS

While the timing and noise analysis do an excellent job of analyzing a design for timing issues under all possible situations, the state-of-the-art still are some aspects of timing verification that cannot yet be completely captured and verified in STA. Such as functional behavior across cross-cycles, clock-synchronization logic, false-paths, interface between analog and digital blocks, IO interface timings.

ACKNOWLEDGMENT

I would like to express the deepest appreciation to my Dept. of Electronics & Communication, Professor Shweta Kaundilya, who has the attitude and the substance of a genius: she continually and convincingly conveyed a spirit of adventure in regard to research and scholarship, and an excitement in regard to teaching. Without her guidance and persistent help this would not have been possible.

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ISSN: 2278 – 909X