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A LOW VOLTAGE AND LOW NOISE CMOS RF BULK INJECTION MIXER FOR UWB SYSTEM APPLICATION

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***Abstract*-A fully differential low voltage, low noise and low power CMOS mixer using bulk injection and switched biasing techniques with dc level shifter for ultra wide band (UWB) application is presented in this letter. The combination of the RF transconductance stage with the local oscillator (LO) switching stage in order to make a single transistor that is able to eliminate parasitic effects by the implementation of the bulk injection technique for a low supply voltage thus resulting low power consumption. This Technique also gives a flat conversion gain over UWB band. A switched biasing technique is adopted for a current source instead of static biasing which lowers noise over a wide range of frequencies. A dc level shifter is used for the symmetric switching operation in the tail current transistors. The proposed mixer features a measured conversion gain from 7.4 to 9.8 dB, an IIP3(3rd order input intercept point) from -10 to – 15.3 dBm, noise figures of 10.6 dB at 1MHz and 7.3dB at 100MHz and good FOM of 14.66dB. The mixer consumes 0.92mW power from a 0.75 V supply voltage.**

***Index Terms*- Bulk injection, Mixer,Static biasing, Ultra wide band (UWB).**

I.INTRODUCTION

UWB (**ultra-wide band**) communication was first conceived in the 1960s and used for radar, sensing, and military communications. In 2002, the FCC allocated 3.1–10.6 GHz available for UWB applications.CMOS technology down-scaling yields an improvement in power consumption, operation speed, and the area of integrated circuits. The low-voltage and low-power design issues are crucial for mobile wireless communication systems due to the limitation of battery capacity, and therefore the volume and weight of the transceivers can be further reduced using the low-voltage low-power technique.

A mixer is an essential component for the wireless transceivers. RF Mixer is a 3-port active or passive frequency translation device. The most popular active, double balancedmixer topography in RF IC design is the Gilbert Cell mixer**.** In general, the Gilbert-Cell mixers are widely used as the down-converter in CMOS transceivers since they are broadband with good conversion gain, good isolation to release the dc offset problem [2] and high linearity. However, it does have drawbacks, such as a relatively high supply voltage and power consumption due to a number of stacked transistors operating in the saturation region.

Among different advanced technology mixers based on the CMOS process, the folded structure mixer operates at a low supply voltage [3] due to the small number of stacked transistors but it requires a higher dc current with similar power consumption compared to the Gilbert-type mixer. The current bleeding technique was designed to improve the mixer noise since less current flows at the LO switching stage [1] but the parasitic capacitance increases between the LO switching stage, the RF transconductance stage, and the current bleeding circuit. The resonating inductors were used to eliminate this parasitic capacitance, but the inductor occupied a lot of chip area [5].In this letter, a mixer using bulk-injection andswitched biasingtechniques is presentedfor UWB applications. The bulk injection technique integrates the RF transconductance stagewith the LO switching stage in order

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to make the core circuits asingle MOSFET stage which lowers the supply voltageand has lower power consumption. The bulk-injection transistorsof the mixer are designed to operate in the sub-threshold region so the total power consumption is also reduceddue to less current [6]. However, the bulk-injection mixer has arelatively high NF, so the switched biasing technique with a dc level shifter is utilized which reduces not only the flicker noise, but also the whitenoise [7] caused by the symmetrical switching operation of tail current transistor. As a result of this technique, the NF for the proposedmixer improves by approximately 4 - 6dB compared to a mixerwith a fixed current source.This letter is organized as follows. In Section II, the design concept of the mixer isdescribed with operating principles of the bulk injection and switched biasing techniques. Section III presents the measurement results. Finally, the conclusions are summarizedin Section IV.

II. DESIGN OF MIXER

A. Bulk-Injection Mixer

The schematic of the single ended mixer core is shown in "Fig.1", which consists of a switched biasing stage (M1) with a dc level shifter (M4),the bulk injection stage (M2) and PMOS transistor stage (M3) as an active load. In contrast to the Gilbert-type mixer, the bulk injection core stage merges the RF transconductance stage with the LO switching stage. Typically, the gate terminal is connected to the RF input, and the bulk terminal is connectedto the source terminal in order to eliminate the body effect. In the proposed mixer, the gate terminal and the bulk terminal are used as inputs for the RF and LO, respectively. Since ithas one less stacked stage than the Gilbert-type mixer, the proposed mixer is able to operate with a lower supply voltage.

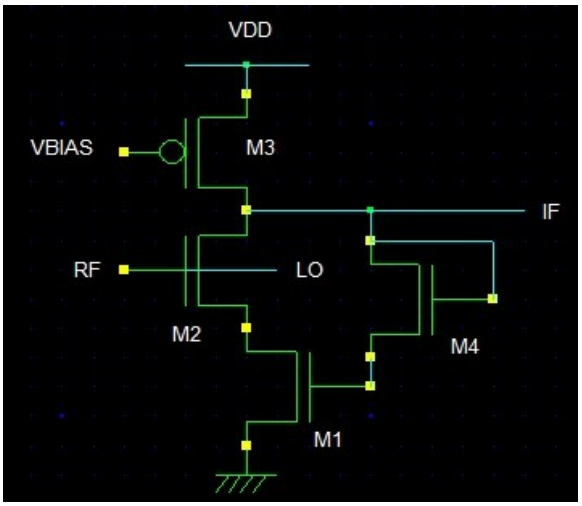


Fig.1.Single ended mixer core

"Fig.2" shows the proposed mixer using bulk-injection andswitched biasing techniques. The mixer consists of four partsincluding the switched biasing stage (M1-M2) as a current source whose gates are connected to IF nodes through a dc level shifting circuit (M11, M12 and RB) to reduce the output noise, the bulk-injection core stage (M3-M6), the loadstage(M7-M8)and output buffer stage (M9- M10) with R1 and R2 resistances to achieve impedance matching."Fig.3" shows the equivalent schematic of the proposed mixer using cadence tool.

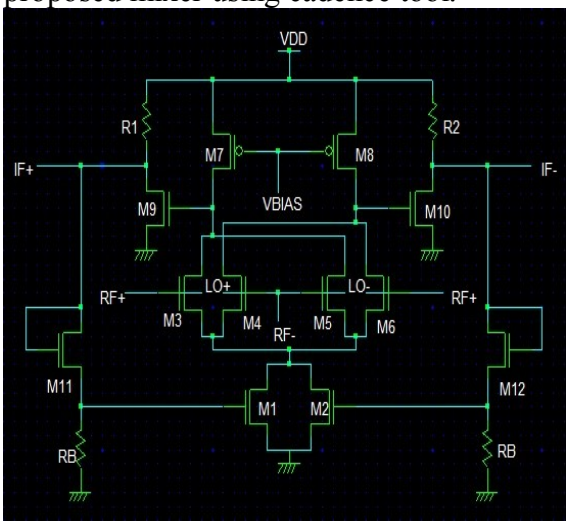


Fig.2.Schematic of the proposed mixer

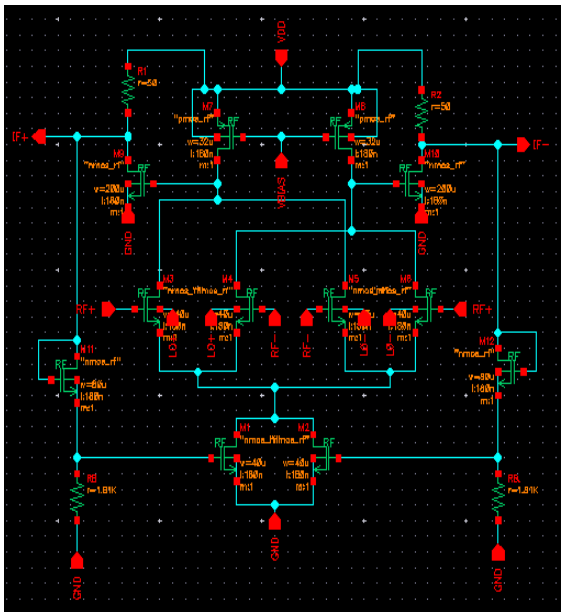


Fig.3.Equivalent schematic of theproposed mixer using cadence tool

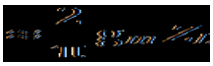
The gatesource voltage of the core transistors(M3–M6) is lower biased than the threshold voltage(VTO) in orderto operate in the sub-threshold region and the typical VTO is about 0.5 V in the 0.18-µm process.The proposed mixerconsumes only approximately 1 mA (250 A foreach of thefour core transistors) of the current.Since the threshold voltage of the transistor is a function of voltage between bulk and source (VBS),shown as following

$$\mathrm{VTH(LO)} = \mathrm{VTO} + \gamma\sqrt{2\varphi\mathrm{F} - \mathrm{VBS(LO)}} - \gamma\sqrt{2\varphi\mathrm{F}}$$

WhereVTOis the zero substrate bias threshold voltage, φFis the surface potential, and γ is the body effect factor. The LO signal is injected into the bulk of the transistors and modulates the threshold voltage. The switching function is controlled by the LO signals. The total dc-current will be limited under mini-ampere level, as a consequence the gate voltage of mixer core is biased smaller than threshold voltage. The high output impedance PMOS transistor M7 and M8 provide themselves as an active load to further reduce the ac current flow through mixer core. With low drain current of the mixer core, supply voltage (VDD) also can be lower due to lower voltage drop on the active load.

The drawback of parasitic capacitancebetween the RF and LO stages giving rise to a lowerconversion gain at a high frequency of a single balanced Gilbert typemixer is shown in "Fig.4(a)" is eliminated by the bulk injection mixer as shown in "Fig.4(b)". The voltage gains of the Gilbert-type mixer and thebulk-injection mixer can be expressed as, respectively,

$$A_{v,\mathrm{Gilbert}} \approx \frac{2}{\pi} g_m \frac{g_{mLO}}{g_{mLO} + j\omega Cp}$$

$A_{v,\mathrm{bulk\text{-}injection}}$ 

whereg_m and $g_{mLO}$are the transconductance of the RF and LOstage, respectively, andCp is the shunt parasitic capacitanceandZ_L denotes the load impedance.From the above two equation thebulk-injection mixer has a smaller conversion-gain fluctuationthan the Gilbert-type mixer. Therefore, this technique makesit possible to achieve a widely flat conversion gain across theentire UWB bandwidth [8].

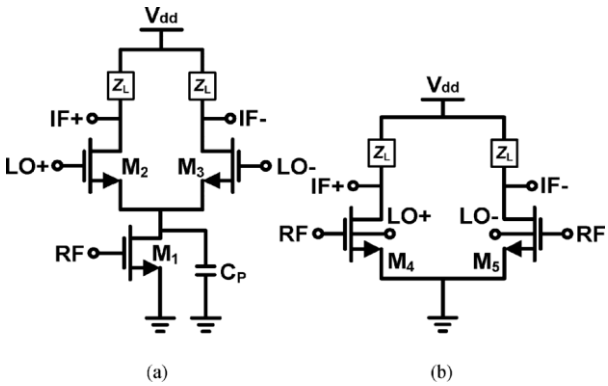


Fig.4(a).Single balanced Gilbert-type mixer. Fig.4(b). Bulk injection mixer

The bulk injectionmixer has a critical drawbackin that it is noisier than the

Gilbert-type mixer because the LOsignal input is inserted directly through the body terminal andcontributes to a noisier drain current of theMOS transistors [9].The additive noisy drain current of the transistors M3-M6 canbe expressed as follows:

$$\overline{i^2 nd, sub} = 4kTRsubg^2 mb\Delta f$$

Where k, T, $R_{sub,}$ g^2_{mb}andΔfare the Boltzmann's constant,absolute temperature in degrees Kelvin, substrate resistance,bulk transconductance, and noise bandwidth in hertz, respectively. Since the bulk-injection technique degrades the NF,the switched biasing technique, discussed in Section II-B, isadopted in order to improve the noise performance.

B. Switched Biasing Technique

The switched biasing technique splitsthe tail current source into two half-size transistors and then alternatelyswitches them using the IF output signals. The resultis a lower flicker noise while maintaining the same dc currentsupply aswith the fixed-biasing current source. This technique has been used primarily for improving the phasenoise in a voltage-controlled oscillator (VCO) design [10]. The noise current ofa tail current transistor, which flows into the load stage with thebias current of the mixer when a LO switch is on, is consideredas a critical noise source in the mixer. Since tail currenttransistors are periodically switched to operate between accumulationand strong inversion regions, randomly trapped chargecarriers are released, which lowers the flicker noise. Moreover,the switched biasing transistors are controlled by the outputsignal itself through the dc level shifter which is composed oftransistors, M11 and M12 (80um/0.18um), and resistors, RB(1.81 KΩ). In VCOs adopting this technique, switched tail-currenttransistors are directly connected to output nodes withoutusing the dc level shifter because of its large output swing.Thus, the switching operation of the tail current transistor pairis asymmetric due to a large difference in the voltage betweenthe dc of the output nodes and the threshold voltage of the tailtransistors.This causes both switched transistors to remain inthe on-status for a short time, which degrades the output noisefigure. To solve this problem in the proposed mixer, a dc levelshifter is adopted to provide the tail current transistors with aproper gate-source voltage to make the overdrive voltage verysmall for the symmetric switching operation with a small output swing. The sizes (40um/0.18um) for the switched biasingtransistors (M1-M2) were selected to generate a sufficientcurrent with a small overdrive voltage to minimize the outputnoise figure.Therefore, a reduction in the noise generated by a MOS transistorin part of the current source should result in a lower NFas compared to a static or fixed biasing current source.

In addition,by using self-biasing with the IF output signal to drive thetail current transistor, the mixer does not require a supplementarybias or current mirror circuit; these would cause additionalpower consumption and current source variation generated byan unsettled supply voltage.

The small signal gain of this mixer can be expressed as

$$G = -g_m(Ro\text{-}nMOS \parallel Ro\text{-}pMOS)$$

Where Ro-nMOSand Ro-pMOSrepresent the output resistances of the NMOS and PMOS transistors, respectively. The$g_m$is the trans conductance of the NMOS transistor.

So the conversion gain of the mixer can be expressed as

$$CG = -2/\square g_m(Ro\text{-}nMOS \parallel Ro\text{-}pMOS)$$

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The conversion gain of the mixer is proportional to thetransconductance of the core transistors (M3-M6) with (50um/180um). Therelationship between the transconductance and the gate widthof the core transistors is

$$g_m = \sqrt{2\mu_n c_{ox} \frac{W}{L} I_D}$$

Where μn, Cox, W, L and I_D are the electron mobility, gate oxide capacitance per unit area, gate width of the core transistors(M3-M6), gate length of the core transistors(M3-M6), and drain current, respectively. The drain current is fixed by the tail current source (M1-M2). To achieve a sufficient transconductance, and thus a high conversion gain, a large gate width of core transistors is required.

The loadstage consists of pMOS transistors, M7-M8 (32um/0.18um),in place of resistors. Although the active load has a disadvantagein noise performance, it enables a lower supply voltage. The biasingvoltages of each transistor are determined to appropriatelyoperate in low supply voltage. In the core transistor, the biasingvoltages of VDS and VGS are 516 and 511 mV, respectively.VDS and VGS of the active load transistors are biased by -194 and -800 mV, respectively.The common-source transistors M9 and M10 (200um/180um) are used as output buffers to achieve the impedance matching for measurement.

The mixer's figure of merit (FOM) can be expressed as

$$\text{FOM} = 10\log\left(\frac{10^{G/20} \cdot 10^{(IIP3-10)/20}}{10^{NF/10} \cdot P}\right)\text{dB}$$

where G and NF represent the voltage gain and noise figure in dB. The dc power consumption (P) and IIP3are expressed in W and dBm, respectively.

III. MEASUREMENT RESULT

The proposed mixer was implemented using cadence tool of version 6.1.5. The conversion gain was measured at an IF frequency of 264 MHz.“Fig.5” shows very flat conversion gain over the wide IF frequency. The RF power was selected to be -30 dBm, andthe LO power was chosen to be 5 dBm in order to achieve the maximum conversion gain of 9.8 dB, as shown in “Fig.6”. The high low power required is a disadvantage of the bulk injection technique.“Fig.7” shows the measured and simulated conversion gainover a wide range of frequencies. The measured conversiongain has ranged between 7.4–9.8 dB for 2.4–11.9 GHz. The fact that thesimulated and measured results had very similar gains and flat characteristics indicates that the proposed mixer will have sufficient3-dB bandwidth from 0.2 to 13.3 GHz in order to covertheentire UWB frequency bands. “Fig.8” illustrates the measured results of the two-tone test,which was performed with a 5-MHz difference and 10.296 GHzof RF frequency. The inputthird-order intercept point (IIP3) of 10 dBm and the input-referred1-dB compression points (P1dB) of 19 dBm wereachieved.

The total power dissipation of the propose mixer core, with an output buffer, was 0.92mW from a supply voltage of 0.75 V. ”Fig. 9” shows the measured double-side band noise figure(DSB NF) over the output frequency range from 100 kHz to 100 MHz.The DSB NF of the proposed mixer was 10.9 dBat 1 MHz, which was improved by about 6 dB compared tothe conventional mixer that was an exact copy of the proposedmixer,with the omission of the dc-level shifting circuit buthaving the same device sizes and operating conditions such assupply voltage, current level, and LO power. The FOM of this mixer was 14.66 dB which is higher than other CMOS mixers.

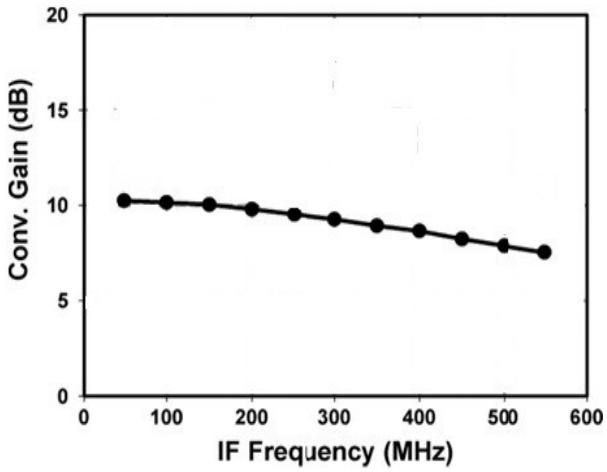

Fig.5.Simulated conversion gain versus IF frequency for an LO power of 5 dBm.

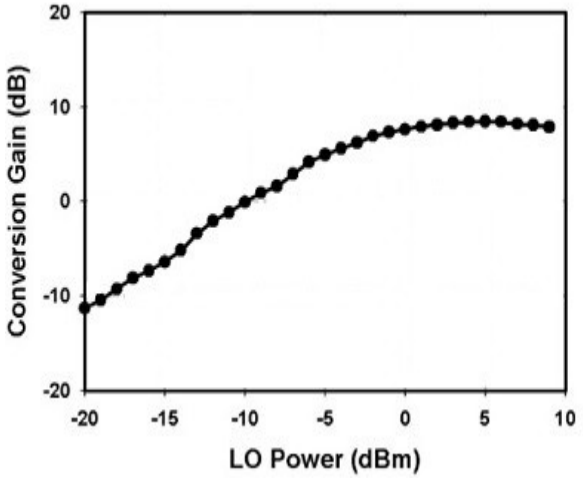

Fig.6.Measured conversion gain versus LO power at 6.6 GHz with an RF power of -30dBm and IF of 264 MHz.

According to the results of [10], the switched biasing technique lowersthe flicker noise significantly and the white noise by a smallamount. This can explain that thermal noise is also reducedby 3 to 4 dB even at frequencies beyond the corner frequency (>10 MHz).

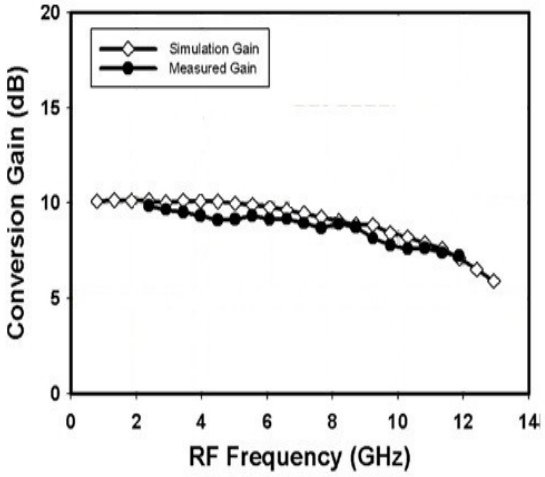

Fig.7.Measured and simulated conversion gain versus RF frequency withan RF power of -30 dBm and LO power of 5dBm at an IF of 264MHz.

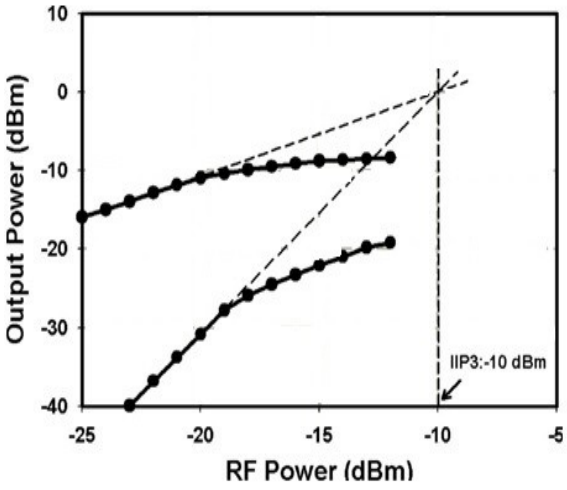

Fig.8.Measured IF output power versus RF power with an RF frequency of10.296 GHz and an LO power of 5 dBm at an IF of 264MHz.

In Table I, the performance of the proposed mixer is summarized and comparedwith state-of-the-art CMOS UWB mixers [11]–[14]. The proposedmixer using bulk-injection and switched biasing techniques hasa wide bandwidth, high gain, low NF, low voltage, low power and good FOM.

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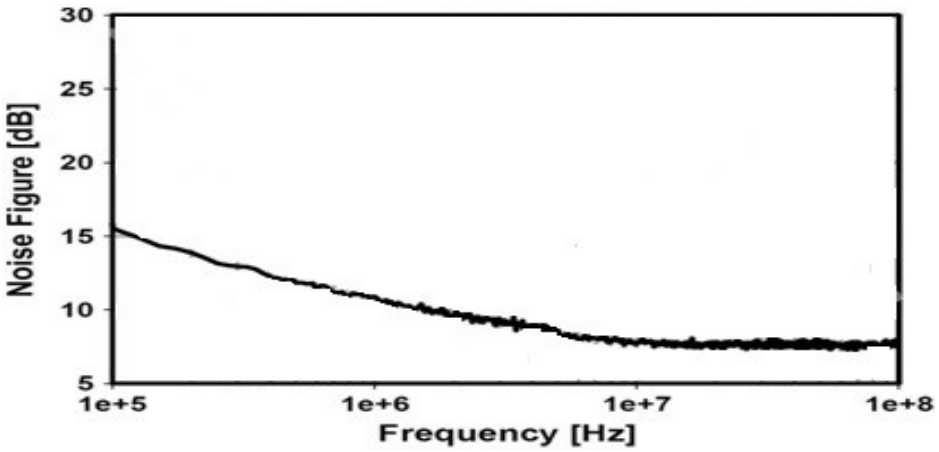

Fig.9.Measured DSB noise figure versus IF frequency.

TABLE.I. (Comparison to UWB CMOS Mixers) (* including buffer stage)

Ref.	CMOS process	Frequency (GHz)	IF (MHz)	LO Power (dBm)	Conversion Gain (dB)	DSB NF (dB)	IIP3 (dBm)	Supply Voltage (V)	Power (mW)	FOM (dB)	Technique
3	0.18µm	0.2 - 16	528	-2	8.7	-	-10	1.8	15*	12.6	Folded structure
14	0.13µm	10 - 35	100	13	1	-	-4	1.6	6	15.7	Bulk-injection
11	0.13µm	3.1 – 10.6	264	-3	14	14.5	-11	1.2	1.85	9.38	Folded structure
12	4Mnm	1-10	100	8	9.5	21.2	-	1.1	1.46	6.96	Bulk-injection
13	0.18µm	0.5 – 7.5	100	5	5.7	15	-5.7	0.8	0.5	12.96	Bulk-injection
4	0.18µm	0.2 - 13	264	5	9.9	11.7	-10	0.8	0.88	13.8	Bulk-injection & Switched biasing
This Work	0.18 µm	0.2 – 13.3	264	5	9.8	10.6 @1MHz 7.3@ 100MHz	-10	0.75	0.92*	14.66	Bulk-injection & Switched biasing with dc level shifter

IV. CONCLUSION

In this paper, we presented an UWB mixer with low voltage, low power and low noise characteristics that was implemented using cadence tool of version 6.1.5.in0.18 µm CMOS process. The bulk-injection techniqueenables the proposed mixer to achieve low voltage and lowpower consumption and a superior gain flatness characteristicresulting from the reduction of parasitic capacitances.By adopting theswitched biasing technique, the flicker and white noises originatingin the tail current were considerably reduced. In addition,a dc level shifter for the tail current transistors was used for the symmetric switching operation.Measurement results showedthat the proposed mixer obtained extensive bandwidth from 0.2to 13.3 GHz with a maximum conversion gain of 9.8 dB, a good FOM OF 14.66dB and a minimum NF of 7.3dB. Therefore, the proposed mixer should be useful for an RFfront-end receiver for UWB systems.

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