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Cascaded H-Bridge Eleven level Inverter Employing PI Control Technique

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Abstract **–This paper presents a single phase cascaded h-bridge eleven level inverter topology with a sinusoidal pulse width modulated control scheme. This inverter topology uses two reference signals, instead of one reference signal, to generate PWM signals for the switches. A Proportional Integral controller is used to control this system to get the required output voltage. This topology magnifies the fundamental output voltage with reduction in total harmonic distortion. The proposed system is verified through simulation and the results are compared with the conventional single-phase h-bridge nine-level inverter.**

Keywords: **Multilevel inverter, Cascaded H-Bridge inverter, Total Harmonic Distortion, PI Controller, Sinusoidal pulse width modulation**

I. INTRODUCTION

Nowadays Multilevel inverters are drawing attention from researchers and manufacturers due to their more benefits over conventional three level pulse width modulated inverter [PWM] inverters. They offer improved output waveforms, smaller filter size, lower EMI, lower total harmonic distortion (THD), and others [3]-[8].

The three common topologies for multilevel inverters are as follows: 1) diode clamped (neutral clamped) [9]–[11]; 2) capacitor clamped (flying capacitors) [12]–[14] and 3) cascaded H-bridge inverter [15]–[17].

In addition, several modulation and control strategies have been developed or adopted for multilevel inverters, including the following: multilevel sinusoidal (PWM), multilevel selective harmonic elimination, and space-vector modulation [3], [18].

A typical single-phase five-level inverter adopts full-bridge configuration by using approximate sinusoidal modulation technique as the power circuits. The output voltage then has the following five values: zero, $+1/2V_{dc}$, V_{dc},$-1/2V_{dc}$ and $-V_{dc}$ (assuming that Vdc is the supply voltage). The harmonic components of the output voltage are determined by the carrier frequency and switching functions. Therefore, their harmonic reduction is limited to a certain degree [25].

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To overcome this limitation, this paper presents a 11 level PWM inverter whose output voltage can be represented in 11 levels: zero, $+1/12\ V_{dc}$, $+1/6\ V_{dc}$, $+1/4\ V_{dc}$, $+1/3\ V_{dc}$, $+1/2\ V_{dc}$, $-1/2V_{dc}$, $-1/3V_{dc}$, $-1/4V_{dc}$, $-1/6V_{dc}$ and $-\ 1/12V_{dc}$. As the number of output levels increases,the harmonic content can be reduced. This inverter topology uses two reference signals, instead of one reference signal, to generate PWM signals for the
switches.

In this paper, a single-phase cascaded h-bridge multilevel inverter with five H-bridges are proposed. A Sinusoidal PWM control technique is adopted in the firing circuit to provide an acceptable control in the inverter output voltage. PI controller is used to control this system to get the required output voltage. Matlab/Simulink software is used in this work to simulate the power and control circuits. The waveforms of output voltage and current along with the harmonic spectra of output voltage are presented and evaluated.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

The structure of single cell of multilevel-cascaded H - bridge configuration is shown in the Fig.1. The output of this cell will have three levels namely *+V, 0* and *–V*. Using one single H-bridge, a three level inverter can be realized. This circuit requires about four switching devices. To realize higher levels of output voltage, the H- bridge circuits are cascaded. The circuit has many advantages like simple, modular, improved waveform which results in reduced total harmonic distortion. This circuit provides high quality output when the number of levels in the output increases and also this reduces the filter components size and cost.

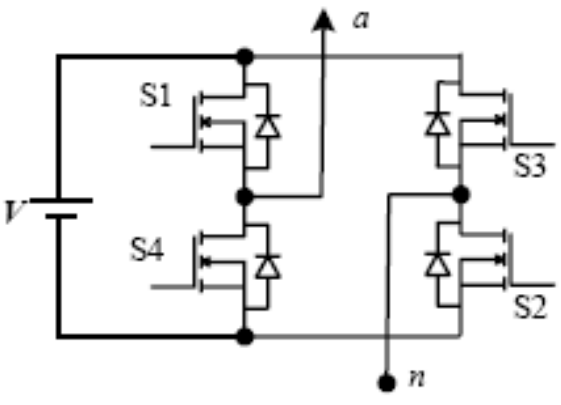

Fig 1. Single cell of multi-level cascaded h-bridge inverter

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III. CASCADED H-BRIDGE MULTILEVEL INVERTER WITH PI CONTROLLER

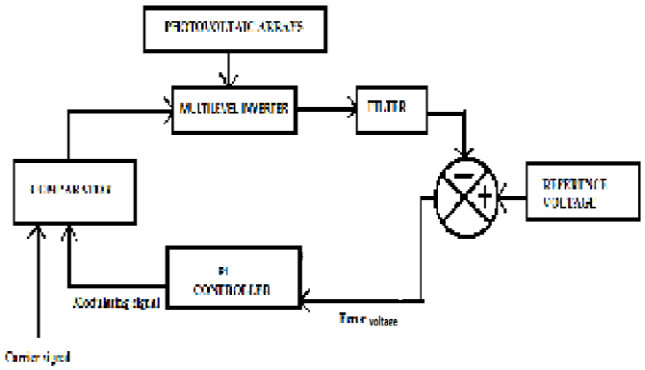

Fig. 2. Cascaded MLI with PI Controller

The Cascaded H-bridge Multilevel inverter with PI controller is shown in Fig. 2. The circuit needs independent dc source which is supplied from the photovoltaic arrays. The gate signals are generated using Sinusoidal pulse width modulation strategy. The output of the cascaded h-bridge eleven level inverter is fed to the load through LC filter to produce sinusoidal output (Vo) which is compared with the reference voltage (Vref) to generate the error signal (e). The input to the PI controller is e. The output of the PI controller i.e the compensating signal (Cs) is added with the reference signal to yield the required modulating signal (ms) which is used to generate the gating pulses. Thus a voltage feedback loop is established to realize the required sinusoidal output voltage. Hence whenever the load is non linear the distortion in the output is more.

IV. PWM FOR HARMONICS REDUCTION

Several modulation strategies have been developed for multilevel inverters. The most commonly used is the Sinusoidal PWM technique. The Sinusoidal pulse width modulation technique is used here to control the output voltage of the multilevel inverter without affecting the low order harmonics. The modulation technique uses a triangular carrier wave at a high witching frequency is compared with the sinusoidal reference wave at a fundamental output frequency. The intersection between these two signals defines the switching instants of the SPWM pulses.

V. SIMULATION RESULTS

In this paper, the simulation model is developed with MATLAB/SIMULINK. The simulation results of the proposed cascaded h-bridge eleven level inverter is shown in Fig.3. The proposed circuit needs independent dc source which is supplied from photovoltaic cell. Simulated output voltage and output current and THD analysis for eleven level cascaded h-bridge inverter is shown in figure 4 and 5. The THD analysis for conventional inverter is shown in figure 6. From the simulated analysis the THD value is low (11.05%) when compared with the conventional single-phase h-bridge nine-level inverter, the THD value is 18.53%.

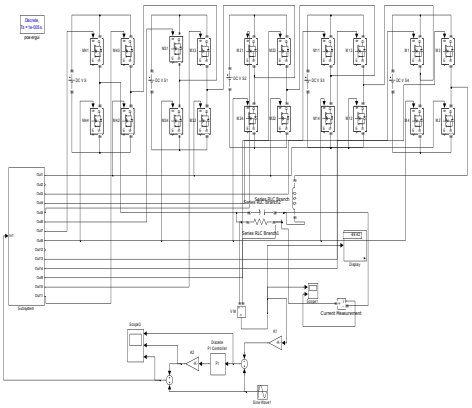

Fig.3.Proposed topology

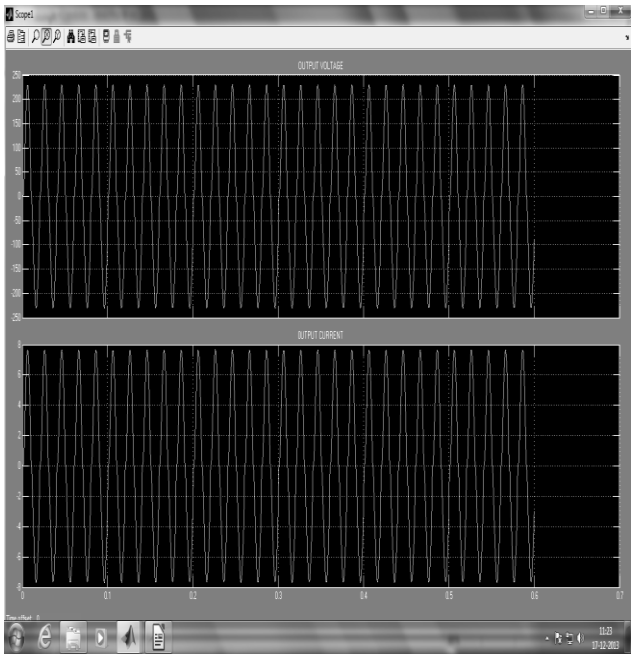

Fig.4.Output voltage and current waveforms

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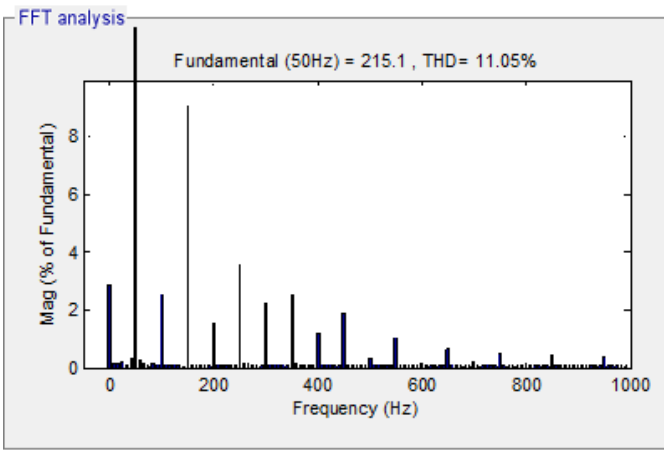

Fig.5.THD analysis (Proposed inverter)

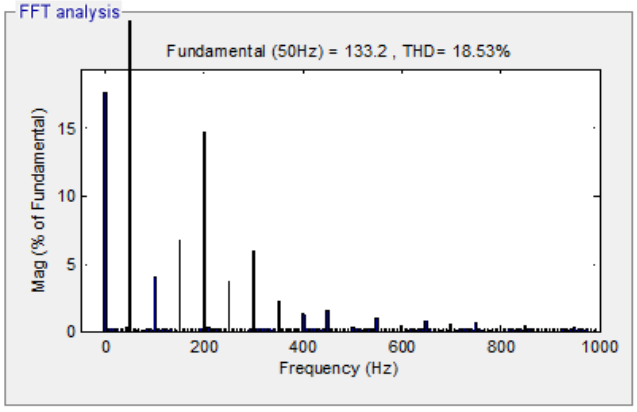

Fig.6.THD analysis (Conventional inverter)

VI. CONCLUSION

A complete simulation model of a cascaded h-bridge eleven level inverter has been proposed using Matlab/Simulink software. A PI controller is to optimize the performance of the inverter. Sinusoidal PWM control technique is adopted in the firing circuit to provide an acceptable control in the inverter output voltage. Simulation results prove that with this inverter strategy, the low order harmonics are substantially reduced and are compared with that with the conventional single-phase h-bridge nine-level inverter.

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