

# Integration of Photonics Technology for Communication Systems

Sudhakar Sekar

**Abstract**— Video is an important revenue generating platform for both cable and telecom service providers and will also impact heavily on the traffic management issues. The purpose of this paper is to pursue photonics integration to resolve traffic issues in transmission. Only viable photonics integration processes can achieve this goal and keep up with future needs of communication systems beyond terabit/s. We must promote the adoption of viable integration processes to sustain progress.

**Index Terms**—Cable, Communication Systems, Photonics, Video.

## I. INTRODUCTION

The traffic management issue can be met by improving the performance of the present set of optoelectronics devices such as DFB laser arrays, tunable lasers, fast and complex modulators, AWG, and ROADM, Low cost OEO conversions allow an alternate approach to network evolution. Coherent transmission eliminates signal impairments but presents multiple challenges. In the FTH/curb environment, the potential for truly photonic integrated circuits to reduce assembly costs and simplify functionality is slowly becoming a reality. 100Gb/s transport in the core is achievable to accommodate the Internet growth forecast in the short-term. However, there is no such optoelectronics device base for a terabit/s network. In fact, we now expect the demand for high speed bandwidth to exceed our capacity significantly over the next decade. This implies that network-choking will be an ongoing problem similar to ‘traffic jams’ in major cities today. The threat of display-choking is emerging on the radar screens of many television manufacturers as they progress towards HDTV. By providing the consumer with an active cable solution with embedded optics, it may be possible to reduce 10Gb/s technology cost through volume production to ease the issues of display-choking. Only viable photonics integration processes can achieve this goal and keep up with future needs of communication systems beyond terabit/s. We must promote the adoption of viable integration processes to sustain progress. We also believe that photonics integration will positively impact the volume consumer market for interconnects in addition to the network edge.

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## II. PROSPECTS AND ISSUES FOR OPTICAL FIBER NETWORKS

Global internet traffic has increased at a rate of 75% per year for the past five years. Video now accounts for nearly 30% of all internet traffic and will account for 60% within a few years. These changes have driven widespread deployment of 10Gb/s links. The industry is installing new network upgrades to 40Gb/s in the core. The timing and level of deployment of 40Gb/s systems depends strongly on the pricing relative to 10Gb/s core network utilization and capacity planning. Carriers are asking for 100Gb/s transport in the core to accommodate the growth forecasts. Installations of carrier Ethernet in the metro networks have been increasing rapidly. Increases in data and flat or reduced cost of services have created an increasing burden for network operators.

Some contenders view the all-optical network as inefficient due to concerns such as:

- Wavelength congestion
- No sub wavelength grooming
- Service limited by number of wavelengths
- Agility and service provisioning

An alternate approach to network evolution is to enable low-cost optical-electrical-optical (OEO) conversions and bandwidth virtualization across the network. The concept is straightforward: manage the bandwidth of the network in one control plane and the wavelength transport in another plane. It is possible to eliminate impairments in signal transmission by encoding the transmitted signal and recovering the phase, polarization, and amplitude with a local oscillator and electronic processing. To achieve coherent detection, we must know the phase, frequency, polarization and amplitude of the signal. Coherent communication presents multiple challenges but promises potentially large rewards. At both 40 Gb/s and 100 Gb/s, coherent transmission allows longer transmission distances (6000 km and 2000 km) and high tolerance to both chromatic dispersion (CD) and polarization mode dispersion (PMD)

## III. PHOTONIC INTEGRATION

At the component level, a key issue is the rate of progress in photonic integrated circuits (PIC) versus optical-hybrid approaches to provide the functionality needed in future components and systems. For monolithically integrated

solutions to be commercially successful, the technology must deliver superior performance and reliability at acceptable prices and performance. Telecom networks have successfully deployed integrated devices such as arrayed waveguide gratings (AWG), reconfigurable optical add drop multiplexers (ROADM), distributed feedback (DFB) laser arrays, tunable lasers, and 10Gb/s modulators including complex modulators (e.g., DQPSK and duo binary modulators). Commercial deployment of integrated devices with ten laser arrays has been achieved. For passive optical networks, several companies have been developing photonic integrated circuits to replace the transistor outline (TO)-can triplexer module deployed in FTTH systems.

Several companies believe successful integration can only be achieved by a hybrid integration approach, such as fabricating a silicon platform and die bonding InP devices to the platform. It is possible to develop complex transmitter and receiver assemblies by the hybrid integration approach. In this example, the yield curve is too steep to fabricate complex DFB arrays. Some level of hybrid integration would allow better cost and performance than discrete devices. But beyond some threshold of complexity, discrete devices would be more profitable.

The essence of the silicon photonic integrated circuit approach is to fabricate both optical and electrical elements by complementary metal oxide semiconductor (CMOS) wafer processing. Several research groups are investigating silicon light emission [5]. One approach is to grow or implant erbium crystals in the silicon. Another approach is to exploit quantum size effects (silicon/silicon dioxide nano particles) to generate gain and hence light within the crystal. In yet another approach, III-V material is wafer bonded to a silicon resonator to provide the light source or photon generator. The silicon waveguide acts as the laser resonator circuit and provides the feedback mechanism to the photon generator to enable gain and hence lasing action. The principal issue with the wafer bonding process for silicon CMOS devices is the introduction of the III-V material into the fabrication facility or process line. The alternative to the silicon CMOS photonic integration approach is the “pure” InP integration. This wafer process technology begins with an InP substrate rather than a Si substrate. Flip chip bond pads or wire bonds connect the InP chips to the electrical drivers. Silicon-based electrical circuits (CMOS, SiGe) supply the electrical functions to drive the InP integrated device. One of the key issues with InP integration is yield. The advantage of the InP optoelectronic integrated circuit is the light source. The laser can be integrated into the circuit at the base wafer epitaxial growth stage. This approach makes it possible to fold most of the routing and detection emission functions into the first wafer processing stage [3].

To succeed, photonics integration must satisfy several requirements, including the following:

- High yield
- Compression of multiple functions into a single device
- Scalable connection to both electrical and optical input/output ports
- Lower cost of production and better performance
- Reduction in power consumption and thermal load

**• Why increased interest in Photonic Integration?**

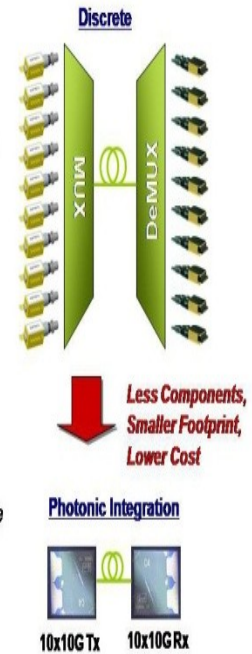
- Further cost reduction of current (discrete) component technology limited
- New emerging, high volume applications (10x10G, 12x10G, 4x25G)
- FTTH provides economies of scale for InP

**• What technology?**

- InP capable of (almost) all of the necessary networking functions
- Silicon on Insulator, Silica on Silicon, etc
- Technology choice is application specific → monolithic and hybrid integration will co-exist

**• What are the requirements?**

- Performance - no compromise for integrated vs. discrete solution
- Yield to performance and reliability specs determine viability and cost



Concept of Integration for Low Cost and high performance

There are at least three approaches to photonics integration:

- Silicon/Silica hybrid integrated components.
- Silicon photonic integrated components.
- InP fully integrated components.

IV. SILICON/SILICA HYBRID INTEGRATED COMPONENTS

Several companies believe successful integration can only be achieved by a hybrid integration approach, such as fabricating a silicon platform and die bonding InP devices (sub-components) to the platform. Due to the large separation of the required grating (DFB) wavelength, selective area growth and grating fabrication are unable to provide reasonable yield [2]. Due to the large separation of the required grating (DFB) wavelength, selective area growth and grating fabrication are enable to provide reasonable yield. Some level of hybrid integration would allow better cost and performance than discrete devices. But beyond some threshold of complexity, discrete devices would be more profitable. In the hybrid approach it is necessary to address additional performance and integration issues. In this example, discrete DFB devices are coupled to the AWG device. This coupling imposes two new constraints that impact the process yield:

- Coupling efficiency
- Placement accuracy

In fact, both constraints are connected in this example because the InP discrete device has a certain Gaussian far-field pattern and hence coupling coefficient to the single mode silicon waveguide. The coupling depends on both x-y displacement and z-axis displacement. High-accuracy

placement equipment is required to control the coupling. It is possible to develop complex transmitter and receiver assemblies by the hybrid integration approach. This approach makes it possible to test each channel independently. Furthermore, we can integrate discrete devices with multiple wavelengths without the constraint of epitaxial growth control. For example, four DFB lasers with widely spaced wavelengths would require four different grating pitches spaced within four chip widths [2]. A standard holograph- IC grating method could not satisfy this requirement. E-beam writing or phase mask contact printing would be the only solutions. Additionally, performance over the desired temperature range would require selective area growth on a chip-to-chip basis to alter the material gain peak and de-tuning wavelength for the individual DFB laser. This approach would suffer from yield and process control problems. The simpler solution is the hybrid, which relies on proven technology and understanding of chip yield.

### V. SILICON PHOTONIC INTEGRATED COMPONENTS

The essence of this approach is to fabricate both optical and electrical elements by complementary metal oxide semiconductor (CMOS) wafer processing. The goal is to carry CMOS electrical processing technology and photonic building blocks. Several companies are investing in this approach as the next logical step in optical integration. In the CMOS photonics evolution, the idea is to put all the different photonics functions into discrete devices that can then be patterned and processed as individual circuit elements in a CAD design package [3]. The basic six elements of the CMOS photonic process are:

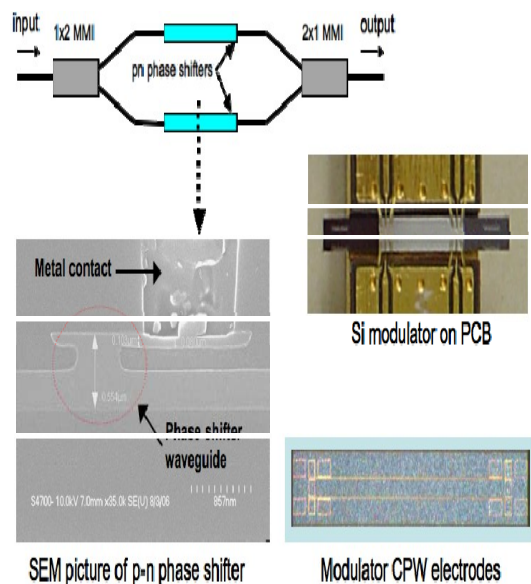
- Light generation.
- Light guiding.
- Light manipulation.
- Light detection.
- Light circuit integration and assembly.
- Light and electronic integration.

Silicon is a group IV element and hence has an indirect electronic band structure. The direct transition for a photon to generate light is not allowed. Within the crystal structure, a phonon (lattice vibration) would need to be coupled to a photon transition to generate light. Alternatively, material engineering—i.e., folding the band structure or manipulating the quantum confinement of electrons and holes—is another strategy to generate light (photons). One approach is to grow or implant erbium crystals in the silicon. Another approach is to exploit quantum size effects (silicon/silicon-di-oxide nano particles) to generate gain and hence light within the crystal. One advanced approach (apart from laser die bonding to a silicon waveguide) is the wafer fusion device. In this approach, III-V material is wafer bonded to a silicon resonator to provide the light source or photon generator. The silicon waveguide acts as the laser resonator circuit and provides the feedback mechanism to the photon generator to enable gain and hence lasing action. The III-V photon generator is typically InGaAlAs/InP quantum well laser epitaxial material. The characteristic manufacturing step is to fuse a thinned wafer of this material to the

processed silicon waveguide resonator. Then an electrical current is applied to the p and n contacts of the devices. The principal issue with the wafer bonding process for silicon CMOS devices is the introduction of the III-V material into the fabrication facility or process line. The stringent quality control in most CMOS facilities limits wafer bonding approaches to the end of the process line. Temperatures above 500 °C can degrade the III-V material processed on the silicon.

In silicon CMOS photonics, the light manipulator or modulator is directly connected to the laser by a silicon waveguide. The emission wavelength needs to be below the band gap of the semiconductor to avoid absorption. Hence this type of device is well suited for long-wavelength communication applications [5]. Today, Intel, Luxtera, and Light wire are fabricating silicon photonic CMOS devices with 1300-nm lasers. This strategy limits the device applications to long-wavelength transceiver applications, which are dominated by the VCSEL 850-nm transceiver for speeds less than 10Gb/s.

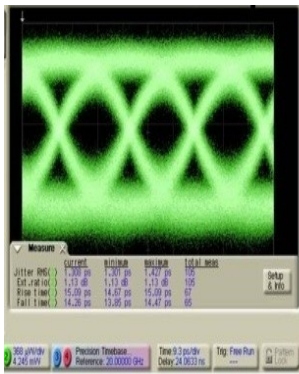
The waveguide is connected to a Mach Zender (M-Z) modulator fabricated in the silicon as a waveguide, with a phase shifter on the arms of the modulator. The silicon waveguide modulator allows high-speed modulation, but the loss in the guide is proportional to the roughness of the sidewalls of the guide. To alleviate the loss, the manufacturers rely on the high-precision photolithography processes [4].



#### A. Silicon CMOS High-Speed Mach Zender Modulator

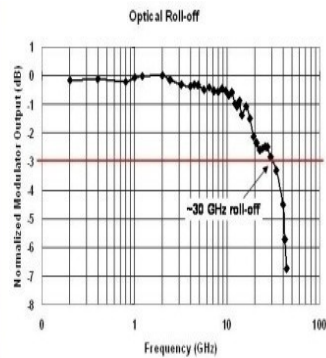
The bandwidth of the modulator has been measured as an independent coupled device. Modulation at 40Gb/s has been demonstrated recently, with further work ongoing to improve the rise and fall times of the modulated signal. The S21 optical bandwidth currently has a 3 dB bandwidth of 30 GHz. This bandwidth is adequate to demonstrate the potential for 40Gb/s operation, but higher bandwidth would be desired to allow margin for long distance transmission.





40Gb/s Data Transmission:

"Eye" diagram from large signal, pseudo-random bit sequence (prbs) testing

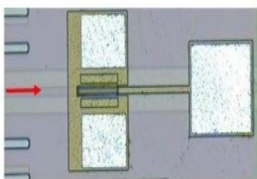


Small Signal Testing:  
 Optical 3 dB roll off ~30 GHz

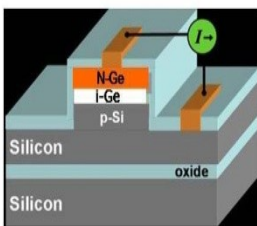
L. Liao, A. Liu, D. Rubin, T. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaki, and M. Paniccia, "40 Gbit/s silicon optical modulator for high-speed applications," *Electron. Lett.*, Vol. 43, No. 22, pp. 25<sup>th</sup> October 2007

### B. Large Signal Modulation of a CMOS Mach Zender

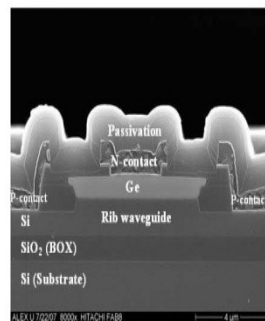
The final stage of the CMOS circuit is to reconvert the optical signal back to the electrical domain. To do this, we need to integrate the photodetector into the CMOS circuit. One of the preferred methods is to use a dopant in the silicon to absorb the received light. As the light flows in silicon optical waveguides around the optoelectronic integrated circuit (OEIC), a waveguide detector is needed for optimum efficiency. This approach allows simple integration into the circuit process. Germanium has been used extensively in photodetector technology for several years. The conventional approach is to form a receiver by implanting or fusing germanium onto the silicon waveguide and forming a p-n junction to sweep the carriers out of the absorption region. Planar processing of the detector chip simplifies the fabrication process [5]. The p and n contacts are fabricated on the surface of the silicon waveguide, allowing simple wire bond pads to be used for test purposes. An alternative approach would be to use the laser source in reverse as receiver technology, rather than as emitter technology.



Top View



SEM Cross-Section



SEM Cross-Section

### C. Germanium Waveguide Photodetector

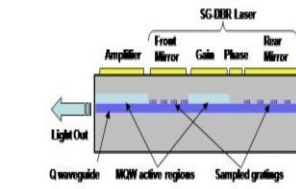
The germanium waveguide detector has a bandwidth of around 30GHz. Receiver eye diagrams with 40Gbit input signals have been demonstrated with low noise on the receiver eye.

## VI. INDIUM PHOSPHIDE FULLY INTEGRATED COMPONENTS

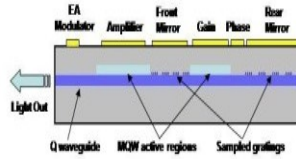
The alternative to the silicon CMOS photonic integration approach is the "pure" InP integration. This wafer process technology begins with an InP substrate rather than a Si substrate. Flip chip bond pads or wire bonds connect the InP chips to the electrical drivers. Silicon-based electrical circuits (CMOS, SiGe) supply the electrical functions to drive the InP integrated device. InP devices are direct band gap semiconductors. The light emitting portion of the device is grown in an epitaxial step. The growth of the crystal structure is controlled to within a few monolayers, i.e., several angstroms of thickness. Today, multiple device structures exist. These device structures are well understood and have been deployed in the communications industry for over 20 years. Today, most telecom networks employ InP long-wavelength devices for transmission over the core, metropolitan, and PON networks. One of the key issues with InP integration is yield. When we integrate multiple complex epitaxial devices onto the same substrate, the yield is a function of both the design complexity and the constraints of the epitaxial structure and processes. In the silicon world, the impact of process control and yield is extremely well understood. In the InP world, the yield has not approached 90%. One key difference between the CMOS photonic approach and the pure-play InP photonic approach is the standardization of processes. Within CMOS fabrication lines, standard process control and constraints have led to a successful outsource fabrication business model for electronic components. Within the InP community, the largest market has been in telecommunications. The high reliability constraints and cost associated with fabrication of small volumes have hindered the standardization of fabrication process compared to CMOS. Furthermore, intellectual property issues complicate the widespread standard application of several key processes, including the growth of epitaxial layers [6].

One target for InP photonic integration is tunable DFB devices for dense division multiplexing systems. Several device designs are currently in production. For wide tuning ranges, vernier-type tuning has proven to be the most effective. In this approach, two gratings are slowly mapped onto each other to pick out a single wavelength for emission. One concern is the loss (absorption) in the cavity. Hence several monolithic devices include an amplifier or gain section in the device.

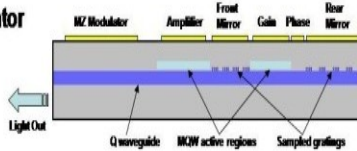
- **Amplifier section**
  - Boosts power
  - Provides shutter/VOA
  - Standard on all products



- **EA modulator section**
  - Provides for modulation
  - 300km reach @ 2.5G



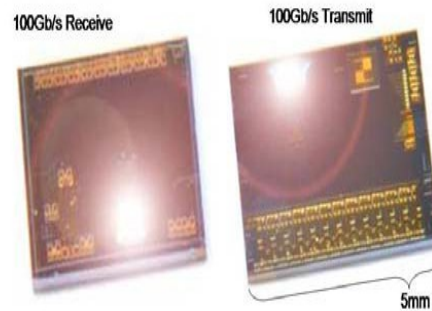
- **ILMZ with MZ modulator section**
  - 80km reach @ 10G



Monolithic Tunable Laser Device With or Without Modulator Section

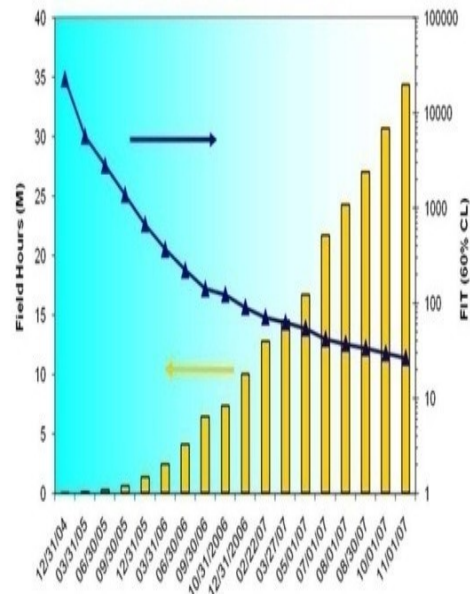
It is difficult to integrate the InP device with the electronic control functions. Today, the process capabilities of InP electronics remain many years behind those of CMOS electronics. As a result, optoelectronic integrated circuits require separate electronic chips connected by wire bonds or flip chip technology. This illustrates an example of the tunable laser chip for telecom applications with wire bond pad layout. Multiple pads are required to control the different section of the chips. The semiconductor optical amplifier section and the laser gain section both require large current supplies. The tunable integrated devices are well understood in terms of performance and control. Mach Zender devices are very useful for new long haul systems because they make it possible to integrate coding functions on the same mask layout [1]. The advantage of the InP optoelectronic integrated circuit is the light source. The laser can be integrated into the circuit at the base wafer epitaxial growth stage. This approach makes it possible to fold most of the routing and detection emission functions into the first wafer processing stage. Waveguide integration is part of the epitaxial stage, using mode converted or couple waveguide solutions to route the light from the emitter into the waveguide path. Alternative ideas include using silicon dioxide waveguides deposited on the wafer during the fabrication processes. Defect formation, morphology control and doping control of the waveguide/laser/detector, and design setup are the key issues concerning the epitaxial growth. The epitaxial device integration approach requires careful design of the chip layout. The key issues are Feedback into the laser, noise control from spontaneous emission for the photodetector, and electrical pad layout. CAD tools for design and integration are available, but the tool sets are inferior to those available for CMOS electronics. Several companies have been developing photonic integrated circuits for switching systems for telecom applications. The biggest issue with telecom applications is the reliability of the system. Carriers expect photonic ICs to deliver 25 years of service before replacement. D-WDM systems are targets for photonic integration because of the requirements for tight wavelength spacing, cost, and

wavelength control [2]. Infinera has been developing devices for their D-WDM switches using photonic integrated circuits based on InP technology. Their approach is to integrate multiple transmitters and receiver on the same piece of InP, as shown in Figure below,



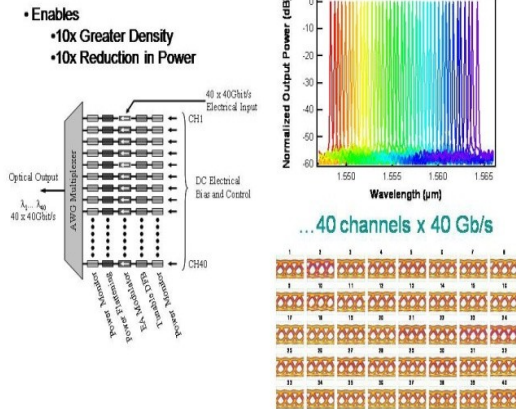
- Improves cost, space, power, reliability
- Makes digital processing economical

A key figure of merit for the reliability of a device or component is the failures in time (FIT) rate. To qualify for communication networks, integrated circuits must meet Telcordia GR-468 standards. Below Figure shows an example of the FIT rate that is achievable for optoelectronic integrated circuits.



This example of the FIT rate reaching nearly 10 FITs after three years of field deployment is a key milestone for InP photonic integrated circuits. It shows that integration can achieve comparable reliability to single component devices. The main concerns moving forward are increasing yield and increasing functionality. D-WDM systems require high channel counts and high modulation speeds. One approach to meeting these requirements is to add more functionality into the current OEICs and increase the number of integrated sources. Currently research is ongoing to improve the density of channels

and to increase the modulation bandwidth of the transmitter and receiver components.



**Wavelength Density and Modulation Capabilities of the PIC**

Higher levels of integration make it possible to reduce power consumption. As new modulation formats increase the single wavelength information carrying capacity, integration of different components can enable greater fiber bandwidth.

VII. CONCLUSION

Photonic integration research has been ongoing for nearly 20 years. The applications have targeted primarily the telecommunication industry. With the recent advances in both CMOS photonics for computer interconnects and InP integration for long haul systems, the future is bright for continued advances in this field.

VIII. REFERENCES

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