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Read and Write Stability of 6T SRAM

Sangeeta Singh, Vikky Lakhmani

Abstract— **SRAM cells are designed to ensure that the contents of the cell are not altered during read access and the cell can quickly change its state during write operation. These conflicting requirements for read and write operations are satisfied by some specific conditions to provide stable read and write operations SRAM cell read stability and write -ability is major concerns in nanometer CMOS technologies, due to the progressive increase in intra die variability and V_{DD} scaling. In conventional six transistors (6T) SRAM cell, read stability is very low due to the voltage division between the access and driver transistors during read operation this paper analyzes the read stability and write ability of 6T, SRAM cell structures. SRAM cell stability analysis is typically based on Static Noise Margin (SNM) investigation.**

Index Terms— **Noise margin, read stability, read noise margin (RNM), cell Ratio, Pull up transistor, SRAM cell, Static Noise Margin (SNM), write ability, Write noise margin (WNM)**

I. Introduction

SRAM is mainly used for the cache memory in microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to high speed and low power consumption. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. With increased device variability in nanometers scale technologies, SRAM becomes increasingly vulnerable to noise sources 6T SRAM is a bistable device consists of two back to back connected inverters (M_1,M_2,M_5,and M_6)along with two access transistors(M_3 and M_4) being separately connected to two complementary bit lines Bit(b) and $\overline{Bit}(\bar{b})$ Two access devices which allow to access to internal node of the cell. Two back to back inverters store two stable states 0 and 1. SRAM cells consist of a latch and, it is called static memory because cell data is kept as long as power is turned on and refresh operation is not required for the SRAM. The 6T SRAM provide very less Read Noise Margin(RNM). To obtain higher RNM in 6T SRAM cell width of the pull down transistor(M_1 and M_2) has to be increased but this increases area of the SRAM which in turn increases the leakage currents. The widerspread of local mismatch leads to reduced SRAM reliability. For the demand of minimizing power consumption during active operation,supply voltage scaling is often used However, SRAM reliability is even more suspect at lower voltages. V_{DD} min is the minimum supply voltage for an SRAM array to read and write safely under the required frequency constraint. Therefore, the analysis of SRAM read/write stability is essential for low power SRAMs

In this paper we analyze various alternatives to improve cell stability in read and write mode. This techniques studied are based on transistor width and word and bit line voltage modulations. We show that it is possible to improve cell stability during read operation while reducing current leakage as opposed to current methods that improve cell read stability at the cost of leakage increase.

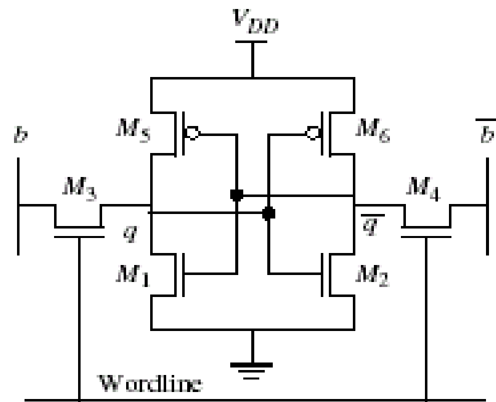

Figure 1 Basic structure of 6 T SRAM

II. Basic Operations Of 6T SRAM

Like other memories, there are three operation modes for SRAM cell: standby (or hold), read, and write modes.

In the standby mode, the word line is set to a low-voltage level and both the internal nodes are isolated from the bit lines. In the read mode, both the bit lines are usually precharged to a high-voltage level before the PO FETs are turned on, the charges in the bit lines will disturb the charges stored in the internal nodes, and if the inverters are not "strong" enough (i.e., the static noise margin is too small. The bit lines may not be sufficiently discharged to the expected values,

Hold(Stand By)

The access transistors(M_3 and M_4) are disabled by applying word line signal WL to a low voltage level equal to '0' to their gates and both the internal nodes are isolated from the bit lines.. The data is held in the latch. The bit lines (b and $\bar{b}$) are charged to the supply voltage.In the large SRAM array(e.g.>1 MB),most of the cell are in standby state ,which dominates the overall power consumption.

A. Read Operation

In the read operation, word line is activated while the external word line driver is disabled. The value can be determined by external logic if the inverter inside the SRAM cell drives the bitlines. The Bit lines (b and $\bar{b}$) of the cell are pre charged as given in the above step if reading is done just after write operation. In the read mode,the charges in the bit lines will disturb the charges stored in the internal nodes,and

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if the inveters are not strong enough'(i.e.the static noise margin is too small),the bit lines may not sufficiently discharged to the expected values.

B. Write Operation

In the write operation, in order to drive the bitlines, the big (external) tristate drivers need to activate first. The previous state of the cross-couple can easily be over write. It is because the internal driver (small transistor used in the 6T SRAM cell) is much smaller than the external drivers. Next, allowed the wordline transistors still, when shafting the data, the short-circuit will happen for just a few nanoseconds. Data to be written into the cell is applied to the bit lines (b and b). The access transistors (M_3 and M_4) are enabled by applying word line signal WL equal to'1' to the gates. When data '0' is to be written to storage node storing '1', the corresponding bit- line is applied with voltage equal to '0', resulting in a current flow through pull up device (say PUP1) to the bit line through the storage node storing high, which is pulled low. When the voltage of the high storage node is below the trip point of the other inverter (M_6 pullup-and M_2 pull down)the content of the cell flips due to feed back. The converse takes place when the storage node voltage is '0' and '1'is to be written. If the storage node is initially storing '0' and the data on the bit line is '0' then there is no change in the state of the cell. If the storage node is initially storing '1' and the data on the bit line is '1' then there is no change in the state of the cell. It is very essential that for easy write operation the pull up ratio (PR) given by the ratio of the width to length (W/L) ratio of the pull up device (PUP) to the width to length (W/L) of the access transistor (PG) should be small

III. SUCCESSFUL READ VS FAILURE READ

SRAM cells are designed to ensure the stable read so that the contents of the cell are not altered during read access, and the cell can quickly change its state during write operation. These conflicting requirements for read and write operations are satisfied by sizing the bitcell transistors to provide stable read and write operation. In read operation, an SRAM bitcell is most prone to failure. After the WL is enabled, voltage at the internal storage node storing a zero (q) slightly rises due to the voltage divider between the PG transistor (PG1) and the pull-down (PD I), as shown in Fig.2.24. If the voltage at q rises close to the threshold voltage of the adjacent pull-down, PD2, the cell may flip its state. Therefore, stable read operation requires that PDI should be stronger than PG I. Means
Drive strength of pull down device>>Drive strengrh of access device

$$\beta_d \gg \beta_a$$

$$\mu \frac{W_d}{L_d}\left(V_{cell} - V_{th,d}\right)^{\alpha} \gg \mu \frac{W_a}{L_a}\left(V_{wl} - V_{th,a}\right)^{\alpha}$$

Read stability failure is exacerbated by process variations, which affect all the transistors in the bitcell 15, 9. 541. To quantify the bitcell's robustness against this type of failure, static noise margin (SNM) is one of the most commonly used metrics 1611. A read stability failure can occur if the bitcell cannot hold the stored data, in which case SNM is zero [5. 54. 61). Read stability failure can occur any time the WL is enabled even if the bitcell is not accessed for either read or write operations. For example, in half-selected bitcells. the WL is enabled while the bitlines column is not selected (the bitcells are not actively accessed for read or write). These bitcells experience a dummy read operation because the bitlines are initially precharged to VDD, and the bitlines are discharged after the WL is enabled, hence, the bitcells become prone for read stability failure. Dealing with read stability failures is one of the biggest challenges for SRAM design and has been extensively studied 15, 9, 54). Circuit techniques to deal with read stability failures will be discussed in Chap. 3.

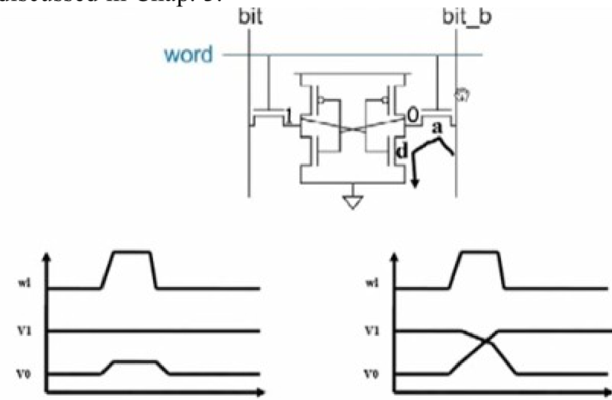

Figure 2 Successful Read Failure Read

IV. READ AND WRITE STABILITY

The SRAM cell read stability Data retention of the SRAM cell, both in standby mode and during a read access, is an impo rtant functional constraint in advanced technology nodes. The cell becomes less stable with lower supply voltage increasing leakage currents and increasing variability, all resulting from technology scaling. The stability is usually defined by the SNM [6] as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit. For a successful write, only one cross point should be found on the butterfly curves, indicating that the cell is mono - stable. WSNM for writing "1" is the width of the smallest square that can be embedded between the lower - right half of the curves. WSNM for writing "0"can be obtained from a similar simulation. The final WSNM for the cell is the minimum of the margin for writing "0"and writing "1‟ . A cell with lower WSNM has poorer write ability. Ce cellcell ratio Pull up ratio

V. SUCCESSFUL WRITE VS FAILURE WRITE

pull the internal node that is high down to a 0 to flip the cell. We would also like to use the same access transistors (M2 and M5) to read the contents of the bit-cell to keep the size of the cell as small as possible. This means that we should be careful to avoid driving a BL to 0 during a read operation so that we do not inadvertently write the cell. To prevent this problem, we prechargc both BLs to V1)0. and then allow them to float before asserting the W L. We can thus consider the BLs to be capacitors that are charged to VDD at the onset of the read access. The side of the cell that stores a 0 will slowly discharge its BL - the read is slow because the cell transistors are small and the BL capacitance is relatively large - while the other BL remains near V DD. By looking at the differential voltage that develops between the BLs, we can determine what value the cell is storing.

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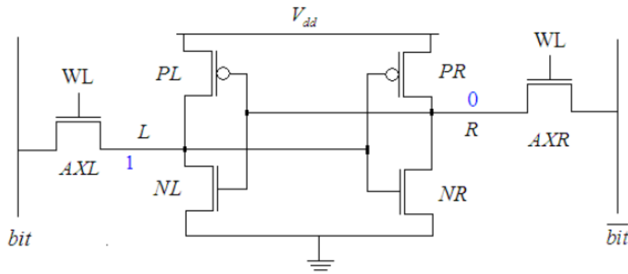

Figure 3 Write Operation

VI. EQUATIONS

A. Cell Ratio

$$cell\ ratio(CR) = \frac{size\ of\ driver\ transistor}{size\ of\ the\ load\ transistor}\ (during\ read\ operation)$$

$$= \frac{\left(W_1/L_1\right)}{\left(W_3/L_3\right)}$$

$$= \frac{\left(W_2/L_2\right)}{\left(W_4/L_4\right)}$$

B. Pull up Ratio

$$pull\ up\ ratio = \frac{size\ of\ load\ transistor}{size\ of\ the\ access\ transistor}\ (during\ write\ operation)$$

$$= \frac{\left(W_6/L_6\right)}{\left(W_4/L_4\right)}$$

C. Drive Strength

$$\beta = \mu C_{ox} \frac{W}{L}$$

VII. CONCLUSION

The improved read and write-ability (data stability), reduced dynamic and leakage power dissipation compared to standard 6T, makes the new approach attractive for nano scale technology regime, in which process variation is a major design constraint. The conflicting read and write problem is addressed by providing a separate read word line however, proposed design departs from the read SNM free SRAM designs those employs the separate read and write ports

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Sangeeta Singh Completed B.Tech from Madan Mohan Malaviya Engineering College Gorakhpur in 2004 in Electronics and Communication Engineering. She has more than six years of teaching experience in different colleges. She has taught different subjects of Electronics and Communication Engineering during her career as lecturer. Presently she is pursuing her M Tech in VLSI technologies from Mewar University Rajasthan

Vikky Lakhmani Completed B.Tech from Madan Mohan Malaviya Engineering College Gorakhpur in 1999 in Electronics and Communication Engineering. He completed his MTech from Uttar Pradesh Technical University in 2010. He has authored several international papers on VLSI and communication engineering. He has more than 8 years of teaching experience in different subjects in Electronics department. Currently he is working as an Associate Professor in RD Engineering College, Ghaziabad and also pursuing his PhD

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