Low power Hybrid CA register design for BIST applications

Amandeep Singh , P. Mohan Kumar, Amandeep Singh

***Abstract*— With the increasing complexity and operation frequencies of Very Large Scale Integration (VLSI) circuit designs, the power dissipation of VLSI circuits is rapidly increasing, causing high temperature on the chip surface that can lead to variety of reliability problems. Moreover, the power dissipation in testing mode is more than in normal operation. BIST and scan based BIST are used mainly for testing and fault detection. In BIST architecture, linear feedback shift register (LFSR) is used to generate random test vectors and the main source of power dissipation is the transitions between the patterns generated. We need to reduce the switching activity in the pseudorandom test patterns so as to reduce the power consumed. This paper focuses on designing a low power linear feedback shift register to reduce the power dissipation in test mode.**

Index Terms— Built-in-self-test (BIST), Linear feedback shift register (LFSR), power dissipation, scan-based BIST, switching activity, Testing, Very large scale integration (VLSI).

I. INTRODUCTION

With the advancement in technology, the power dissipation is becoming an important issue to be considered while designing the system on chip (SoC). The test power is the prime contributor for this power dissipation. If the power consumed during testing exceeds the power handling capacity of the chip, then chip may get structural degradation or may get damaged. So, there is an intense need of optimizing this power during test mode. Built-In-Self-Test (BIST) is the most recurrently used technique for testing a chip. BIST architecture consists of a Linear Feedback Shift Register (LFSR), Clock, Circuit under Test (CUT) and Output Response Analyzer (ORA) [9]. Linear Feedback Shift Register (LFSR) produces test vector for detection of faults and the transitions between two consecutive patterns and within the patterns are the prime contributor to the power consumed in testing mode:

$$P = 0.5\, V_{DD}^2\, E(sw)\, f_{clk}\, C_L \qquad (1)$$

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Where V_{DD} is supply voltage, E(sw) is the average number of output transitions per 1/ f_{clk}, f_{clk} is the clock frequency and C_L is the physical capacitance at the output of the gate. From the above equation the dynamic power dissipation as in (1) depends on: voltage supplied (V_{DD}), Clock frequency (f_{clk}) and switching activity. Power optimization on the basis of first two parameters effects the circuit performance but power reduction using the switching activity keeps the fault coverage and performance same as in the original technique.

The power dissipation can be classified as:

i) Static Power: Due to leakage current in transistors in steady state.

ii) Dynamic Power: Due to the switching activity.

Many techniques have been implemented and proposed to reduce the dynamic power dissipation. These include scan testing techniques [1] [9], test scheduling algorithms [21], LFSR architecture modifications, correlation driven advancements [11] in BIST structure, low transition test pattern generator. BIST architecture is programmed in VHDL and four different test pattern generators are simulated using Xilinx ISE tools and are compared with each other in terms of switching activity and power consumption.

Rest of the paper is organized as following: Section II describes the BIST architecture, Section III gives an overview of different LFSR architectures, Section IV defines a low power technique integrated in LFSR to optimize power and Section V concludes the paper with simulation results.

II. BUILT-IN-SELF-TEST

A. BIST Architecture

Built in self test is a design for testability in which the elements of circuit are used to test the circuit itself. In circuit testing, either the circuit can be tested using all the possible combinations of inputs or only the necessary vectors that can predict the faults in the circuit. We call such vectors to be Test Vectors that are capable of detecting the faults in the circuit. BIST has linear feedback shift register for generating random test patterns and whenever test vectors are generated there is a lot of switching that takes place in LFSR itself. So we need to reduce this switching activity as it directly relates to the dynamic power of the circuit [5].

A typical BIST architecture consists of a Test Pattern Generator: usually a linear feedback shift register (LFSR), Output response Analyzer (ORA): implemented as a multiple

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input signature register (MISR) and a BIST control unit (BCU).

Different components of BIST architecture are:

a) Circuit under test (CUT): This part is the circuit that is to be tested in BIST mode. It can be a combinational circuit or a sequential circuit. Their primary output (PO) and primary input (PI) delimit it.

b) Test Pattern Generator (TPG): It is a dedicated circuit for generating pseudo random test patterns or deterministic test patterns. The patterns generated by TPG are given to CUT for testing.

c) Multiple input signature register (MISR): Signature register efficiently match different input streams with different signatures with a very less probability of alias.

d) BIST Controller unit (BCU): It manages TPG, ORA and reconfigures the CUT, thereby controlling the execution of test activity. It is activated by Normal/Test signal and generates a Go/ No go signal.

e) Output response analyzer (ORA): It analyses the sequence on primary output (PO) and compares it with the expected value.

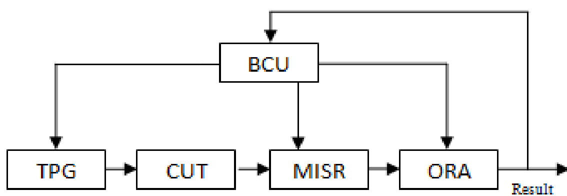

Fig. 1. BIST architecture

Different architectures are possible using the components listed above and it is very important to choose an appropriate linear feedback shift register (LFSR) as it defines the fault coverage and is responsible for power consumed by the circuit [2].

III. LFSR Architectures

Usually a linear feedback shift register (LFSR) is used to generate the pseudo random patterns to be used as test vectors in testing the circuit under test (CUT) [7]. LFSR is an arrangement of flip flops, in which some of the inputs and outputs are added in modulo-2 addition to provide the input to the register. The Overall output of LFSR acts as a Test Pattern. There are two ways to implement LFSR:

- Internal LFSR
- External LFSR

A. Internal LFSR

For an internal feedback LFSR, the feedback from the last FF is the input to the first FF of the shift register and all the taps are XORed with the feedback to modify the input to the next FF in the shift register as illustrated in Fig. 2.

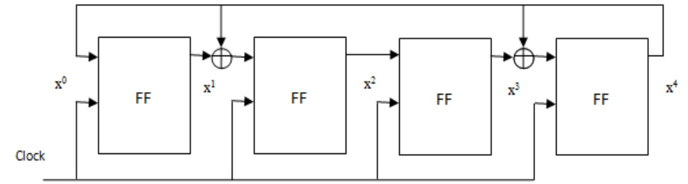

Fig. 2. Internal LFSR

Depending upon the number of bits we have equal number of flip flops in LFSR and output of register can be expressed as a characteristics polynomial P(x).

The characteristics polynomial for the LFSR shown in figure 2 is:

$$P(x) = x^0+x^1+x^3+x^4;\ n=4 \quad (2)$$

where n is the degree of the polynomial and it also defines the number of nodes/bits of LFSR.

B. External LFSR

Same as the internal LFSR, external LFSR is interconnection of the flip flops to form a shift register for generating test patterns [10]. In an external feedback LFSR these taps are in the feedback path and the input to the shift register is the XOR of all the taps.

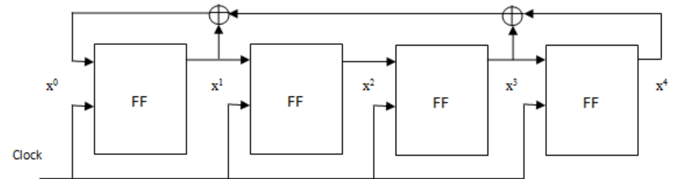

Fig 3. External LFSR

The characteristics polynomial for the external LFSR shown in figure 3 is same as in internal LFSR but the patterns generated by the internal and external LFSR are entirely different.

IV. Cellular Automata

Cellular automata (CA) consist of a collection of cells/nodes formed by flip-flops which are logically related to their nearest neighbors using XOR gates [2]. When the value of a node is determined only by two neighboring cells the CA is known as one-dimensional linear CA. The logical relations which relate a node to its neighbors are known as *rules* and they define the characteristics of a CA.

A. CA Rule 90

In CA rule 90 the flip flops are arranged to produce more random patterns as compared to an LFSR. The Relation between different flip flops is:

$$X_i(t+1) = X_{i-1}(t) \text{ xor } X_{i+1}(t) \quad (3)$$

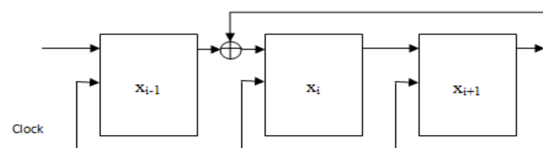

Fig. 4. CA Rule 90

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B. CA Rule 150

In CA rule 150, in addition to previous and next flip flop outputs, output of present flip flop is also feed back to calculate the next stage output [15]. This further increases the randomness of the patterns generated by LHCA150. The relation between different flip flops is defined as:

$$X_i(t+1) = X_{i-1}(t) \text{ xor } X_i(t) \text{ xor } X_{i+1}(t) \quad (4)$$

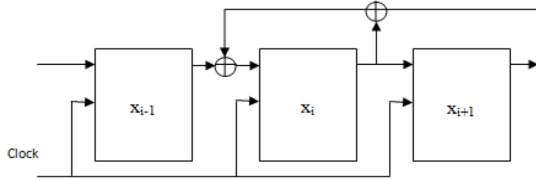

Fig. 5. CA rule 150

V. Low Power Technique

There are so many testing methods available for different circuits. These available test techniques are evaluated using area overhead, fault coverage, test application time and test development time. Now power consumption should also be taken into account. There can be many reasons of power consumption in test mode. The major one is the switching activity which increases the dynamic power consumption of the circuit [20]. So we need to minimize this weighted switching activity (WSA) so as to reduce the power consumption [17].

A. Optimization rule

To concatenate the two 4 bit outputs of multiplexer we have applied basic GA rules of mutation and crossover. As in mutation, the basic principle is to swap the bits within in a pattern mutually and in crossover, we take to patterns and we insert the pattern between the two patterns as shown in figure 6. Bit invert technique as an optimizing rule has provided considerable reduction in power consumption as compared to 8 bit LFSR. In this technique mutual swapping of the bits within the patterns is performed. The resultant pattern generated by this helps in reducing the switching activity which in turn decreases the dynamic power consumption.

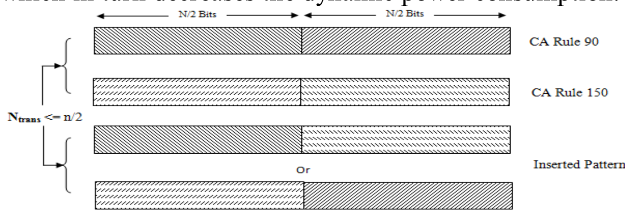

Fig. 6. Pattern insertion

B. Proposed Lower Power Hybrid CA

Many techniques have been proposed and implemented in the literature to reduce the power consumption of VLSI circuits [14], [19]. However, most of these methods focus on the power consumption during normal mode operation, while test mode operation has not normally been a predominant concern. It has been found that the power consumed during test mode operation is often much higher than during normal mode operation. So, the present work focuses on reducing the switching activity between the patterns generated in test mode.

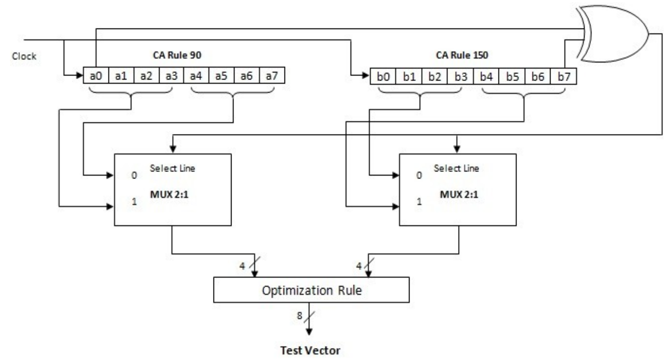

Fig. 7. Low power Hybrid CA-TPG

Figure 7 shows the architecture of proposed scheme in which the patterns generated by two CA registers i.e. CA Rule 90 and CA rule 150 based registers are given to MUX 2:1 so as to concatenate the two into one patterns depending upon the status of select lines. The status of these select lines changes randomly with each generated patterns so the proposed architecture maintains the randomness required for sufficient fault coverage in test mode. Technique proposed in this paper is an integration of both the CA rules into one test pattern generator and this proposed scheme has proved to reduce the power consumption by 14.4 % for 8-Bit test pattern generator (TPG).

VI. Result And Conclusion

Implementation of the proposed design is done in Xilinx 14.1 and results are obtained. Xpower Analyzer is used to calculate the switching activity and dynamic power dissipation. The results are obtained for external LFSR and proposed hybrid-CA. Table 1 shows the comparison of the two for dynamic power and total power consumed as done for 50 patterns.

TABLE I. Comparison of Power Consumption in External LFSR and LP-Hybrid CA

Power	External LFSR	LP-Hybrid CA
V_{ccint} (V)	1.8	1.8
V_{cco25} (V)	2.5	2.5
Quiescent Power (mW)	76	76
Dynamic Power (mW)	21	7
Total Power (mW)	**97**	**83**

Figure 8 shows the graph plotted between the dynamic power and total power consumed in each case. Quiescent (static) power for both the designs is same whereas the dynamic and total power reduces considerably.

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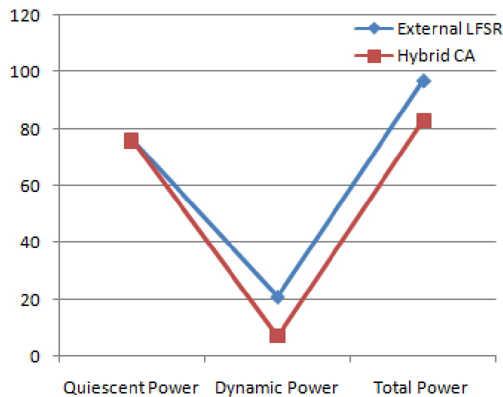

Fig. 8. Comparison of power consumed in test mode of External LFSR and Hybrid CA

It is observed that the total power consumed in Hybrid CA register is 14.43 % less than the power consumed in External LFSR. It is concluded that if this proposed Hybrid CA can be made to generate test vectors in BIST applications it can reduce the power consumed in test mode. Moreover, as Cellular Automata is used in this architecture so it maintains the randomness of the test vectors which in turns gives us considerable fault coverage.

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