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A Novel Methodology to Implement Viterbi Decoder Using FPGA

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Abstract: **Bandwidth and power is the most important parameter in every communication system. So the maximum utilization of bandwidth and minimum useful usage of power is achieved with error detection and correction methods. In satellite &space communication channel capacity is degraded as a result of Additive White Gaussian Noise, which are mostly random. Convolutional encoder with Viterbi decoder is a random error correction method with small constraint length and memory. Viterbi algorithm is a dynamic programming method which maintains the reliability and allows transmission of information quickly and accurately. Without retransmission it will provide maximum accuracy and reliability with low power consumption. It reduces error probability to almost closer to theoretical bounds, so it can be use maximum bandwidth for our application. FPGA acts as memory for the working of Viterbi decoder which adds design flexibility and adaptability with optimal device utilization. It conserving the system power, speed and board space.**

Key Words: **High Speed, Low Power, Convolutional Encoder, Viterbi Decoder**

I. INTRODUCTION:

Viterbi encoding is widely used for satellite and other noisy communication channels. A Viterbi encoder includes extra information in the transmitted signal to reduce the probability of errors in the received signal that maybe corrupted by noise. In digital communication system encoding and decoding are an important part of the system. Digital signal is input to the encoder, which encodes the message. The encoded message is transmitted through the transmitter after modulation and multiplexing. The Receiver receives this message which after demultiplexing and demodulation is input Maximum likelihood decoding is used in Viterbi decoding section, thus applying maximum likelihood to the convolutionally encoded bits is performed in the context of choosing the most likely sequence. Hard decision using hamming distances is applied in the decoding process for evaluation of data transmitted message at the receiver. This decoding must be very efficient and error-free otherwise the original message would be destroyed. The original message might get distorted on the way to receiver due to noise. It must be corrected by some means to get the correct message. The Viterbi Algorithm is perform as a maximum likelihood decoding.

II. Viterbi Decoder

A Viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using Forward error correction based on a code. It consists of three blocks: BMU, SMU and ACSU that is shown in figure 1.

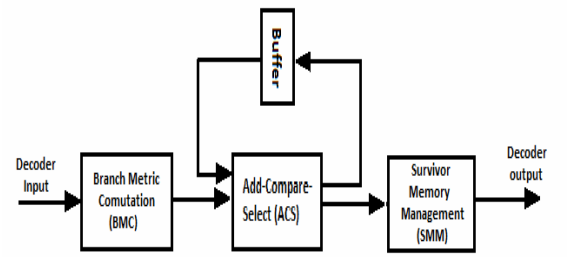

Fig.1.Viterbi Decoder

Thus, the most optimal path through the trellis is the path with the minimum Hamming distance.

1. Branch Metric Unit

Received data symbols are compared to the ideal outputs of the encoder from the transmitter and branch metric is calculated is shown in figure 2. Euclidean distance or Hamming distance is used for branch metric computation.

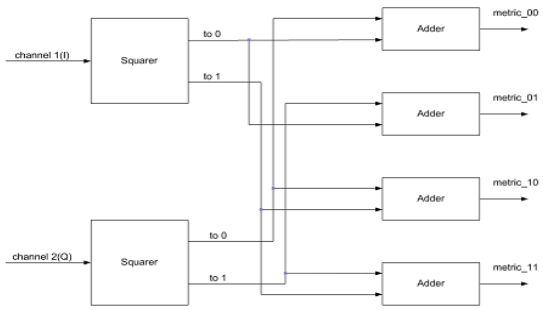

fig 2. Branch Metric Unit

2. Add Compare Select

ACS is also known as a Butterfly module as shown in fig.3. This structure contains a pair of origin and destination states, and four interconnecting branches.ACS unit adds BM (Branch Metric) to partial path metric to lower and upper state metric.

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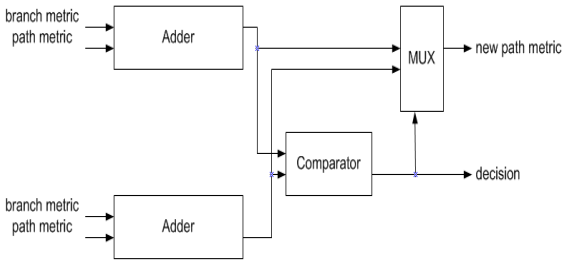

fig 3.Add Compare Select

3. Path Metric Unit

Path metric unit, calculating the path metrics of a stage by adding the branch metrics, associated with a received symbol, to the path metrics from the previous stage of the trellis is shown in figure 4.

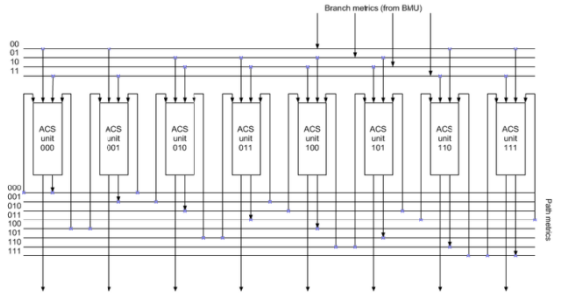

fig4. Path Metric Unit

4.Trace Back Method

Each individual survivor is written into a memory position that corresponds to its state. The write pointer moves forward through the memory as the ACS unit moves on to each new stage in the code trellis. The trace back unit is shown in figure 5.

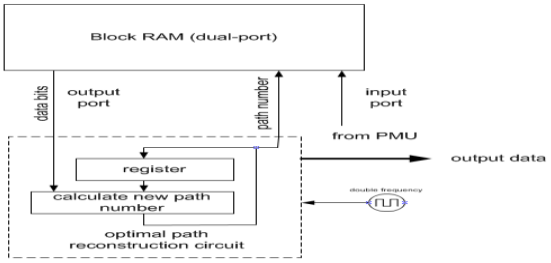

fig 5. Trace Back Method

5. Survivor Memory Unit

The Survivor Memory Unit receives the bit decision from the PMU. This will producing the decoded sequence. After it will perform the trace back module with SMU.

6. Register Exchange Method

The register-exchange method shown in figure 6 eliminates the need to trace back since the register of the final statecontains the decoded output sequence.

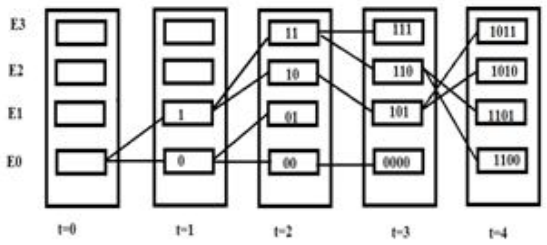

Fig 6.Register Exchange Method

The survivor pathinformation is applied to the LSB of each register and all of the registers perform a shift left operation at each stage to make room for the next bits.

III.PLATFORM FOR THE IMPLEMENTATION

FPGA is used as the platform. Advantages of the FPGA are Flexibility, Better area utilization, High Performance and Low Cost . These parameters are better while comparing with DSP and ASIC processor, Higher sampling rate than DSP It adds design flexibility and adaptability with optimal device utilization conserves both board space and system power.

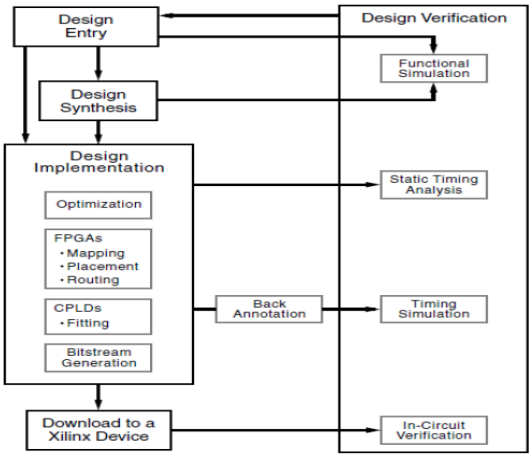

fig 7.Xilinx Design Flow

IV.RESULT AND DISCUSSION

1.SIMULINK CIRCUIT OF VITERBI DECODER SYSTEM

The simulink circuit of the proposed system consist of Bernoulli binary generator, BER, Convolutional encoder, BPSK modulator&demodulator AWGN channel, Error rate calculation circuit, Quantizer, Viterbi decoder, Display and scope is shown in figure 8 and the output shown in figure 9.

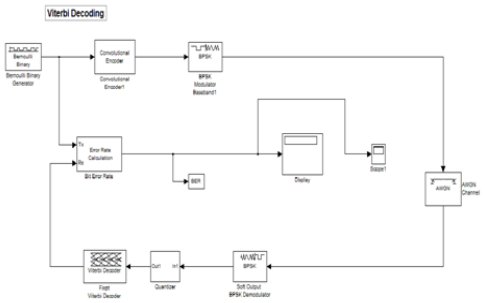

fig 8. Simulink Circuit Of Viterbi Decoder System

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2.CONVOLUTIONAL ENCODER WITH VITERBI DECODER

This figure.9 shows how to use a convolutional encoder and decoder in a simulation of a communications link. It also shows the error correcting capability of convolutional codes. This demonstrates the convolutional trellis generator, convolutional encoder and Viterbi decoder. It also demonstrates the use of functionalities such as rectangular pulse, BITERR, Barcoding, AWGN, MODEM, and PSKMOD.

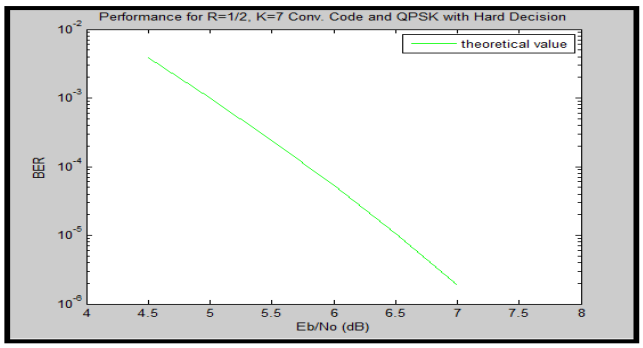

Fig.9 Performance for R=1/2, K=7convolutional Code QPSK with Hard Decision

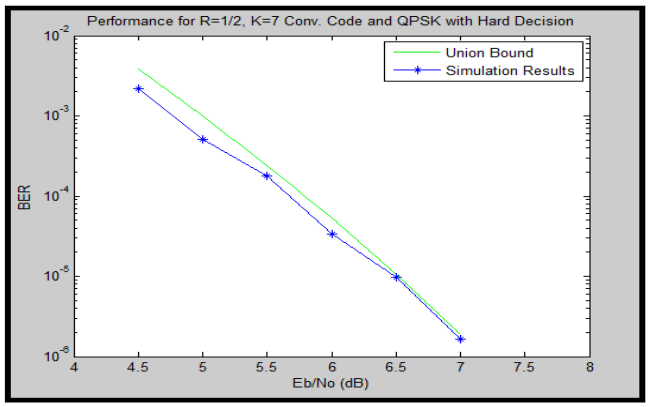

Fig.10 Comparison Of Theoretical And Practical Performance for R=1/2, K=7convolutional Code QPSK with Hard Decision

The figure 10 shows thathow to simulate a QPSK communication system, and compares the error correction capabilities of convolutional encoding with the union bound performance estimates shown here.From the variation of theoretical value and practical value of the BER versus Eb/N0 (Db) get the clear idea about convolutional encoder with viterbi decoder.It almost shows the practical value nearly equal to the theoretical value.Use poly2trellis to generate the trellis of convolutional encoder with G= [171 133]. Calculate the distance spectrum with DISTSPEC, and the BER upper bound with Bar coding.

3 .BINARY SYMBOLS BEFORE CONVOLUTIONAL ENCODING

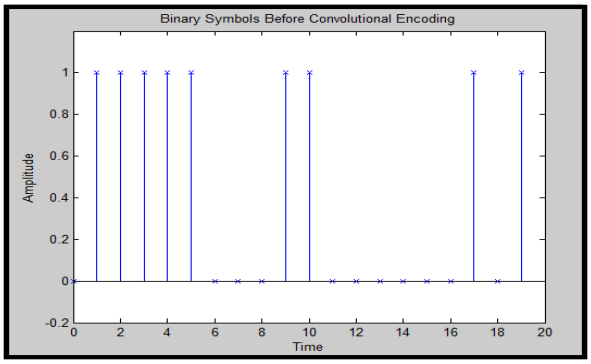

Fig 11 Binary Symbols Before Convolutional Encoding

Setting parameters needed for the simulation. Then generate binary data using Bernoulli generator. Create a new random number stream with a known seed, so only the result can repeat. The first 20 points of this data are plotted here to use convolutional encoder to encode the information symbols. It is shown in figure 11.

4 .BINARY SYMBOLS AFTER CONVOLUTIONAL ENCODING

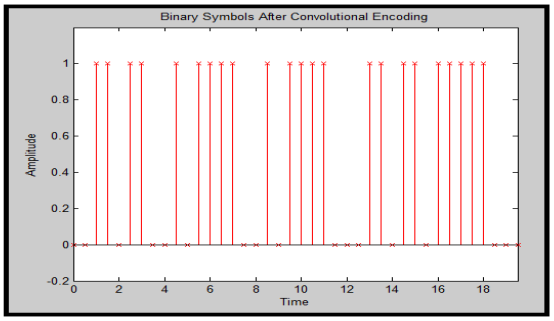

fig.12Binary Symbols After Convolutional Encoding

The figure 12 shows that the encoded symbol rate is twice the information symbol rate.Because some redundancy is added with the data to achieve accuracy.

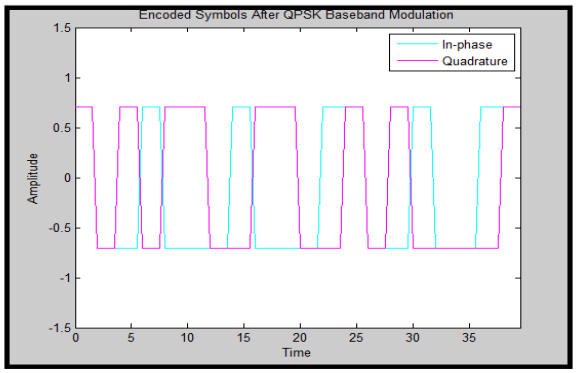

Fig.13.Encoded Symbols After Qpsk Baseband Modulation

Figure 13 shows that the carrier signal is added with original signal and quandrature phase shit keying will transfer the data with low power about 5 dB less power than other modulation method.

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5.DEMODULATED SYMBOLS BY QPSK DEMODULATOR

By using QPSK demodulator ,demodulates the signal to get encoded information on the receiver side.It is sown in the figure 14.

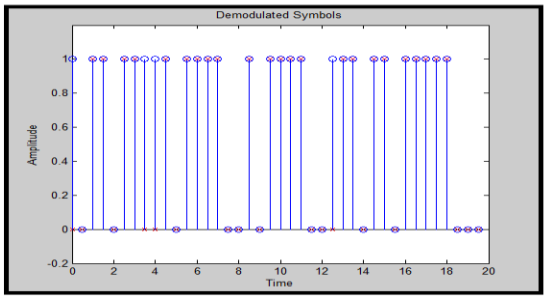

Fig.14 Demodulated Symbols

6.DECODED DATA BY VITERBI DECODER

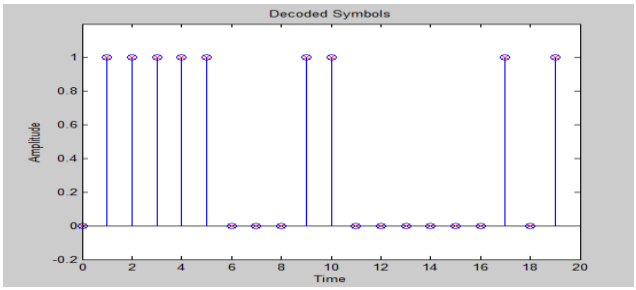

Fig.15. viterbi decoded symbols

The viterbi decoder will decoded the demodulated signal to get the original signal is shown in figure 5.10.

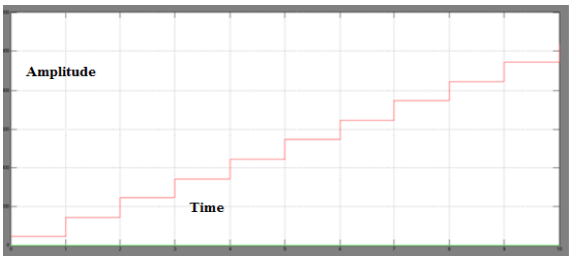

fig 9. Input Signal error rate calculator

7. POWER CALCULATION FROM THE MODELSIM PROGRAM

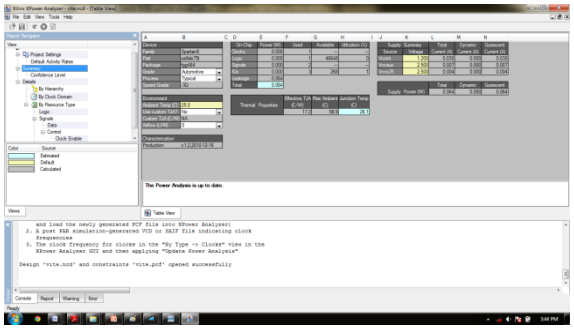

fig 10 .Power Calculation From The Modelsim Program

By writing a program in verilog HDL and simulating in modelsim provided an output of the 20 mW very low power consumption for the decoding. This is highly desirable and it is the best option for satellite communication.

V. CONCLUSIONS

Viterbi decoder on FPGA to improve design with a constraint length of 3 and a code rate of ½.Viterbi Algorithm allows safe data transmission via error correction and original message can be recovered accurately without any noise. The power consumption for the execution of the Viterbi decoding system is very low and it will give decoded output within the minimum time. Along with high speed it also maintains reliability. It provides low power decoder design with in minimum time.

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