

Implementation of Discrete frequency synthesizer based GMSK communication system on FPGA

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Abstract— Gaussian Minimum Shift Keying is a digital modulation technique. It is implemented on Spartan3E FPGA board. The Gaussian filter, which shapes the input pulse, is implemented using distributive algorithm. It is used to implement FIR filter efficiently with ROM Look up table method. The sampling frequency at the output of Gaussian filter will be 8 khz. The FM modulator is implemented using discrete frequency synthesizer. The DFS generates carrier at around 71 khz. Cascaded integrator-comb filter is used to implement decimator and interpolator. The CIC interpolator increases the sampling frequency to 240 khz. CIC decimator at the receiver side reduces the sampling frequency to 8 khz. FM demodulator detects the Gaussian data from the decimated output. Since The DFS is used to generate carrier frequency. The advantage of DFs is, its frequency, phase and amplitude can be controlled using its parameter. The use of distributive algorithm and discrete frequency synthesizer results in reduced area. Since multiplication is avoided using distributive algorithm, hence delay is also reduced.

Index Terms—Gaussian, GMSK, DFS, Distributive algorithm .

I. INTRODUCTION

Gaussian Minimum Shift keying is continuous phase modulation technique. In band-limited applications, it is desirable to employ a pulse whose spectrum drops sharply in the adjacent channel. In other phase shift keying methods due to rectangular pulse, abrupt changes arise in modulated waveforms leading to wide spectrum. This then interferes with other adjacent channels. This consideration warrants the use of “Continuous phase modulation scheme”. Minimum shift keying is a continuous modulation scheme. MSK does not encode rectangular pulses; instead each consecutive rectangular pulse is multiplied with half sinusoidal wave. So, MSK exhibits sharper decay in its spectrum than rectangular pulse. This smooth phase change reduces signal power in the side lobes but at cost of widened main lobe. The phase transitions can be made further smooth by low pass filtering the rectangular pulse before modulating with the carrier. This can be done by using Gaussian Filter because it has sharp cut-off narrow bandwidth.

II. GMSK TRANSMITTER

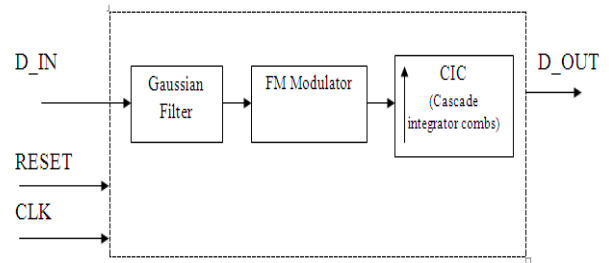


Fig 2.1 GMSK Transmitter [1]

a) GAUSSIAN FILTER

The Gaussian filter transfer function is given by

$$H(f) = \exp(-\alpha^2 f^2) \quad 1$$

Where α is 3db bandwidth. Given by Bandwidth*symbol time (B*Ts):

$$\alpha = \frac{\sqrt{\ln(2)} T_s}{\sqrt{2} B T_s} \quad 2$$

As α increases the impulses response widens and interferes with adjacent channel.

Impulse response of Gaussian filters in time domain is given by:

$$h(t) = \frac{\sqrt{\pi}}{\alpha} \exp\left[-\left(\frac{\pi}{\alpha} t\right)^2\right] \quad 3$$

Gaussian filter impulse response in discrete-time domain given by:

$$h(kt_0) = \frac{\sqrt{\pi}}{\alpha} \exp\left[-\left(\frac{\pi}{\alpha} kt_0\right)^2\right] \quad 4$$

Where $t_0 = T_s / OSR$, $t = kt_0$.

OSR=Oversampling rate.

k =Sample index

Substituting 2 in 4 and dropping explicit dependence on t_0 .

$$h[k] = \underbrace{\frac{\sqrt{2\pi}}{\sqrt{\ln(2)}} \frac{BT_s}{T_s}}_{h_{max}} \exp \left[- \left(\frac{\sqrt{2\pi}}{\sqrt{\ln(2)}} BT_s \frac{k}{OSR} \right)^2 \right] \quad 5$$

Where h_{max} given by first term in the equation 5.

For Bluetooth $BT_s=0.5$ and $T_s=1\mu s$ we obtain $h_{max}=1.5MHZ$
 For GSM $BT_s=0.3$ and $T_s=3.62\mu s$ we obtain $h_{max}=244.62KHZ$.

b) DISTRIBUTIVE ALGORITHM:

Distributive algorithm is an efficient technique in implementing DSP functions. DA eliminates the use of multiplier in the design, which is required in the implementation of Finite Impulse Response filter [3]. DA uses Look-Up table to store the filter coefficients and it uses input samples as address to the Look-Up tables. Depending upon the sample values corresponding coefficients are selected from Look-Up tables and added to get final filter output.

$$y = \sum_{k=1}^K A_k X_k \quad 6$$

A_k =Constant filter coefficients.

X_k =Input Samples.

y =Out response.

X_k be expressed in 2's complement form.

$$x_k = -b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \quad 7$$

Substituting equation 7 in equation 6

$$y = \sum_{k=1}^K A_k \left[-b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \right] \quad 8$$

Rearranging equation 8

$$y = - \sum_{k=1}^K b_{k0} \cdot A_k + \sum_{k=1}^K \left[\sum_{n=1}^{N-1} (b_{kn} \cdot A_k) 2^{-n} \right] \quad 9$$

Rearranging the summation based on power terms and then grouping the sum of the products [4]:

$$y = - \sum_{k=1}^K A_k \cdot b_{k0} + \sum_{n=1}^{N-1} \left[\sum_{k=1}^K A_k \cdot b_{kn} \right] 2^{-n} \quad 10$$

c) FM MODULATOR:

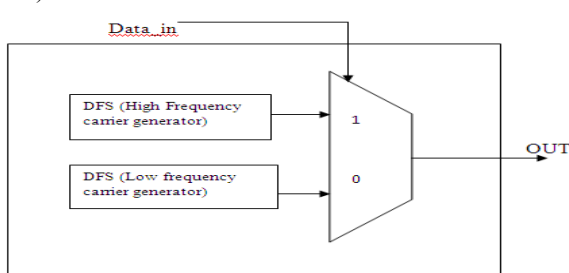


Fig 2.2 Fm modulator

Frequency modulator uses discrete frequency synthesizer to modulate the carrier.

d) DISCRETE FREQUENCY SYNTHESIZER:

Digital frequency synthesizer is used to generate a sampled sinusoidal wave in many DSP tasks. DFS has advantage that the its output frequency, phase and amplitude can be precisely and rapidly controlled. DFS also has the ability to tune with extremely fine frequency and phase resolution and to rapidly “hop” between the frequencies [5].

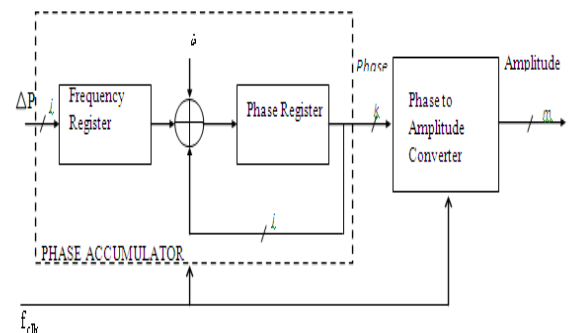


Fig 2.3 DFS[5]

DFS is shown in figure. It consists Frequency register which holds ΔP (frequency control word). Phase accumulator, its output is feedback to be added with ΔP (frequency control word). The output of phase register is converted to sine value using sine Look-Up table.

$$f_{out} = f_{clk} \times \frac{\text{frequency control word}}{2^N} \quad 11$$

Where f_{out} =Desired Output frequency.

N =number of bits of phase accumulator.

e) CASCADED INTEGRATOR COMB:

The two basic building blocks of a CIC filter are an integrator and a comb. An integrator is simply a single-pole IIR filter with a unity feedback coefficient [4]:

$$Y[n]=Y[n-1]+X[n] \quad 12$$

It is also called accumulator.

A comb filter running at the high sampling rate, f_s , for a rate change of R is an odd symmetric FIR filter described by:

$$Y[n]=X[n]-X[n-RM] \quad 13$$

Where M is differential delay. Usually $M=1$ or 2 .

Difference equation of CIC interpolator is given by:

$$Y[n]=X[n]-X[n-RM]+Y[n-1] \quad 14$$

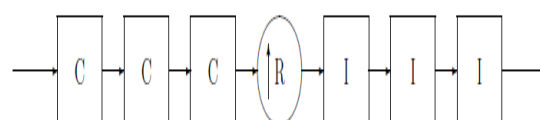


Fig 2.4 CIC Interpolator [4]

III. GMSK RECEIVER

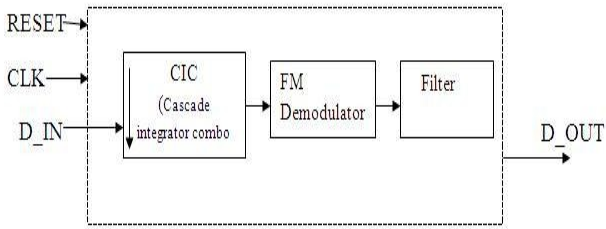


Fig 3.1 GMSK RECEIVER [1]

In receiver side the CIC filter is used as Decimator. It reduces the sample rate to filter sample rate. The FM demodulator decodes the filtered data from the carrier signal. FM demodulator output is filtered to get final original data.

a) CIC DECIMATOR

Cascaded integrated comb filter is implemented as decimator by integrating the received data and then passing it through the comb filter.

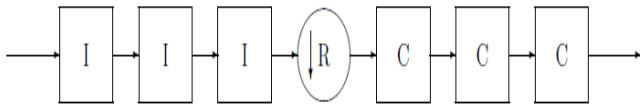


Fig 3.2 CIC Decimator [4]

IV. SIMULATION RESULTS

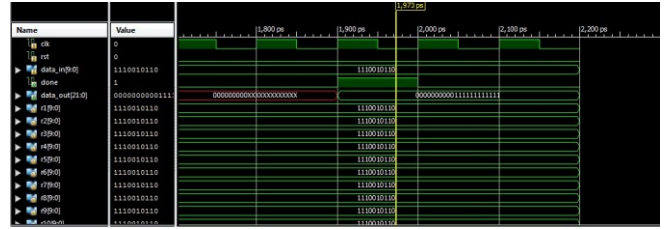


Fig 4.1 SIMULATION OF GAUSSIAN LOW PASS FILTER

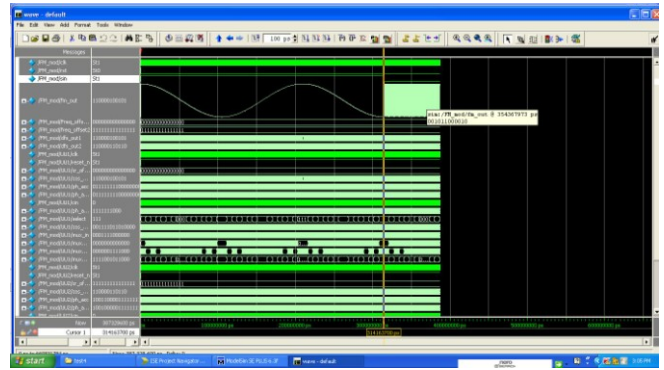
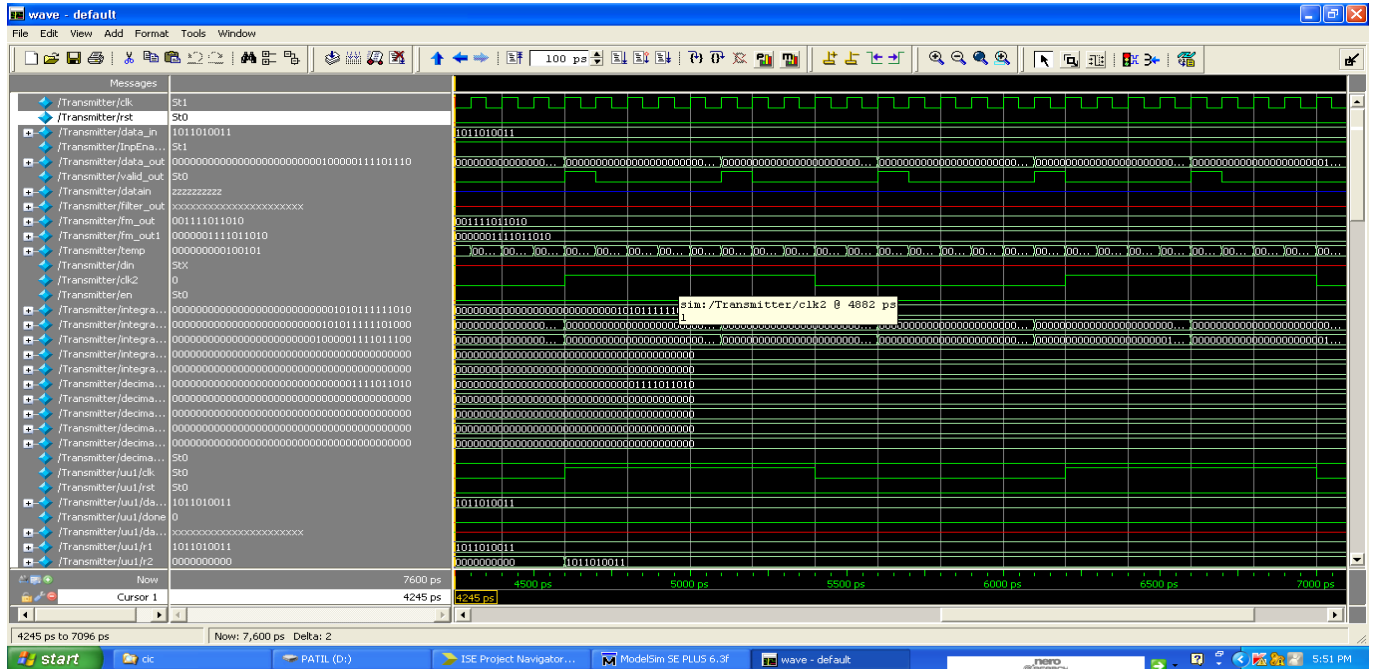


Fig 4.2 SIMULATION of FM modulator

Fig 4.3 SIMULATION of GMSK system



V. CONCLUSION

A Gaussian minimum shift keying communication system has been implemented using distributive algorithm and discrete frequency algorithm. Distributive algorithm uses look-up tables to store filter coefficients.

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