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Offset voltage Analysis of Latched Comparator

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Abstract:
Comparator is one of the most widely used building block for analog and mixed signal systems. The implementation of dynamic latch comparator provides high speed, less power dissipation, having zero static power consumption and also provides full-swing digital level output voltage in shorter time duration. Back to back inverter in these dynamic comparators provides positive feedback mechanism which converts a smaller voltage difference in full scale digital level output. In this paper, dynamic comparator offset is determined to the extent of high accuracy. In addition to the offset, propagation delay and power dissipation, being the important parameter of the comparator to be analyzed.

Keywords: Latched Comparator, Analog to digital converter, Double Tail Comparator, Rail-to- rail comparator

I. INTRODUCTION

In Today's electronics era Comparators are the basic building blocks in an Analog to Digital Converters. The basic operation in an analog-to-digital Converter (ADC) is to perform comparison between analog signals. The input comparisons are performed by Dynamic latched comparator. Dynamic latched comparator works synchronously with all the clock and outputs a digital signal, based on comparison of given input signals.

Latched comparators use regeneration mechanism which regenerates (amplifies) the analog input signal into a Full-scale digital level output signal [1]. The Dynamic latched comparators have an important role in high speed Analog to digital converters. The speed, power consumption, delays and offset plays an important role in the designing of the comparators. Instead of using the traditional amplifier-chain type comparators and to obtain a low power dissipation and better speed the dynamic comparators are mostly preferred [2].

However, an offset voltage, resulting from the transistor mismatches such as threshold voltage Vth, current factor μCoxW/L and the internal node Capacitances and output load capacitances variations, deteriorates the accuracy of these comparators [3], [4]. Because of the above mentioned points, the input-referred offset voltage is also the important parameters of the design CMOS comparator.

To meet the specifications such as offset voltage and power dissipation in a limited area, it is necessary to fully understand the correlations between sizes of transistors. Conventionally, the latch offset voltage can be reduced by using a pre-amplifier preceding the regenerative latch stage. The major disadvantage or drawback of using a Preamplifier based comparators is that they provide huge static power consumption from the reduced intrinsic gain with a reduction of the drain-to source resistance rds due to the continuous technology scaling.

II. BASIC DYNAMIC LATCH

Dynamic latch is composed of two inverters connected in a closed loop. Figure 1 presents the dynamic latch circuit schematic. It works as follows, when Vout+ increases (Vout decreases), transistor M2 will increase the current drawn from the Vout- node, decreasing its voltage. Consequently, the transistor M1 will reduce the gate to source voltage, Vgs, thus decreasing the current through M1, which causes the voltage at node Vout+ to increase. The PMOS transistors have the same function as the NMOS transistors. The benefit of using the combination of a PMOS transistors and NMOS transistors latches is a 25% time constant reduction compared to its single regeneration counterpart [5]. To meet high speed requirements, transistors should have small sizes to keep parasitic capacitances as small as possible. This, in the addition of the threshold voltage offset variation, introduces errors in the offset voltage that hamper the accuracy of the comparator. To reduce the effect of the offset voltage, a preamplifier is incorporated to the comparator.

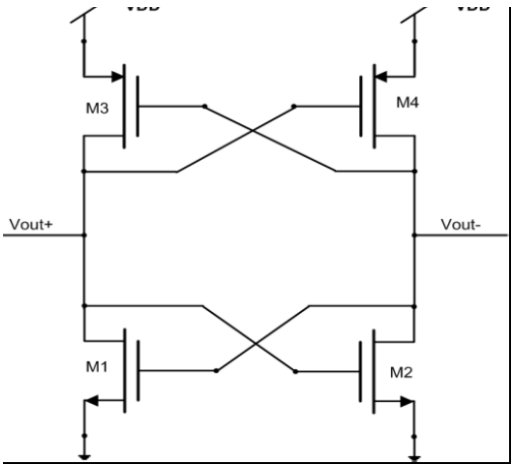

Fig.1. Basic latch comparator

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Offset in the Dynamic Latch

The offset voltage of the dynamic latch can be expressed as

$$V_{offset} = \Delta V_{th} + \frac{1}{2}\left(\frac{\Delta w}{w} - \frac{\Delta L}{L}\right) - (V_{gs} - V_{th}) + \frac{\Delta Q}{CD} \qquad (1)$$

where ΔV_{th} represents the standard deviation of the threshold voltage, ΔW/W is the width dimension mismatch, ΔL/L is the length dimension mismatch, V_{gs}- V_{th} is the overdrive voltage at the beginning of dynamic latch regeneration phase, ΔQ is the charge due to the switches controlling nodes Vout+ and Vout-, and C_D denotes the total equivalent capacitance in the output nodes of the dynamic latch. Also, can be expressed as:

$$\sigma(V_{TH}) = \frac{A_{VTH}}{\sqrt{WL}} \qquad (2)$$

Here, A_{VTH} is a technology dependent factor measured in V·μm.

Analyzing (1) and (2), suggests that the width and length of the transistors should be increase in order to soothe the effect of device mismatch. However, the increase of area will increase parasitic capacitance. Hence, the speed will be downgraded.

III. CONVENTIONAL DOUBLE TAIL DYNAMIC COMPARATOR

A dynamic latched comparator with lower offset voltage and higher load drivability has two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator; the gain preceding the regenerative latch stage is improved. The complementary version of the regenerative latch stage, which provides larger output drive current, is provided.

IV. CONVENTIONAL LATCHED COMPARATOR

Fig. shows a widely used standard conventional latch type comparator circuit with the high impedance input, rail to rail output swing and no static power consumption. Robustness against noise and mismatch are the main advantages of the conventional latch type comparator. However, it suffers from high sufficient power supply, which is caused by many stacked transistors in circuit design.

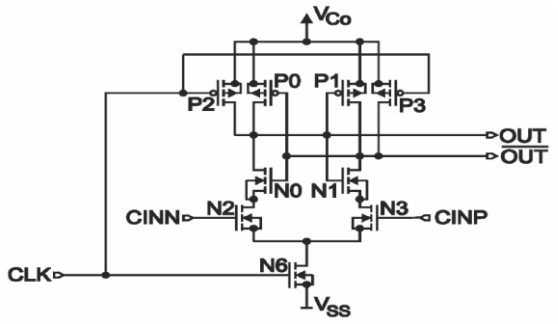

Fig.2. Conventional latched comparator

A part from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity.

V. COMPARISON

In this paper, simulated results are presented for offset voltage & propagation delay of various latches Comparator .The summary of the comparison is given in the Table I.

Comparator	Input offset voltage (mv)	Power dissipation (μW)	Propagation delay (ps)	Speed (GHz)
Preamplifier based comparator	16.6	102.5	104.1	9.6
Dynamic comparator	13	19	987.5	1.012
Double tail latch type	30.3	64.7	996.8	1.003

Table I-Simulated results of different latch comparators

VI.OFFSET ERROR OPTIMIZATION

To minimize the offset error due to mismatches in the components present in the latched comparator shown on figure 1, an offset cancellation negative feedback-loop circuit has been added. The modified latched comparator circuit is shown in figure 3. This comparator works in three different phases: offset cancellation phase, tracking phase and latching phase. In the offset cancellation phase, clkb becomes high and clk becomes low which causes transistor 21 and 22 on bringing the offset cancellation block into action. The offset cancellation feedback-loop consists of a differential pair with active load. Its common mode voltage is set by resistive common mode feedback R1 and R2. When clkb moves to logic low with clk at logic low state, offset cancellation phase stops.

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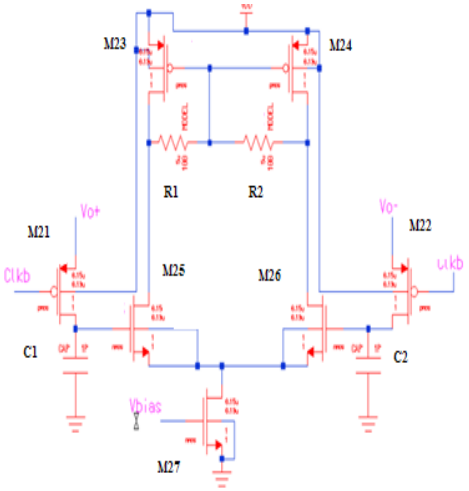

Fig. 3 Offset cancellation block

VII. CONCLUSION

The implementation of dynamic latch comparator is required for high-speed analog-to-digital converters to get faster signal conversion & low offset voltage. In this paper, dynamic comparator offset is determined to the extent of high accuracy

Among the comparators studied the dynamic comparator which has a back to back latch stage has the lowest power dissipation. Also it has less

speed and input offset voltage compared to the pre-amplifier based comparator.

VIII. REFERENCES

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