

Effective Modelling of higher order Sigma Delta - ADC using MATLAB - Simulink for multibit Quantizer

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Abstract—The requirement of effective analog to digital conversion and accuracy gives growth to converters. The Sigma Delta Modulator have a salient feature of shaping the noise, such that noise reduces from the band of interest resulting in high accuracy in comparison to other converters and high tolerance to non idealities of analog circuits. The significant advantage of the method is that conversion of analog signals can be performed by using only a 1-bit ADC and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter. This paper presents an effective simulink model of fifth order sigma delta modulator for the input frequency 20 KHz, OSR equal to 64, and at the quantization level of 16. The SDM is designed using CIFB topology with all the gain values to be 1, for keeping the conditions more likely to be with practical implementation conditions. The effect of different OSR is observed on the parameters like signal to noise ratio and effective number of bits.

Index Terms—SDM: Sigma delta modulator, SNR: Signal to Noise Ratio, DR: Dynamic Range, ENOB: Effective Number of bits.

I. INTRODUCTION

In the present era, the processing in digital domain provides high accuracy, high efficiency, less chip area, better simulation options etc. Sigma Delta Modulator has proved their sound presence in applications as communication systems, audio systems, and precision measurement decision etc. SDM is also vital building block in RFID application. [1] As per the sampling frequency, ADC are classified into two categories : Nyquist ADCs and Sigma-Delta ADCs .Sigma Delta Modulators achieve a high degree of insensitivity to analog circuit imperfections, thus making them a good choice to realize embedded analog-to-digital interfaces. [2][3] They have not been very successful in high-speed high-bandwidth applications. Modern society relies on signal processing. The vital feature of this converters are ,they provide high dynamic range and flexibility in converting low bandwidth input signals with very low costing. It is applied in communication equipment, medical devices, automated production facilities, computers, weapons, navigation

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equipment, tools etc.[4] The first step performed by a signal-processing system is to convert a considered signal into a form that can be processed by an electronic circuit. Sometimes a dedicated electro-mechanical system (called a sensor) will be required to sense the signal and convert it into a voltage, charge or current signal, and sometimes the signal is readily available in one of these forms. The signal processing that needs to be performed can vary from very simple operations (e.g. amplification) to extremely complex ones involving computation of several parameters, such as standard deviation, spectral composition, correlation coefficients, etc.[5][6] A fundamental property of analog electric signal processing is that each operation will be associated with a degradation of the signal-to-noise ratio (SNR). Hence, if substantial analog signal processing (ASP) is performed, stochastic artifacts (noise) will accumulate, and the resulting signal may not represent the desired signal with the required significance. This work focuses almost exclusively on delta-sigma modulation as chosen technique for A/D and D/A conversion. Based on the combination of oversampling and quantization error shaping techniques,[7] $\Delta\Sigma$ Ms achieve a high degree of insensitivity to analog circuit imperfections, thus making them a good choice (the best one in many cases) to realize embedded analog-to-digital interfaces in modern systems-on-chip (SoCs) integrated in nanometer CMOS[3]. In spite of all the above mentioned advantages , this modulator have some practical issues and trade off related to power consumption, silicon area etc, which must be taken into account for optimized performance. The paper is organized as follows Section 2 gives the overview of different blocks of SDM, Section 3 provides the realization of fifth order SDM, Section 4 provides the SNR Value and effective number of bits for different Oversampling ratios and at quantization level = 16, Section 5 provides the Conclusion on the basis of comparison.

II. BASICS OF SIGMA DELTA MODULATOR

A. Over Sampling

In signal processing, over sampling is the process of sampling a signal with a sampling frequency significantly higher than twice the bandwidth or highest frequency of the signal being sampled. Oversampling helps avoid aliasing, improves resolution and reduces noise. Oversampling is the process of increasing the sampling frequency by generating new digital samples based on the values of known samples.

Over sampling Factor: An oversampled signal is said to be oversampled by a factor of β , defined as

$$\beta = f_s / 2B \quad (1)$$

or $f_s = 2 \beta B$

where:

- f_s is the sampling frequency
- B is the bandwidth or highest frequency of the signal; the Nyquist rate is $2B$.

B. Quantization and Quantization Error

Discretization in amplitude domain of any continuous signal is said to be Quantization. This continuous-to-discrete transformation in amplitude generates an error, commonly referred to as quantization error. The quantization itself introduces a fundamental limitation on the performance of an ideal ADC. It degrades the quality of the input signal whose continuous-value levels are mapped onto a finite set of discrete levels

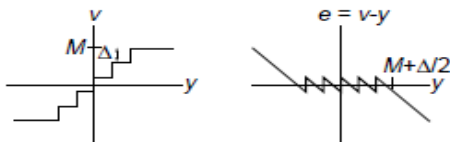


Fig. 1. Quantization process. (a) Ideal characteristic. (b) Quantization error.

Fig. 1(a) shows the transfer characteristic of an ideal quantizer, where e stands for the quantization error. This error is a nonlinear function of the input signal, as shown in Fig. 1(b). Note that, if x is confined to the full-scale input range $[-XFS/2, XFS/2]$, the quantization error is bounded by $[-\Delta/2, \Delta/2]$, with Δ being the quantization step, defined as the separation between adjacent output levels in the quantizer. As long as the quantizer does not overload $|e| \leq \Delta/2$. The number of quantization levels is large, then the quantization noise is white with a power $\sigma_e^2 = \Delta^2/12 = 1/3$ for $\Delta=2$.

C. Noise Shaping

The accuracy of Oversampling ADC / DAC can be increased by applying methods to reduce quantization noise. A method in which the inband noise is pushed in the frequency out of interest. Such a phenomena is called Noise Shaping, where the quantization error conceptually generated by the difference of the input signal, from an analog version of the quantizer output, is shaped by a filter with a transfer function, usually called noise transfer function (NTF), which can be either of high-pass type or band-stop type. In case low pass oversampled signal, the low frequency inband component the removal of quantization Noise can be done through Differentiator in z domain transfer function is given by :

$$NTF(z) = (1 - z^{-1})^L \quad (3)$$

Where L denotes the order of filter.[6]

D. Collectively: Sigma Delta Modulator

A Sigma Delta Modulator contains feedback loop, containing a loop filter which is in the forward path of the loop. Replacing as before the quantizer by its linear model, the linear sampled-data system of Fig. results.

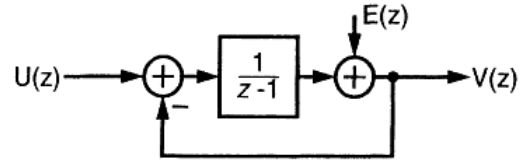


Fig 2: Sigma Delta Modulator: Linear model in z - domain (used as an ADC)

Analysis gives

$$v(n) = u(n-1) + e(n) - e(n-1).$$

Thus, the digital output contains a delayed, but otherwise unchanged replica of the analog input signal u , and a differentiated version of the quantization error e . The differentiation of the error e suppresses it at frequencies which are small compared to the sampling rate f_s . In general, if the loop filter has a high gain in the signal band, the in-band quantization "noise" is strongly attenuated, a process now commonly called noise shaping.

If the quantizer is having 2^N level and separated by Δ . The signal to noise ratio is given as:

Mean Squared value : $(2^{N-1} \Delta)^2 / 2$ and

Mean Squared Noise: $\Delta^2 / 12$

Therefore,

$$SNR = (2^{N-1} \Delta)^2 / 2 / \Delta^2 / 12 = 1.5 \cdot 2^{2N}$$

SNR (in dB) = $6.02 N + 1.76$ dB

Effect of oversampling on SNR can be viewed mathematically as

Mean Squared value: $(2^{N-1} \Delta)^2 / 2$ and

Mean Squared Noise: $\Delta^2 / 12 / OSR$

Therefore,

$$SNR = (2^{N-1} \Delta)^2 / 2 / \Delta^2 / 12 / OSR = 1.5 \cdot 2^{2N} \cdot OSR$$

SNR (in dB) = $6.02 N + 1.76$ dB + $10 \log OSR$

which signifies that increase in OSR will increase the SNR by 10 times the logarithmic OSR value.

III. REALIZATION

Fifth order Sigma Delta Modulator is realized using MATLAB [7], by providing the input parameters as OSR = 64, Quantization Level = 16 by the usage of specifically DelSig Toolbox. Figure 3 (a) shows the Time domain analysis of fifth order SDM, Figure 3 (b) shows the Frequency domain analysis of fifth order SDM. Figure 3 (c) shows the integrator states of fifth order SDM

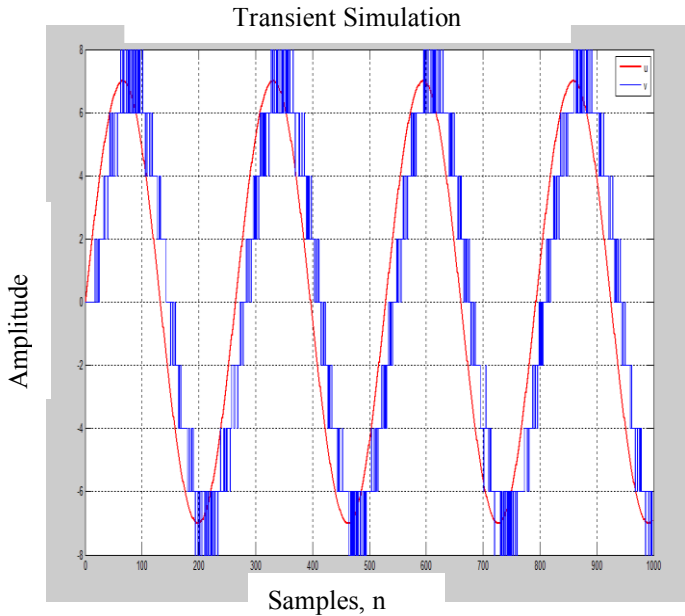


Figure 3(a) Time domain simulation of fifth order SDM

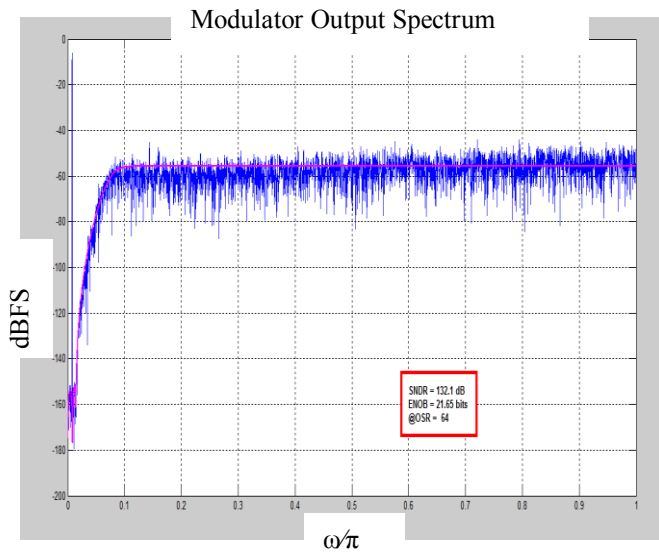


Figure 3 (b) Frequency domain analysis of fifth order SDM

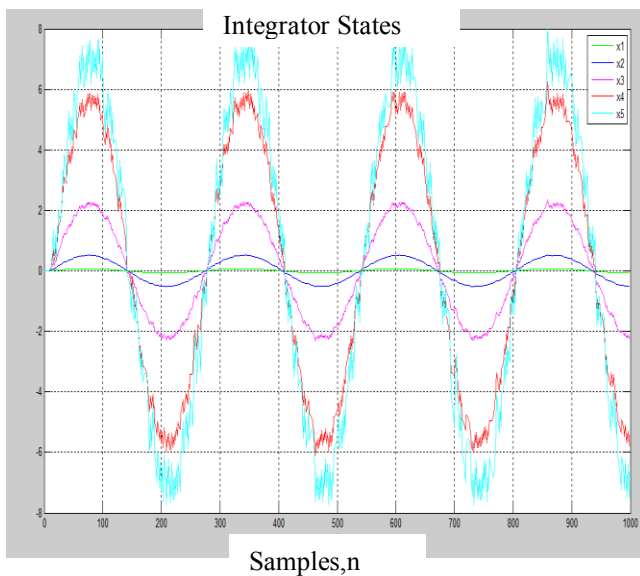


Figure 3 (c) Integrator States of fifth order SDM

The fifth order Sigma Delta Modulator is also analyzed using Simulink. Figure 3 (d) shows the circuit layout of fifth order SDM in Simulink. Figure 3 (e) shows the analog input signal and output signal of fifth order SDM. Figure 3 (f) shows the circuit layout of second order SDM in Simulink. Figure 3 (g) shows the analog input signal and output signal of second order SDM.

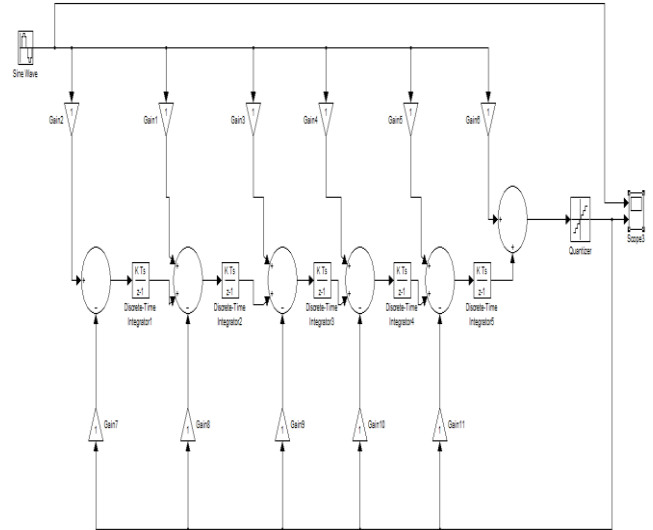


Figure 3 (d) Circuit layout of fifth order SDM in Simulink

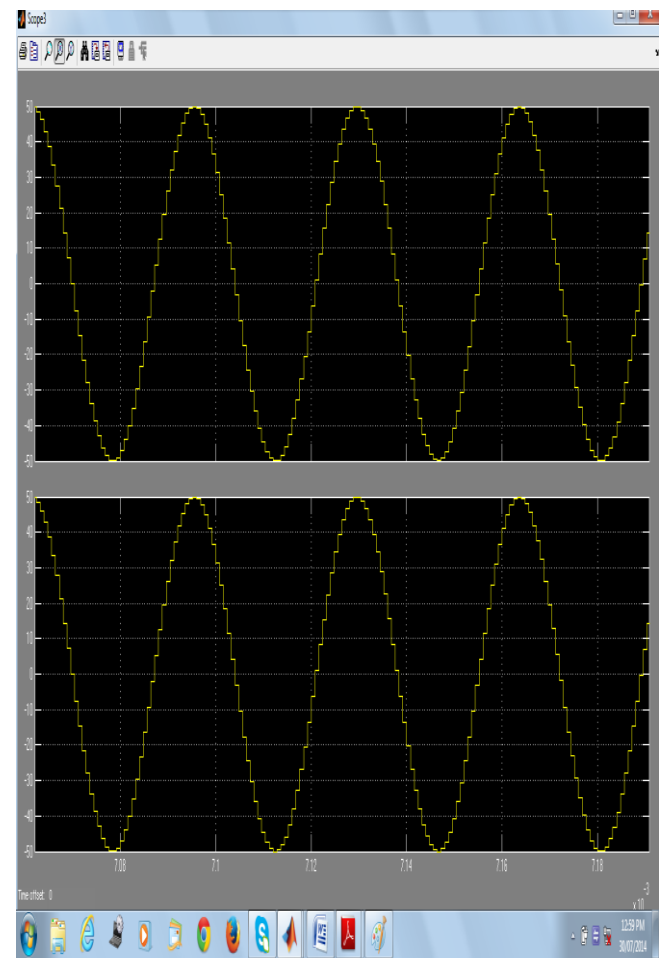


Figure 3 (e) the analog input signal and output signal of fifth order SDM.

IV. SNR VALUE AND EFFECTIVE NUMBER OF BITS FOR FIFTH ORDER OF SIGMA DELTA MODULATOR

The essential performance parameter of sigma delta modulator that are signal to noise ratio and effective number of bits are analyzed for different OSR ranging from 2 to 128, for the quantization level 16. Comparative table is drawn showing the fifth order sigma delta modulator SNR value and effective number of bits for different OSR at quantization level 16, with optimized zeros. Table 1 shows the variation of SNR and effective number of bits in fifth order modulator for quantization level = 16 .

Table 1 : Variation in SNR Value and Effective number of bits for different order at quantization level 16

Sr. No	OSR	5TH Order	
		SNR (in dB)	ENoB
1	2	13.7	1.98
2	4	20.0	3.04
3	8	39.1	6.21
4	16	66.2	10.70
5	32	100.3	16.37
6	64	132.1	21.65
7	128	150.3	24.67

V. CONCLUSION

This paper concludes that by sampling theorem and quantization theory, sigma delta converter grossly oversamples the input signal and shapes the noise spectrum such that the modulator appears to be a high pass filter for the noise and a low pass filter for the input signal. Stability of the modulator is higher in the lower order but SNR and ENoB achieved is low. For achieving high signal to noise ratio, higher order Sigma Delta modulator can be used but the stability criteria has to be considered. For stability Signal Transfer Function should be kept maximally flat and Noise Transfer Function should be selected so to provide higher stability to the system. Also, by using multi bit quantizer the output of the modulator can be obtained with high resolution, but the practical realization of the quantizer is tough. So mostly single bit quantizer is used.

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