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DESIGN & IMPLEMENTATION OF LOW POWER FULL ADDER CELL USING POWER GATING TECHNIQUES FOR MOBILE APPLICATIONS

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Abstract— **For the foremost recent CMOS feature sizes (e.g., 180nm), run power dissipation has become Associate in Nursing paramount concern for VLSI circuit designers. As technology scales into the nano meter regime run power and noise immunity are getting vital metric of comparable importance to active power, delay and space for the analysis and style of complicated arithmetic and logic circuits. During this project, low run 1-bit full adder cells square measure projected for mobile applications. Noise immunity has been rigorously thought-about since the numerous threshold current of the low threshold voltage transition becomes additional vulnerable to noise. Since, Adders square measure heart of process circuits and plenty of complicated arithmetic circuits square measure supported the addition. The huge use of this operation in arithmetic functions attracts plenty of researcher's attention to adder for mobile applications. In recent years, many variants of various logic designs are projected to implement 1-bit adder cells. thus a brand new junction transistor resizing approach for 1-bit full adder cells to work out the optimum sleep transistor size that scale back the run power has been projected. The simulation results depicts that the projected style conjointly results in economical 1-bit full adder cells in terms of standby run power. so as to verify the run power, numerous styles of full adder circuits square measure simulated exploitation DSCH, small wind.**

Index Terms—**Low run power; Noise Margin; Ground bounce noise; Sleep transistor; Sleep technique; Stack method; twin stack method and Adder cell**

I. INTRODUCTION

Adder's square measure heart of procedure circuits and lots of advanced arithmetic circuits square measure supported the addition. The large use of this operation in arithmetic functions attracts plenty of researcher's attention to adder for mobile applications. In recent years, many variants of various logic designs are projected to implement 1-bit adder cells. These adder cells unremarkably aimed to cut back power consumption and increase speed. These studies have additionally investigated totally different approaches realizing adder's exploitation CMOS technology. For mobile applications, designers got to work among a really tight outpouring power specification so as to satisfy product battery life and package value objectives. The designer's concern for the extent of outpouring current isn't associated with guaranteeing correct circuit operation, however is expounded to reduce power dissipation. For moveable electronic devices this equates to increasing battery life. for instance, mobile phones have to be compelled to be high-powered for extended periods (known as standby mode, throughout that the phone is ready to receive associate degree incoming call), however square measure absolutely active for abundant shorter periods (known as speak or active mode, whereas creating a call). once associate degree device like a movable is in standby mode, sure parts of the electronic equipment among the device, that square measure active once the phone is in speak mode, square measure finish off. These circuits, however, still have outpouring currents running through them, even supposing they need been de-activated. albeit the outpouring current is way smaller than the traditional in operation current of the circuit. The outpouring current depletes the battery charge over the comparatively long standby time, whereas the in operation current throughout speak time solely depletes the battery charge over the comparatively short speak time. As a result, the outpouring current includes a disproportionate impact on total battery life. This can be why building low outpouring adder cells for mobile applications square measure of nice interest. Shortening the gate length of a semiconductor device will increase its power consumption thanks to the multiplied outpouring current between the transistors supply and drain once no signal voltage is applied at the gate. Additionally to the sub threshold outpouring current, gate tunneling current additionally will increase thanks to the scaling of gate compound thickness. Every new technology generations results nearly a 30x increase in gate outpouring. The outpouring power is anticipated to achieve over five hundredth of total power in sub 100nm technology generation. Hence, it's become extraordinarily necessary to develop style techniques to cut back static power dissipation in periods of inactivity.

The power reduction should be achieved while not trading-off performance that makes it tougher to cut back outpouring throughout traditional (runtime) operation. On the opposite hand, there square measure many techniques to cut back outpouring power. Power gating is one such accepted technique wherever a sleep semiconductor device is supplemental between actual ground rail AND gate ground (called virtual ground). This device is turned off within the sleep mode to cut-off the outpouring path. It's been shown that this method provides a considerable reduction in outpouring at a minimal impact on performance and any peak of ground bounce noise is feasible with projected novel technique with improved staggered part damping technique.

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so as to attain high density and high performance, CMOS technology feature size and threshold voltage are reducing for many years. due to this technology trend, semiconductor device outpouring power has multiplied exponentially. because the feature size becomes smaller, shorter channel lengths end in multiplied subthreshold outpouring current through a semiconductor device once it's off. Low threshold voltage additionally leads to multiplied subthreshold outpouring current as a result of transistors cannot be turned off utterly. For these reasons, static power consumption, i.e., outpouring power dissipation, has become a major portion of total power consumption for current and future chemical element technologies. There square measure many VLSI techniques to cut back outpouring power. every technique provides associate degree economical thanks to scale back outpouring power, however disadvantages of every technique limit the applying of every technique. we tend to propose a brand new approach, so providing a brand new option to low-leakage power VLSI designers. Previous techniques square measure summarized and compared with our new approach bestowed during this project. the arrival of a mobile computing era has become a serious motivation for low power style as a result of the operation time of a mobile device is heavily restricted by its battery life. The growing complexness of mobile devices, like a telephone with a photographic camera or a private digital assistant (PDA) with world positioning system (GPS), makes the facility downside more difficult. Dynamic power consumption was antecedently a serious concern for chip designers since dynamic power accounted for ninety nine or additional of the entire chip power. However, because the feature size shrinks, static power, that consists chiefly of subthreshold and gate-oxide outpouring power has become a good challenge for current and future technologies. the most reason is that outpouring current will increase exponentially because the feature size shrinks. supported the International Technology Roadmap for Semiconductors (ITRS), Kim et al. report that subthreshold outpouring power dissipation of a chip can exceed dynamic power dissipation at the 65nm feature size [1][2]. Techniques for outpouring power reduction will be classified in 2 categories: state-preserving techniques wherever circuit state (present price) is preserved and state-destructive techniques wherever this Boolean output value of the circuitmight be lost [1]. A state-preserving technique has a plus over a state harmful technique in this with a state-preserving technique the electronic equipment will resume operation at some extent abundant later in time while not having to somehow regenerate state. Our new style technique, that we tend to decision the “sleepy stack” technique, retains information throughout sleep mode whereas providing reduced outpouring power consumption at a value of slightly multiplied delay. What is more, the asleep stack approach will be applicable to single- and dual-threshold voltage technologies. The asleep stack approach delivers a brand new option to designers to implement low leakage- power circuits that retain state.

II. Proposed Full Adder Circuits

Recently, power dissipation has become a vital concern and sizable stress is placed on understanding the sources of power and approaches to coping with power dissipation [3].Static logic vogue offers hardiness against noise effects, thus mechanically provides a reliable operation. Pseudo NMOS and Pass-transistor logic will scale back the amount of transistors needed to implement a given logic operates. However those suffer from static power dissipation. Implementing Multiplexers and XOR based mostly circuits ar advantageous once we implement by the pass semiconductor unit logic [4]. On the opposite hand, dynamic logic implementation of advanced operate needs atiny low atomic number 14 space however charge escape and charge refreshing ar needed that reduces the frequency of operation. In general, none of the mentioned designs will vie with CMOS vogue in hardiness and stability [4], [13]. Fig. one shows the standard CMOS twenty eight semiconductor unit adder [12]. this is often thought-about as a Base case throughout this paper. All comparisons ar finished Base case. The CMOS structure combines PMOS pull up and NMOS pull down networks to supply thought-about outputs. Semiconductor unit sizes ar such as a magnitude relation of Width/Length (W/L). The filler of transistors plays a key role in static CMOS vogue. it's determined within the standard adder circuit that the semiconductor unit magnitude relation of PMOS to NMOS is a pair of for Associate in Nursing electrical converter and remaining blocks additionally followed identical ratios once we thought-about the remaining blocks as the same inverters. This magnitude relation doesn't provide best results with regard to noise margin and standby escape power once it's simulated in 90nm method. Changed adder circuits with filler are planned in Design1 and Design2 targeting the noise margin, and ground bounce noise. Further, power gating technique is employed to scale back the escape power, wherever a sleep semiconductor unit is connected between actual ground rail gate ground. Ground bounce noise is being calculable once the circuits ar connected with a sleep semiconductor unit. Further, the height of ground bounce noise is achieved with a planned novel technique.

Modified filler are shown in Fig. 2 and Fig. 4 severally. The tiniest semiconductor unit thought-about for 90nm technology incorporates a dimension of one20nm and a length of 100nm and offers W/L magnitude relation of 1.2. The W/L magnitude relation of NMOS is mounted at one.2 and W/L of PMOS is three.8 that is three.1 times that of NMOS in Design1. The filler of every block is predicated on the subsequent assumption. Changed adder circuit i.e Design2 shown in Fig. 4, the W/L magnitude relation of PMOS is one.5 times that of W/L magnitude relation of NMOS and every block has been treated as the same electrical converter. The goal of this style is to scale back the standby escape power. Additional compared to the bottom case and Design1 and ground bounce noise created once a circuit is connected to sleep semiconductor unit. However, there'll be a small variation on the noise margin levels and is nearly adequate the bottom case.

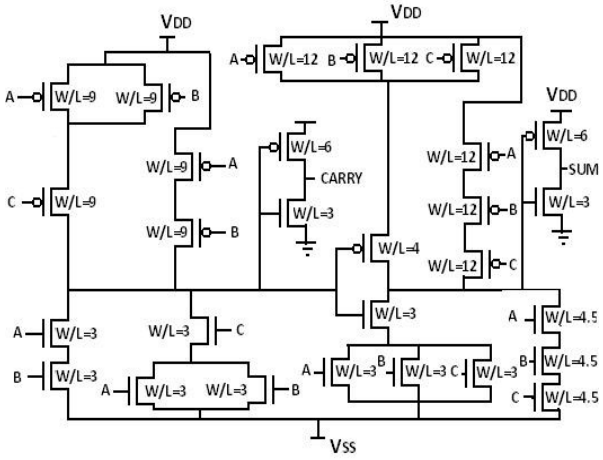

Figure 1. Conventional CMOS full adder

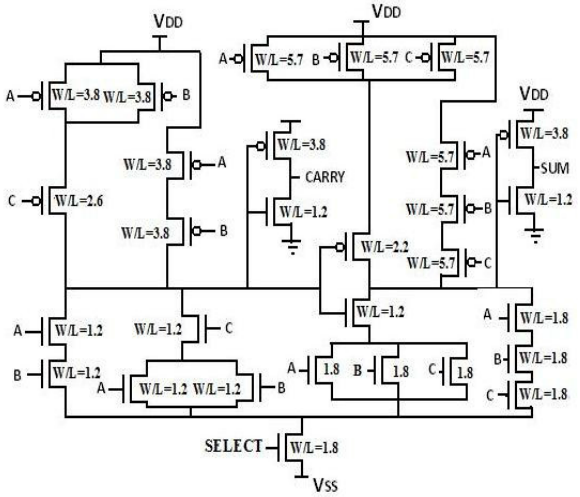

Figure 2. Proposed full adder (Design1) circuit with sleep transistor

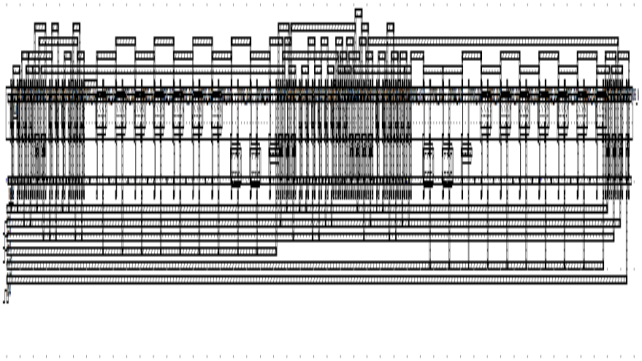

Figure 3. Layout for design-1 full adder circuit

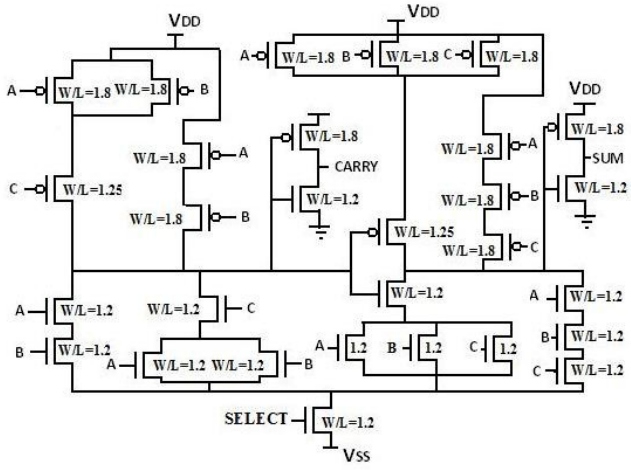

Figure 4. Proposed 1 bit full adder (Design2) circuit with sleep transistor

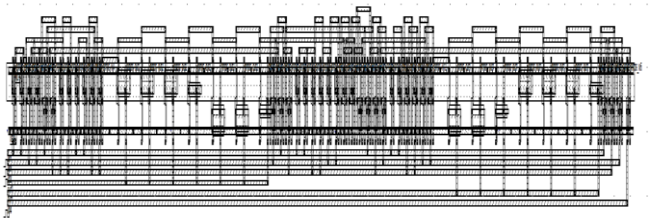

Figure 5. Layout for design-2 full adder circuit

III. SLEEP METHOD

Low power has emerged as a principal theme in today's industry. the necessity for low power has caused a significant paradigm shift wherever power dissipation has become as vital a thought as performance and space. 2 elements verify the ability consumption during a CMOS circuit: Static power: Includes sub-threshold leak, drain junction leak logic gate leak owing to tunneling. Among these, subthreshold leak is that the most outstanding. Dynamic power: Includes charging and discharging power and contact power. once technology feature size scales down, provide voltage and threshold voltage conjointly scale down. Techniques for leak power reduction are often classified into 2 categories: state-preserving techniques; wherever circuit state is maintained and state-destructive techniques; wherever the present mathematician output worth of the circuit could be lost. A state-preserving technique has a bonus over a state harmful technique therein with a state-preserving technique the electronic equipment will resume operation at some extent abundant later in time while not having to somehow regenerate state. the foremost well-known ancient approach is that the sleep approach. within the sleep approach, a "sleep" PMOS junction transistor is placed between V_{dd} and therefore the pull-up network of a circuit and a "sleep" NMOS transistor is placed between the pull-down network and Gnd (Fig.6). These sleep transistors close up the circuit by alienating the ability rails. The sleep transistors square measure turned on once the circuit is active and turned off

once the circuit is idle. By alienating the ability supply, this method will cut back leak power effectively.

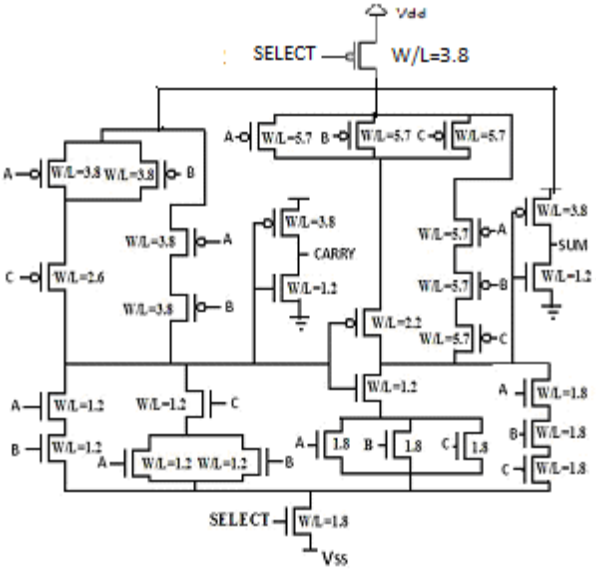

Figure 6. Full Adder circuit using sleep method

IV. Dual Stack Approach

In twin stack approach (Fig.7), two PMOS within the pulldown network and a couple of NMOS within the pull-up network are used. The advantage is that NMOS degrades the high logic level whereas PMOS degrades the low logic level. Sleep transistors within the sleep approach (Fig.6) are sized such any sleep junction transistor| between V_{dd} and a pull-up network takes the dimensions of the biggest transistor within the pull-up network, and any sleep junction transistor between G_{nd} and a pull-down network takes the dimensions of the biggest transistor within the pull-down network. we tend to compare the twin stack approach with Base Case, Design 1, Design 2, Sleep techniques. Thus, we tend to compare 5 style approaches in terms of outpouring power and space.

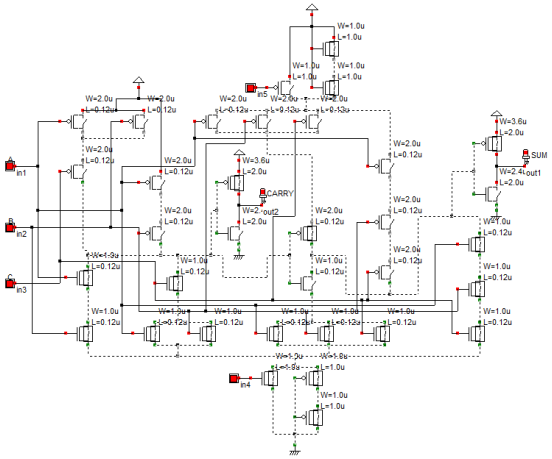

Figure 7. Digital schematic design for full adder circuit using dual-stack method

For example, sleep transistors utilized in the pull-up and pull-down networks of the bottom case electrical converter chain have W/L=6 and W/L=3. Transistors within the stack approach square measure sized to 1/2 the scale of the bottom case transistors, e.g., transistors utilized in pull-up and pull-down of the bottom case electrical converter chain have W/L=3 and W/L=1.5, severally. Similarly, transistors, together with sleep transistors, within the sleepy-eyed stack approach square measure sized to 1/2 the scale of the bottom case transistors.

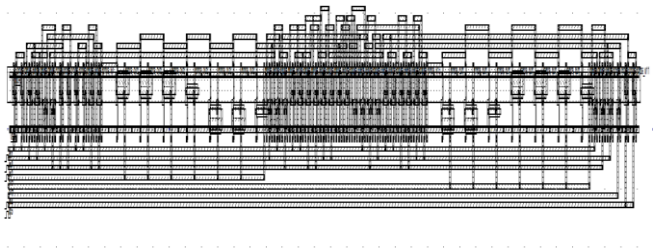

Figure 8. Layout for full adder circuit using sleep method

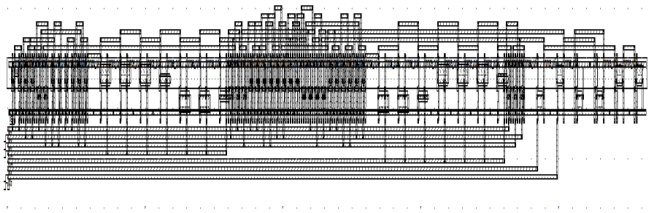

Figure 9. Layout for full adder circuit using dual-stack method

V. Conclusion & Future Work

In this thesis, low discharge one bit full adder cells ar planned for mobile applications with low discharge power. By victimization the planned technique discharge power is reduced by 33%(Design1), 46% (Design2) as compared to the traditional adder cell (Base case). By victimization the novel techniques of sleep technique and dual-stack technique discharge power is additional reduced compared with the essential circuit, design-1 and design-2 circuits as shown within the below tabular column one. in keeping with the necessity wherever space reduction is that the key purpose, sleep technique circuit is enforced as a result of in twin stack technique since every junction transistor is replaced by 2 transistors, the 28T full adder circuit are going to be regenerate in to a 56T excluding the sleep transistors and if sleep transistors are enclosed then it becomes a 58T circuit and if space isn't a matter however power reduction is that the key purpose then, in such cases dual-stack technique is enforced.

Full Adder circuit	Optimized Power	%Power reduction
Base case	0.594mw	-----
Design-1	0.200mw	66.33%
Design-2	93.377uw	82.21%
Sleep method	74.601uw	87.34%
Dual stack method	58.733uw	90.11%

Table-1: Performance characteristics of simulated full adder circuits

In this thesis, we've bestowed alternative ways to cut back the discharge power of one-bit full adder circuits. an equivalent full adder circuit styles i.e., sleep technique and twin stack styles with very little modifications as mentioned below may be accustomed scale back the bottom bounce noise and additional may additionally scale back the discharge power. Throughout last one decade numerous alternatives and enhancements of typical power gating has been planned to cut back the bottom bounce noise throughout mode transition. In staggered section Damping technique [15] throughout standby-to-active power mode transition, staggered-phase damping delays the activation time of 1 of the 2 sleep transistors relative to the activation time of the opposite one by a time that's up to [*fr1] the resonant oscillation amount. As a result, noise cancellation happens once the second sleep transistor activates because of section shift between the noises evoked by the second sleep transistor thence reduction in subsidence time. however it's not terribly effective in reducing the height noise because of the initial spike. And in another theme [17], there'll be a 2 stage procedure. In initial stage sleep {transistor operating as diode by activate the management transistor that is connected across the drain AND circuit of the sleep transistor. because of this, drain to supply current of the sleep junction transistor drops during a quadratic manner. This reduces the voltage fluctuation on the bottom and power web and it conjointly reduces the circuit wakeup time. In second stage management junction transistor is off so sleep transistor works ordinarily. This technique isn't effective to suppress the general fluctuations within the ground bounce noise. Therefore, the technique should be adopted to cut back each peak of ground bounce noise and reducing the general fluctuations within the ground bounce noise. The thought is to mix each the on top of techniques to additional scale back the height of ground bounce noise and overall power mode transition noise within the planned technique.

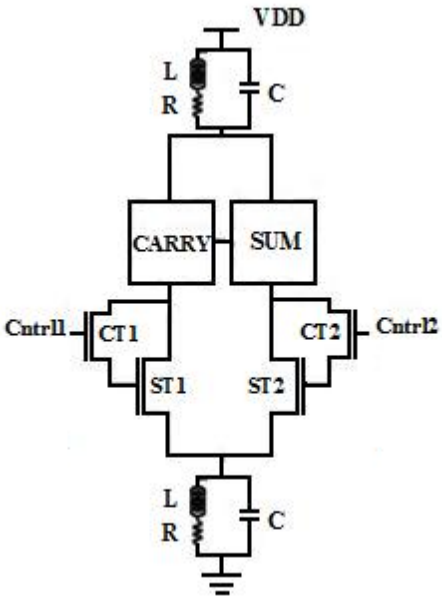

Figure 10. Proposed novel technique for ground bounce noise reduction

Figure10 shows the planned theme for peak of ground bounce noise reduction in mode transition. One bit full adders are going to be taken to use the planned technique. One-bit full adder circuit is taken into account as 2 cascaded blocks i.e. carry generation block and add generation block. Separate sleep transistors are another at rock bottom of the blocks. To summarize, since full adder circuits are designed in 5 completely different ways, every with its own benefits and drawbacks of power, area, etc,. may be used relying au fait the necessity of the designer

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