Implementation of digit serial fir filter using wireless priority service(wps)

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Abstract—**Many efficient algorithms and architectures have been proposed for the design of low complexity fir filter. In order to design the filter a bit-parallel multiple constant multiplication (MCM) operation which dominates the complexity of the digital signal processing ,where the most importance is given to digit-serial MCM design which also offers the low complexity MCM operations instead of increase in delay.In this the main problem is of optimizing the gate-level area in digit-serial MCM design and introduce high level synthesis algorithms and design architectures.The proposed architecture is capable of operating at high-level synthesized algorithms at different word length filter coefficients without any distraction in software.The algorithms The algorithms common sub expression(CSE) and graph based(GB) are solved with many shifters and adders where as wireless priority service(WPS) is solved with very less shifters and less no of adders .Here the WPS algorithm gave very efficient results in less area, less delay and less power .**

Keywords-MCM,FirFilter,GB,CSE and WPS algorithms,0-1ILP

I. INTRODUCTION

In digital signal processing systems FIR filters have great importance. Since their characteristics in linear-phase and feed-forward implementations make them very useful for building stable high-performance filters. Transposed direct form is the usually used computational technique as it offers a high power efficiency and high performance. Full flexibility of a multiplier is not necessary for the constant multiplications. Here only constants are to be multiplied and no floating point multiplication is involved. This is generally known as the multiple constant multiplications (MCM) operation and is also a central operation and performance bottleneck in many other DSP systems such as fast fourier transforms(FFT), discrete cosine transforms (DCTs), and error-correcting codes. Although area, delay, and power-efficient multiplier architectures, such as Wallace and modified Booth multipliers, have been proposed, the full flexibility of a multiplier is not necessary for the constant multiplications, since filter coefficients are fixed and determined beforehand by the DSP algorithms. Hence, the multiplication of filter coefficients with the input data is generally implemented under a shift-adds architecture, where each constant multiplication is realized using addition/subtraction and shift operations in an MCM operation .For the shift-adds implementation of constant multiplications, a straightforward method, generally known as digit- based recoding, initially defines the constants in binary. Then, for each "1" in the binary representation of the constant, according to its bit position, it shifts the variable and adds up the shifted variables to obtain the result. Dynamically reconfigurable filters can be efficiently implemented by using canonical signed digit (CSD) .This is more efficient that other and offer good area and power reductions and speed improvement compare to the best existing.

II. OPTIMIZATION OF AREA AT GATE-LEVEL

The gate-level area of an operation realizing a constant multiplication depends on the type of the operation (addition/subtraction), the bit width of an input of the operation ,the number of shifts in the operation, and the type of the input variable (signed or unsigned) [4]. Thus, a solution with the minimum number of operations does not always guarantee a design with optimal area at gate-level since the algorithms of [1], [2] do not take these parameters into account while optimizing the number of operations.

A.*MCM Operation*

Main objective is to eliminate multiplier block and introducing MCM architecture in digit serial FIR filter for the reduction of multiplication in the form of shift and add operations.

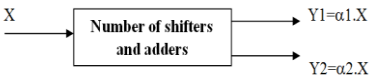
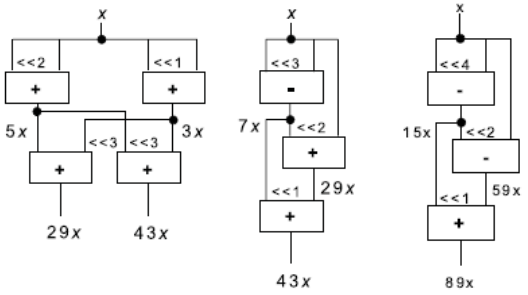


Fig.1 MCM operation

In Fig.1 X denotes input , α1 and α2 are the filter coefficients, Y1 and Y2 are the outputs.An operation with the same input is to be multiplied by a set of coefficients is said to be MCM. Serial input data is multiplied with two pair of coefficients and produces Y1, Y2 outputs

In [4], the gate-level implementation costs of all possible addition/subtraction operations in MCM are introduced under the ripple carry adder architecture. The subtraction operation is implemented using 2's complement. The high-level algorithms, that consider the gate-level implementation cost of

each addition/subtraction operation while synthesizing constant multiplications.



(a) (b) (c)

Fig 1: (a)Exact CSE algorithm,(b)Exact GB algorithm of 29x and 43x ,(c)GB algorithm with partial products of 59x and 89x.

III OPTIMIZATION OF AREA UNDER A DELAY CONSTRAINT

Performance is also a crucial parameter in many DSP systems and circuit area is generally expandable in order to achieve a given performance target. Although the delay parameter is dependent on design architectures and implementation issues, the delay in multiplierless design of constant multiplications is generally considered in terms of the number of adder-steps which denotes the maximal number of adders/subtracters in series.The high-level algorithms of [3], [4] can handle the delay constraint, enabling us to find the tradeoff between area and delay by changing the delay constraint. Moreover, it is shown the power dissipation of constant multiplications depend both on the gate-level area and the depth of each operation in the design.

IV ALGORITHMS WITH MCM ARCHITECTURE

Many algorithms have been proposed with the MCM architecture but they are all not successful in particular operations which are mainly at the shifting operations .

A. EXACT CSE ALGORITHM

A common sub expression elimination algorithm is proposed to minimize the complexity of the multiple constant multiplication operation. The coefficients (constants) of the multiple constant multiplications are represented using the binary signed digit number system. The binary signed digit representations of each coefficient are enumerated using the representation tree. The algorithm traverses the tree to calculate the possible sub expressions at each node. Each sub expression is used to find a possible decomposition for the coefficient to be encoded. A complexity formula is proposed to compare the decompositions. The algorithm is designed to prune the tree when it finds decomposition with minimum complexity. This reduces the search space while minimizing the hardware complexity. Results show that the algorithm has better performance than other published algorithms including linear programming optimization methods. The algorithm outperforms the sub expression sharing method in that uses only the canonical signed-digit representations .

B.EXACT GB ALGORITHM

The GB exact algorithm finds a solution with the minimum number of operations by the sharing the common partial product 7x in both multiplications. However all these algorithms assume that the input data x is processed in parallel. On the other hand, in digit-serial arithmetic, the data words are divided into digit sets, consisting of d bits that are processed one at a time. Since digit –serial operators occupy less area and are independent of the data wordlength; digit-serial architectures offer alternative low complexity designs when compared to bit parallel architectures.

C. WIRELESS PRIORITY ALGORITHM(WPS)

The Wireless Priority Services can be defined as an enhancement to the basic wireless service that allows the National Security/Emergency Preparedness (NS/EP) calls to queue for priority service instead of being blocked. In times of emergency or crisis, the system enables designated WPS users to have a greater chance of being able to complete calls.Not every individual can subscribe for WPS; only NS/EP personnel can benefit from the advantages of WPS. The WPS provides only the qualified and authorizedNS/EP users with means to obtain priority access to the next available radio channel in a wireless call path when emergency calls are placed.

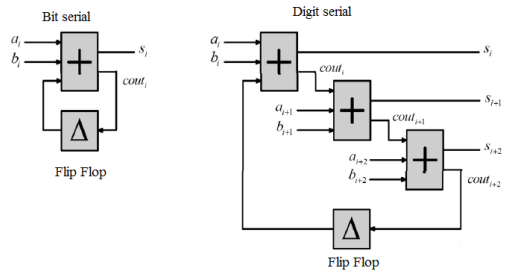


Fig. 2: Digit serial operation using flip flop

Bit serial and Digit serial are the two cases for serial addition. Compared to bit serial operation, Fig.2 explains that Digit Serial operation needs less number of delay elements such as flip flop for addition or subtraction. In digit-serial designs, the input data is divided into d bits and processed serially by applying each d-bit data in parallel. The special cases, called bit-serial and bit-parallel, occur when the digit size d is equal to 1 and equal to input data word length, respectively. The digit-serial computation plays a key role when the bit-serial implementations cannot meet the delay requirements and the bit-parallel designs require excessive hardware. Thus, an optimal tradeoff between area and delay can be explored by changing the digit size d.

CONSTANT VECTOR MULTIPLICATION

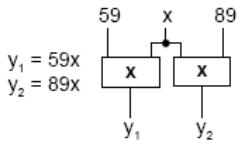


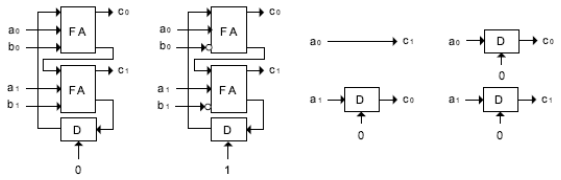
Fig 2.1 multiple constant vector matrix

Multiplication of data samples with constant coefficients is a ubiquitous operation and performance bottleneck in Digital Signal Processing (DSP) systems such as, digital Finite Impulse Response (FIR) filters and linear DSP transforms.

C.FORMALIZATION OF 0-1 ILP

The Linear-Programming models that have been discussed thus far all have been continuous, in the sense that decision variables are allowed to be fractional . The implementations of constants are represented in terms of a Boolean network. Third, the gate-level area optimization problem is formalized as a 0–1 ILP problem with a cost function to be minimized and a set of constraints to be satisfied. Finally, a set of operations that yields the minimum area solution is obtained using a generic 0–1 ILP solver.At other times, however, fractional solutions are not realistic, and that must consider the optimization problem. The feasible integer points are shown , in dashed lines indicate their convex hull, which is the smallest polyhedron that contains all of these points. The dot lines together with the coordinate axes define the polyhedron of the LP relaxation, which is given by the inequalities without the integrity constraint. The goal of the optimization is to move the black dotted line as far upward while still touching the polyhedron.

V OPTIMIZATION OF AREA IN DIGIT-SERIAL MCM DESIGN



III. (B) (C) (D)

Fig 2:The digit-serial operation when d is equal to 2 (a)addition operation,(b)substraction operation,(c)left shift by 1 time (d) left shift by 2 times.

In digit-serial designs, the input data is divided into *d* bits and processed serially by applying each *d*-bit data in parallel. Since digit-serial operators occupy less area and are independent of the data wordlength, the digit-serial architectures offer alternative low-complexity designs when compared to bit-parallel architectures. The digit-serial digit-serial MCM design. Thus, the optimization algorithms should

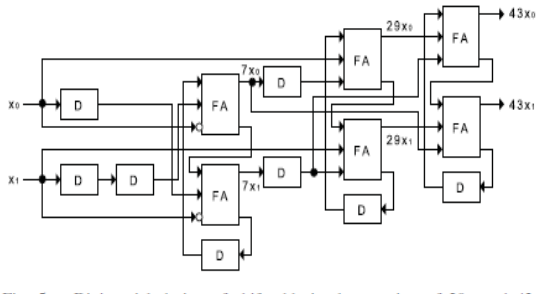


Fig 3.Digit serial arithematic operation

take into account the sharing of shift operations as well as the sharing of addition/subtraction operations.Since each digit-serial operation has a different implementation cost at gate-level, the high-level algorithms of [6],[7] consider the gate-level area optimization in digit-serial MCM designs by sharing the addition/subtraction and shift operations.

VI COMPUTER-AIDED DESIGN TOOL

This section initially presents the design of a digit-serial MCM operation under the shift-adds architecture. Then, a generic digit-serial constant multiplier architecture adapted from , which is used for an alternative digit-serial realization of the MCM block and for comparison with the shift-adds architecture in Section VI, is introduced. Finally, the design process of a digit-serial FIR filter is presented. In SAFIR, all the circuits are described in VHDL, and a commercial synthesis tool is used to design these circuits.

VII COMPARISON

Algorithms		
CSE	1.area(mm^2) 2.delay(ps) 3.power(nw)	397.06 927 316
GB	1.area(mm^2) 2.delay(ps) 3.power(nw)	179 912 310
WPS	1.area(mm^2) 2.delay(ps) 3.power(nw)	379.21 956 292

Table :1 Comparisons between CSE GB and WPS

The above table:1 shows the comparison among CSE,GB and WPS algorithms. From the table it is observed that, GB algorithm is an efficient technique for filter implementation where area is the major concern. By using WPS algorithm the power dissipation is less when compared to other two algorithms .Therefore GB and WPS algorithms are most efficient methods to implement FIR filter than other algorithms.

VIII EXPERIMENTAL RESULTS

Digit-serial FIR filter coefficients are implemented using CSE ,GB and WPS algorithms.The **Cadence tool** is used to simulate and synthesize the algorithms.**NClaunch tool** is used to simulate and observe the waveforms of various blocks used in CSE ,GB and WPS algorithms using verilog code**. Encounter tool** is used for synthesis and to observe the power,area and delay.

WPS ALGORITHM

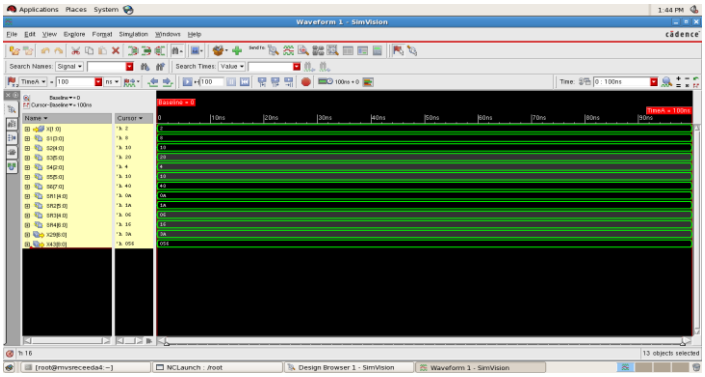


Fig 1: simulation of WPS algorithm

The WPS algorithm is designed with the adders and shifters .This is designed by giving any single binary value as input and the output is observed in terms of the filter coefficients of 29x and 43x . Here , when a value is given as input and by shifting and adding the value finally observed with the filter coefficients in hexadecimal.

Fig 1 By taking x=2 then the filter coefficients are 03A,056 are observed in the decimal representation.

TIMING DELAY

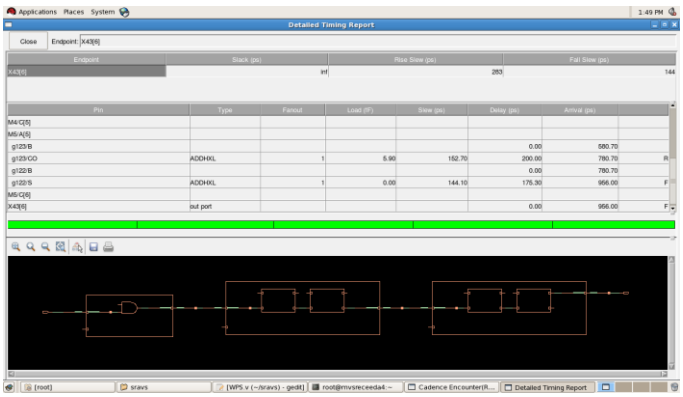
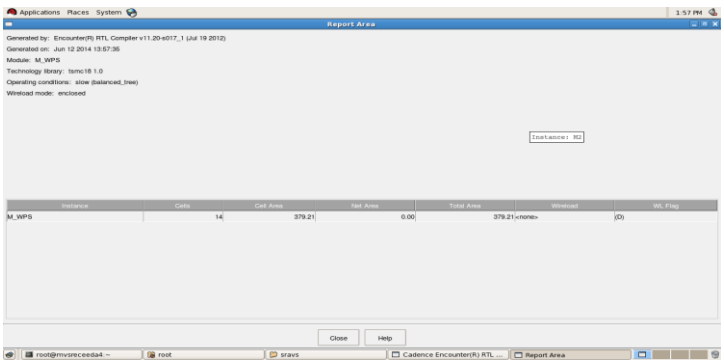


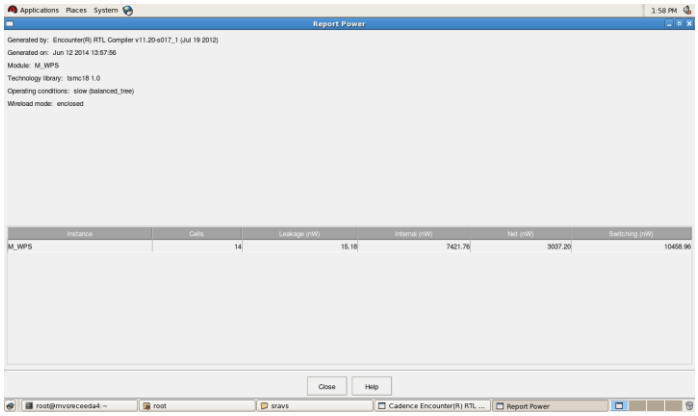
Fig 1.1 Timing delay od wps algorithm

The delay report for WPS algorithm is shown in fig 1.1 by using WPS algorithm the timing delay of FIR filter is 956 ps.

AREA



POWER



IX CONCLUSION

The 0-1 ILP formalization for designing digit-serial MCM operation with optimal area at the gate level by considering the implementation costs of digit-serial addition, subtraction, and shift operations. Since there are still instances with the exact CSE algorithm cannot cope, and also proposed an approximate GB algorithm that finds the best partial products in each iteration which yield the optimal gate level area in digit –serial MCM design. Also a new reconfigurable MCM architecture using WPS is proposed which provides the flexibility of changing the filter coefficient word lengths dynamically with less power dissipation.

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