

COMPARISON OF LOW POWER AND DELAY USING BAUGH WOOLEY AND WALLACE TREE MULTIPLIERS

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Abstract:This paper presents a design of 8-bit x 8-bit unsigned multiplier for high-speed Digital Signal Processing (DSP) applications. High-speed is achieved by a new architecture implementing our earlier multiplication technique for less power consumption and delay. The comparison with Baugh-Wooley multiplier with Wallace tree multiplier which shows that our multiplier consumes only 74% of the power with 2.37×10^{-9} delay.

I.INTRODUCTION

The next generation of wireless network requires high-throughput and low power Digital Signal Processing (DSP) System-on-Chip (SoC). Amongst the building blocks of a DSP system a multiplier is an essential component that has a significant role in both speed and power performance of the entire system. Therefore to enhance the performance of DSP SoCs designing of a high-performance and power efficient multiplier is crucial. In this chapter we discussed 2 different multipliers namely Baugh wooley multiplier, Wallace tree multiplier These three multipliers are implemented in xilinx and compared them in terms of both Power dissipation and Delay.

II. BAUGH WOOLEY MULTIPLIER:

Baugh Wooley multiplier is designed to cater multiplication of both signed and unsigned operands, which are represented in the 2's complement number system. The partial products are adjusted so that the negative signs are moved to the last steps, which in turn maximize the regularity of multiplication array. The Baugh Wooley multiplier is an interesting implementation of a multiplier. It produces a relatively standard cell shape for easier manufacturing, while maintaining good driving characteristics. Each full adder within the multiplier performs a similar number of computations, with the diagonal ripple carry propagating the input signal a constant and similar number of times

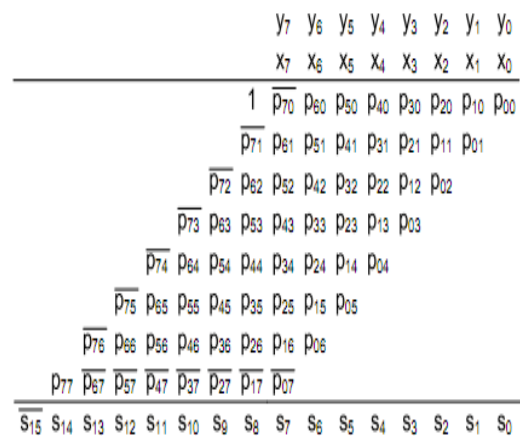


Fig.1.Baugh wooley multiplier

a)Architecture Baugh wooley multiplier

Architecture of baugh wooley multiplier is based on the carry save algorithm. It inherits the regular and repeating structure of the array multiplier. The structure of a 4x4-bit 2's complement multiplier is shown below

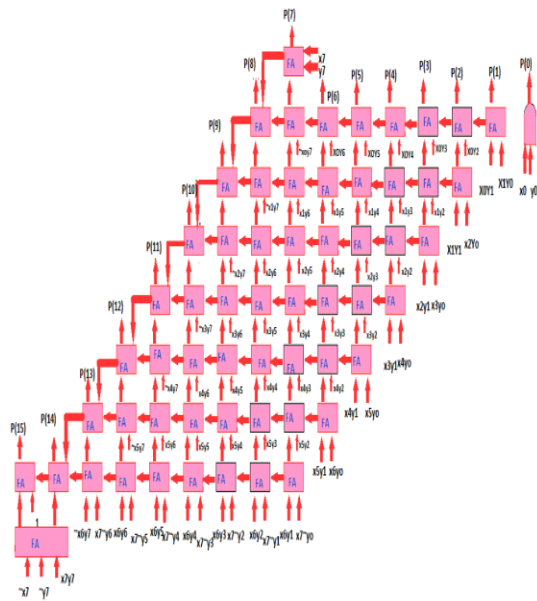


Fig.2. Architecture of 8 bit Baugh Wooley Multiplier

b) ALGORITHM OF BAUGH WOOLEY MULTIPLIER:

The Baugh Wooley multiplier operates on signed operands with 2's complement representation to make sure that the signs of all the partial products are positive. To reiterate, the numerical values of 2's complement numbers, X and Y can be obtained using the following expressions

$$X = -X_{n-1}2^{n-1} + \sum_{i=0}^{n-2} X_i 2^i$$

$$Y = -Y_{n-1}2^{n-1} + \sum_{j=0}^{n-2} Y_j 2^j$$

The product of X and Y is expressed as

$$P = XY$$

$$= X_{n-1}Y_{n-1}2^{2n-2} + \sum_{i=0}^{n-2} \sum_{j=0}^{n-2} X_i Y_j 2^{i+j}$$

$$- X_{n-1} \sum_{j=0}^{n-2} Y_j 2^{n+j-1} - Y_{n-1} \sum_{i=0}^{n-2} X_i 2^{n+i-1}$$

It is observed that last two terms of above equation are subtracted from partial product. To prevent the use of subtractor cells and use only adds these negative terms must be transformed. Therefore

$$-X_{n-1} \sum_{j=0}^{n-2} Y_j 2^{n+j-1} = X_{n-1} \left(-2^{2n-2} + 2^{n-1} + \sum_{j=0}^{n-2} Y_j 2^{n+j+1} \right)$$

The product P becomes

$$P = XY$$

$$= -2^{2n-1} + (X_{n-1} + Y_{n-1} + X_{n-1}Y_{n-1})2^{2n-2}$$

$$+ \sum_{i=0}^{n-2} \sum_{j=0}^{n-2} X_i Y_j 2^{i+j} + (X_{n-1} + Y_{n-1})2^{n-1}$$

$$+ X_{n-1} \sum_{j=0}^{n-2} Y_j 2^{n+j-1} + Y_{n-1} \sum_{i=0}^{n-2} X_i 2^{n+i-1}$$

Using a step by step approach, this 2's complement multiplication algorithm can be converted into an equivalent parallel array expression, as adopted by Baugh wooley multiplier

c) Block Diagram of Baugh wooley multiplier:

Baugh wooley multiplier code is written using verilog HDL and implemented in xilinx and the block diagram obtained is shown as below

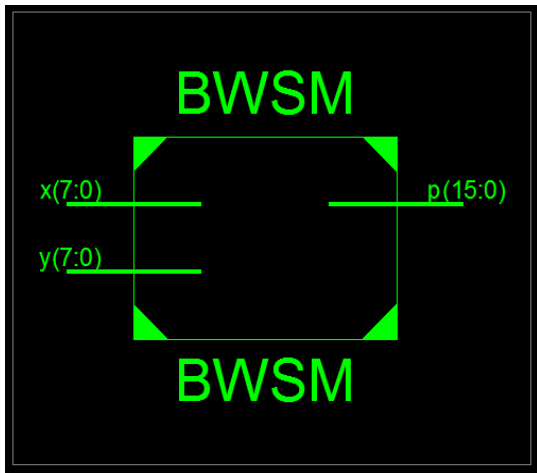


Fig.3.pin diagram

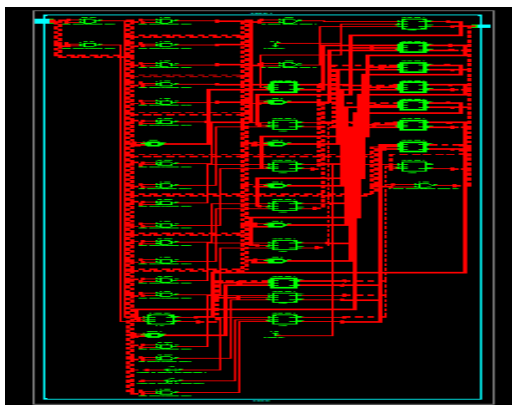


Fig.4.Technology schematic of Baugh Wooley Multiplier

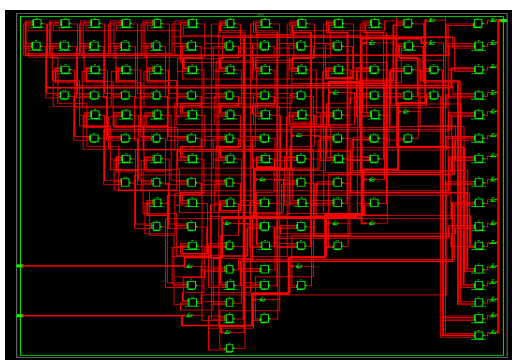


Fig.5.RTL Schematic of Baugh wooley multiplier

Baugh wooley multiplier block diagram implemented in xilinx and main sub blocks used are full adders and gates and inverters.

Table 1:Power and timing report of Baugh wooley multiplier

Power Dissipation	74.3mW
delay	2.37X10 ⁻⁹

III .WALLACE TREE MULTIPLIER

A wallace tree multiplier is an efficient hardware implementation of a digital circuit that multiplies two integers, Let us take two 4bit numbers and the multiplication according to the Wallace tree multiplication is as follows

$$\begin{array}{r}
 a_3a_2a_1a_0 \times b_3b_2b_1b_0 \\
 \hline
 a_3b_0 \ a_2b_0 \ a_1b_0 \ a_0b_0 \\
 a_3b_1 \ a_2b_1 \ a_1b_1 \ a_0b_1 \\
 a_3b_2 \ a_2b_2 \ a_1b_2 \ a_0b_2 \\
 a_3b_3 \ a_2b_3 \ a_1b_3 \ a_0b_3 \\
 \hline
 \end{array}$$

The product terms are adjusted as shown below

$$\begin{array}{r}
 a_3b_3 \ a_2b_3 \ a_1b_3 \ a_0b_3 \ a_0b_2 \ a_0b_1 \ a_0b_0 \\
 a_3b_2 \ a_2b_2 \ a_1b_2 \ a_1b_1 \ a_1b_0 \\
 a_3b_1 \ a_2b_1 \ a_2b_0 \\
 a_3b_0
 \end{array}$$

And these adjusted partial products added using 3 to 2 adder i.e full adder in two stages and the partial products obtained in 2nd stage are added using final adders as shown below the architecture of 4 bit Wallace tree multiplier

a)Architecture of wallace tree multiplier

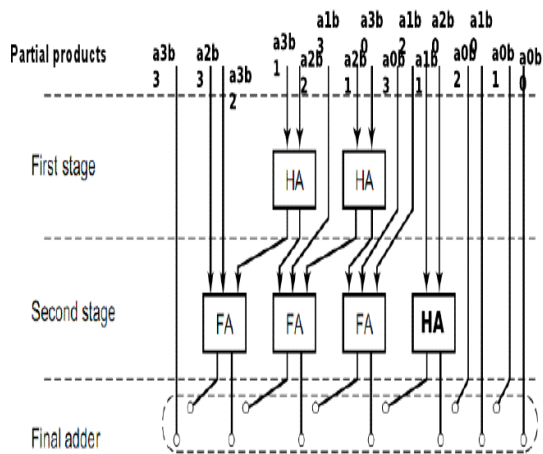


Fig. 6: Architecture of Wallace Tree Multiplier

The Wallace tree multiplication has three steps:

1. Multiply (that is - AND) each bit of one of the arguments, by each bit of the other, yielding n^2 results. Depending on position of the multiplied bits, the wires carry different weights, for example wire of bit carrying result of a_2b_3 is 32 (see explanation of weights below).
2. Reduce the number of partial products to two by layers of full and half adders.
3. Group the wires in two numbers, and add them with a conventional adder.

Wallace tree algorithm reduces both the critical path and number of adder cells. This algorithm reduces the propagation stages by 3 to 2 compressor Using Wallace tree algorithm hardware saving for larger multiplier. Propagation delay is reduced

Wallace tree do not provide any advantage over ripple adder trees in many

FPGAs. Due to the irregular routing, they may actually be slower and are certainly more difficult to route. Adder structure increases for increased bit multiplication.

Let us consider 8bit Wallace tree multiplier as shown in figures

b) Block Diagram of 8bit Wallace Tree Multiplier:

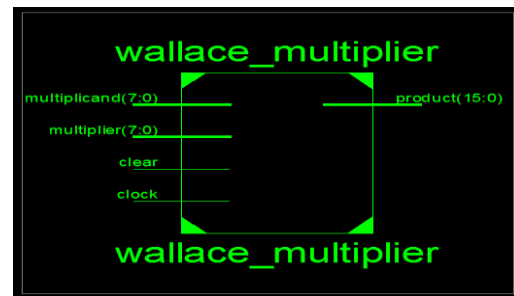


Fig.7.Pin diagram of 8 bit Wallace tree Multiplier

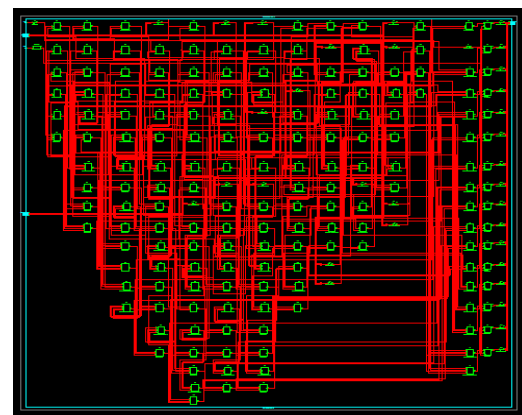


Fig.8.RTLSchematic diagram of 8 bit Wallace tree Multiplier

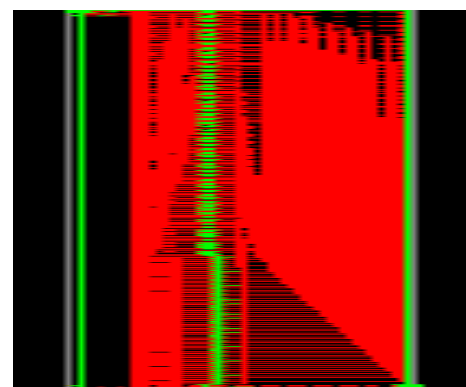


Fig.9.Technology schematic

In the above figure stage 1 and stage 2 are divided in to two stages 1a ,1b, 2a and 2b respectively and block diagrams and Schematic diagram of each stage shown below

Table 2:power and delay report of wallace tree multiplier

POWER	67.72mW
DELAY	42.15ns

Table 3: power and delay comparison of different multipliers

Multiplier(180nm)	Power dissipation	delay
Baugh wooley(0.25MHz)	74.3mW	2.37×10^{-9}
Wallace tree(0.25MHz)	67.72mW	42.15×10^{-9}

IV. Simulation results

Output wave forms of different Multiplier implementations are shown.Different multipliers like Baugh wooley multiplier, Wallace Tree multiplie functionality is verified by writing verilog code. And these two multipliers are implemented using xilinx simulator as shown below



Fig.10. Output wave form of 8 bit baugh wooley multiplier

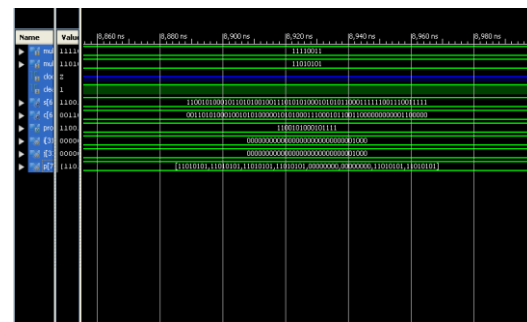


Fig.11. output wave form of 8 bit wallace tree multiplier

V. CONCLUSION

Wallace Tree Multiplier Baugh Wooley Multiplier are implemented and power dissipation and propagation delay are calculated.

To implement Proposed pipelined multiplier different adders namely pseudo NMOS adder, xor & Transmission Gate, transmission gate full adder, Complementary CMOS are implemented and they are compared in terms of power and propagation delay product pseudo NMOS has less power propagation delay product.

Different latches are implemented namely positive edge triggered register, C²MOS register, split output using 5 transistors and 8 transistors and true single phase positive latch and negative latch

among which 5 Transistor split output is best in terms of power and propagation delay

Wallace Tree Multiplier, Baugh Wooley multiplier are implemented and their power dissipations and delays of each multiplier are calculated and compared. Pipelined multiplier is implemented in 180nm technology, 90nm technology and 45nm technology and their respective power and delay and operating frequency are calculated. Power dissipation and delay are reduced. Pipelined multiplier implemented in 180nm technology has 3.1GHz operating Frequency, pipelined multiplier implemented in 90nm has 7GHz operating frequency And 45nm technology pipelined multiplier has 9.4GHz frequency

V. REFERENCES

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