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Design of Auto Depannage Digital System with Efficient Fault Coverage

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***Abstract*— In this paper presents the design of an efficient method for fault recovering in a digital system. The biological inspiration used in auto depannage system overcomes the limitations of conventional fault tolerant methods. The fault recovering and processing steps are adopted from endocrine cellular communication. By using this method system can recover fault by replacing faulty module with spare module or with transferring the encoded data in similar module. This scheme reduces hardware overhead and additional rerouting along with increasing size of the circuit.**

***Index Terms*—Endocrine cellular communication, Functional layer, Gene control layer, Stem Cell, Working cell**

I. INTRODUCTION

Every electronic circuit always faces the difficulty of functional fault, even if they provide good performance. The regular routine of the circuit may disturb if there any single fault occur in the system. In critical applications, fault plays a major role in system performance, and system need efficient fault recovery method to maintain normal state. In the early stages, conventional methods like DMR and TMR were used ,but they offered less fault coverage and increased redundancy. Thus new approaches arose from biological concepts and are more suitable in fault tolerant digital system design [1]-[15]. One of the delegate approaches, MUX TREE method [13] offers better self repairing and replication, but has only less fault coverage. Another approach uses endocrine systems [9] to improve redundancy, but needs a complex communication for rerouting. This paper presents a new methodology to overcome these problems, thereby using endocrine cellular communication for self repairing [1] in digital systems. The Auto Depannage mechanism improves the fault detection and also reduces hardware overhead for digital system design.

II. AUTO DEPANNAGE MECHANISM USING ENDOCRINE CELLULAR COMMUNICATION

Auto Depannage digital system is a self recovering digital system that can recover from different types of functional faults. In endocrine cellular communication, endocrine cell secretes a specific hormone for cell replacement only after it receives another specific hormone of damage cell indication. By adopting the similar mechanism, proposed system isolates the faulty cells and replaces with a proper spare cell.

III. SYSTEM OVERVIEW

The entire architecture of Auto Depannage digital system is composed of two layers, called functional layer and gene control layer as in Fig 1.

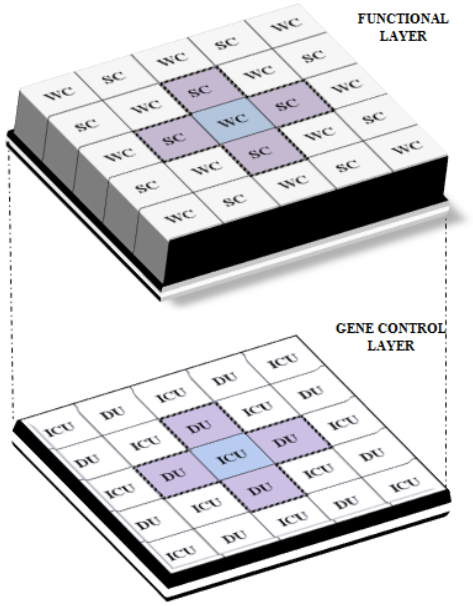

Fig 1. Auto Depannage digital system architecture

Both layers are operated in parallel, thus the system can recover even several faults occur in different modules a same time. Functional layer contain artificial cells (modules). Module may be working cell(WC), spare cell(SC) or isolated cells. Every WC is surrounded with its 4 SC as shown in Fig 1, and each SCs is connected to its neighbouring WC. Each WC having its own ICU and SCs has it own DU in gene control layer. The gene control layer is functionally positioned in parallel with the functional layer. Thus, the gene control layer must control the functional layer properly without a collision. Fig 2. shows interaction between layers for fault recovering. Here WC is replaced by SC when a permanent fault arises in it.

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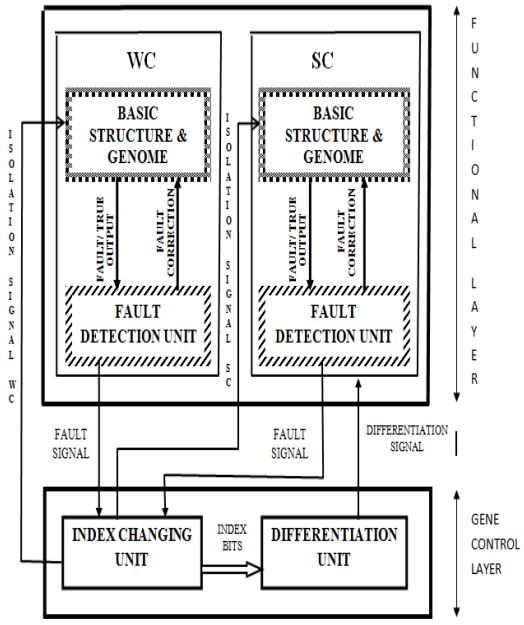

Fig 2. Interaction between layers for fault recovery

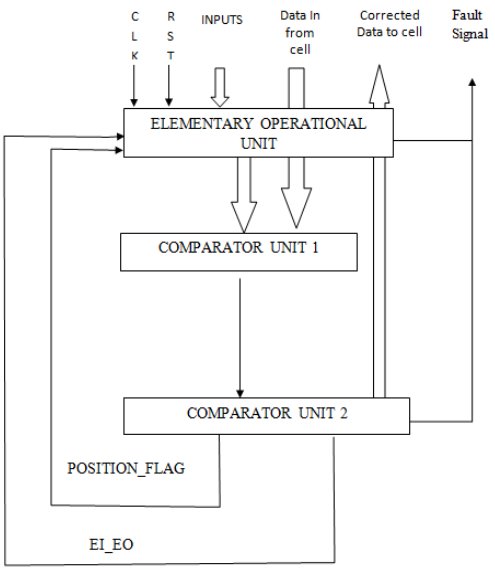

Fig 3. Fault detection and correction unit

A. Functional Layer

Functionality of target digital system is divided into different genome and fed in each working cells (WC). Each WC is surrounded by its own stem (spare) cells and it contains genome of neighboring working cell. The isolated cells are cells which are isolated due to permanent fault . These 3 types of cells are commonly known as module. All modules have similar basic structure and these different modules forms a layer called functional layer (structural layer).Every module contain two major units. They are,

1) Genome and Basic Structure

The genome plays the most important role in each cell. Genome is similar to a memory, which contains encoded data about functionality and routing structure. Using the proper genome, module constructs a basic structure corresponding to functionality of WC. The output from it is given to fault detection and correction unit.

2) Fault Detection and Correction Unit

The drawbacks of existing system are it requires large memory for fault detection and correction, and less functional fault recovery. The proposed architecture overcomes it by elementary operational unit as shown in Fig 3.The elementary unit produce bitwise fixed result corresponding to inputs of WC. This result is fed into comparator unit 1 and cross check the data in (True or fault output). Then it is set flag if any mismatch is present. Faulty data and its location, is found out by using comparator unit2. If it is a transient fault, then try to correct it using elementary unit and perfect genome and send corrected data to cell. If the fault appears simultaneously, even after fault correction and genome replacement, then it is a permanent fault. It is due to the fault in genome, the entire cell has to be replaced then set a fault signal and given to gene control layer.

B. Gene Control Layer

The gene control layer assigns proper spare cell by producing control signals after receiving fault signal as in Fig 2. It finds available spare cell and selects proper genome to the particular spare cell. Then the spare cell takes the functionality of the faulty working cell. The gene control layer is composed of,

1) Index Changing Unit

Index changing unit (ICU) receives faulty signals and changes the index bits. TABLE I shows index bits and its ideal values.

State bit: It shows whether the cell is a SC or a WC or an isolated cell.

Direction bit: It indicates the direction of the WC for which stem cell is differentiated

Differentiation bit: It signifies the indication to enable spare cell.

TABLE I . INDEX BITS FOR EACH STEM CELL

State bit	Stem cell		0
	Working or Isolated cell		1
Direction bits	The direction of the WC for which stem cell is differentiated	Left	00
		Down	01
		Right	10
		Up	11
Differentiation bit	No change		0
	Differentiate the stem cell		1

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2) Differentiation Unit

The Differentiation Unit (DU) receives index bits and sends differentiated signal to corresponding stem cell. At the same time, the isolation signal is sent to faulty module from ICU. Thereby, the fault recovery is achieved and the target system maintains the normal operation

IV. FUNCTIONAL FAULT COVERAGE

Auto Depannage mechanism offers functional fault coverage. It may be a transient or permanent or simultaneous fault. Fig 4 shows Auto Depannage ALU without any fault. Consider it can perform 4 different operations like addition, subtraction, multiplication and shifting. The WC and SC arranged as in Fig 4.

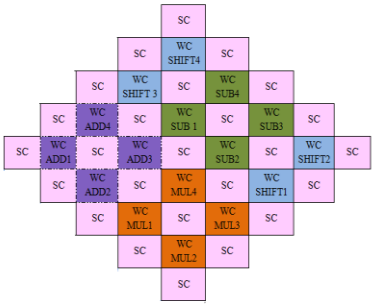

Fig 4. Auto Depannage ALU without any fault

A. Transient Fault

Transient fault or a temporary fault can recover by fault detection and correction unit itself.

B. Permanent Fault

Permanent fault corrupt the genome or its basic structure. Thus it can recover by selecting proper spare and isolates faulty cell. Consider the case of selecting addition operation. If there is no fault in adder WC's, the system continue it's working in without using SCs as in Fig 4. But when the adder 4 WC suffer by temporary fault, it will try to overcome by fault detection and correction unit and retain it's working condition. Sometimes it is not possible correct the fault, due to permanent fault in genome. Thus the WC replaced by stem cells and also isolated the faulty cell. Gene control layer generate corresponding signals according to the status of functional layer. The following figures, Fig 5 to Fig 9 show different stages of fault recovering in Auto Depannage ALU.

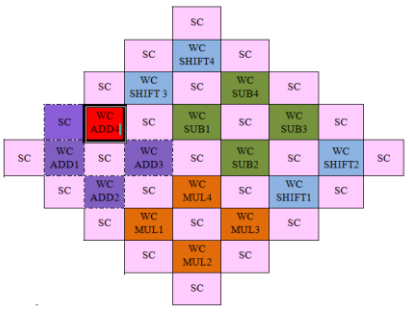

Fig 5. Permanent fault recovery by left SC

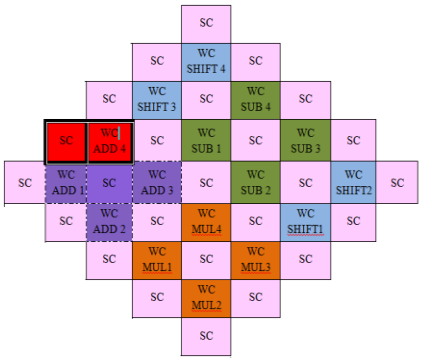

Fig 6. Permanent fault recovery by down SC

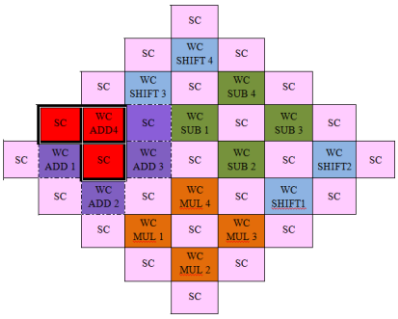

Fig .7 Permanent fault recovery by right SC

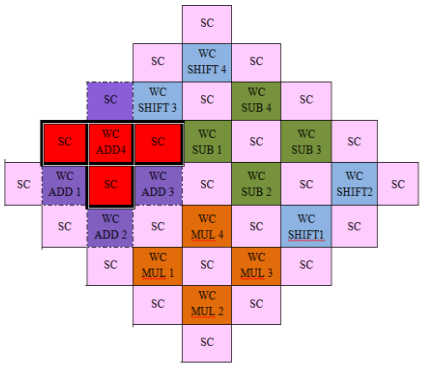

Fig 8. Permanent fault recovery by top SC

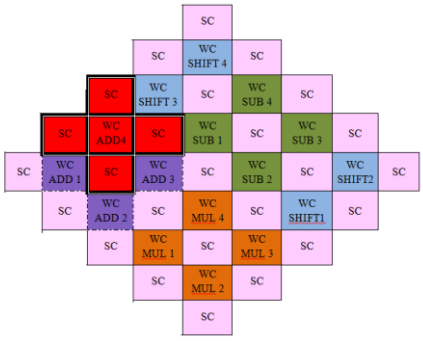

Fig 9 . Permanent fault in adder 4 WC and its all SCs

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If 4 SCs and its working cell WC ADD4 become fault, the addition operation module stop its working by isolating SCs as in Fig 9. Thus the adder 4 unit becomes fault.

C. Simultaneous Fault

There is a chance to occur simultaneous fault in this ALU. Here the Fig 10. shows the simultaneous fault occurring in working cell of WC ADD3 and left stem cell of WC ADD4.SC for both cell are same. In that case gene control layer assigns the next proper stem cell to WC ADD4, that is its down cell, as in Fig 10. These are shows only several conditions of fault in adder cell. Similarly it is possible to recover different kinds of faults in other functional modules in Auto Depannage ALU .

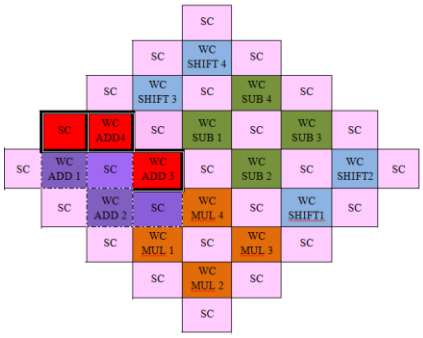

Fig 10. Simultaneous fault recovery.

V. SIMULATION RESULT

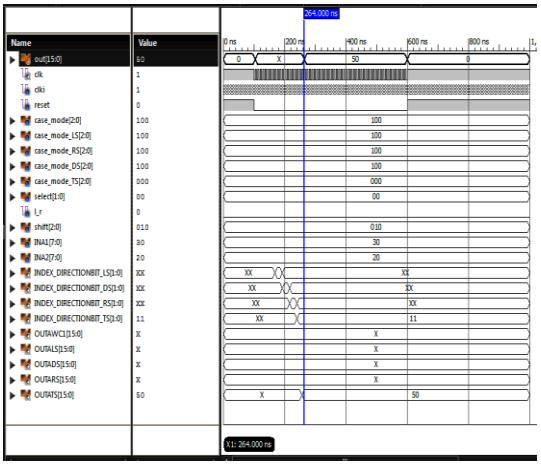

Fig 11. Simulation result of system after fault recovery.

Fig 11, shows the permanent fault recovery after injecting fault in WC and its 3 SCs.

VI. EXPERIMENTAL SETUP

The proposed system is embedded in a digital platform with an Xilinx Spartan 6 FPGA for the application of an ALU. Several cases of recovery from a permanent fault and transient fault are demonstrated in the platform. When the transient fault is detected, at the rising of the next clock faulty data recovered to normal data and the system operates normally.

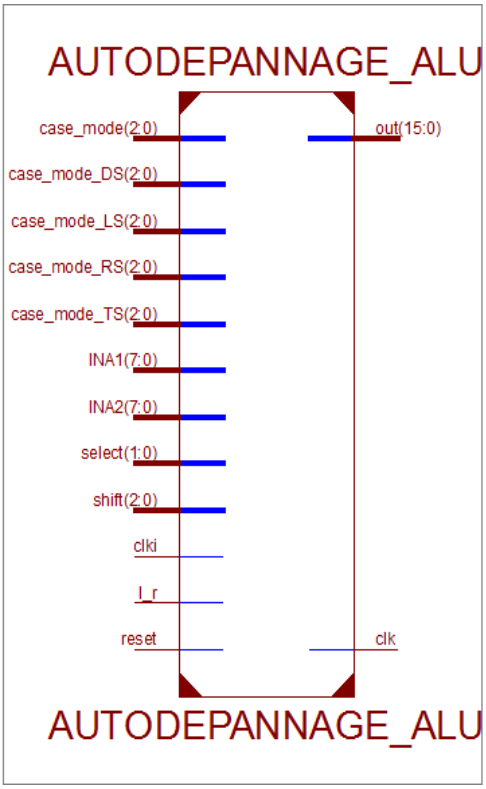

Fig 12. Autodepannage ALU

In permanent fault, the normal operation is maintained using spare cells. Fig.5 to Fig 10 shows the changed states of cells by the fault recovery after a fault is injected in cells. Here, the system repairs the permanent fault in a counter clockwise sequence. However, if the fault is generated in TS after a faulty RS is replaced by TS, the entire system stops operating because there is no SC left for repair. The speed of the clock used for the recovery is much faster. Thus, the ALU can operate normally after fault generation. Through various demonstrations, the proposed system is verified.

VII. PERFORMANCE ANALYSIS WITH EXISTING APPROACHES

The main aim of the proposed Autodepannage architecture is to reduce the area, memory usage, time delay and thereby increase scalability and accuracy. Xilinix ISE Design Suite 14.2 platform provides a summary for logic utilization, time constraints and memory usage. By analysing the graphs we can conclude that compare to existing self repair ALU, proposed Autodepannage ALU reduce the area, memory usage, time delay.

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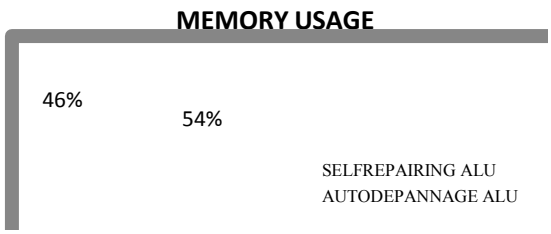

Fig 12. Memory Usage

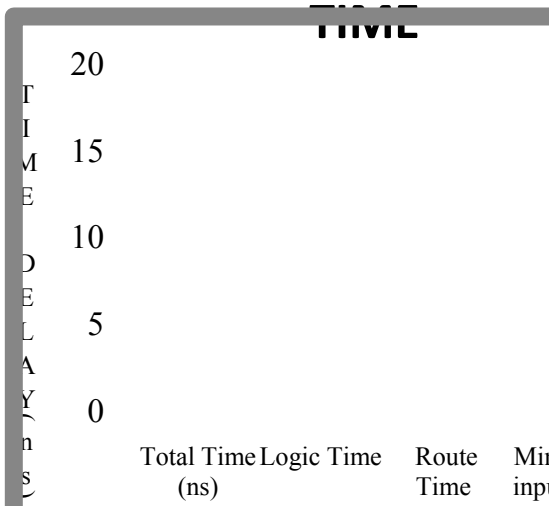

Fig 13. Timing analysis

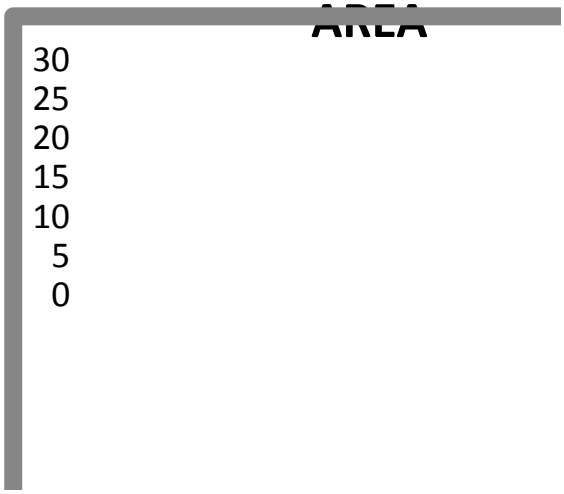

Fig 14. Area Analysis

Here the Fig.12 shows proposed Auto Depannage ALU reduce in memory usage existing self repair ALU. This will happen mainly due to the modified architecture of Fault detection and correction. Timing Analysis shows in Fig.13, the proposed system reduces the total time delay. It is the sum total of logic time and the routing time. The total time required to Auto Depannage ALU got reduced. Area Analysis Fig 14 shows that the proposed system reduces the total area compared to the existing one. These 3 Plots were drawn by analysing the design summary of both approaches after synthesis.The proposed system was compared to other major self-repair approaches and it was found that the proposed system has good fault coverage, low overhead, and no unutilized resources for fault recovery.

VIII. CONCLUSION AND FUTURE SCOPE

The Auto Depannage digital system provides good scalability and fault coverage. New architecture for fault detection offers less memory usage and having good fault coverage. Furthermore, due to the new architecture, the cells could be arranged in densely and flexible way, also the WC could be expanded to any four directions. The exact control in the gene-control layer offers fault recovery without collision. As a result, all these create the system efficient compare to other existing approaches.

For further improvement of the proposed Auto Depannage system, there remains several issues awaiting further studies. The primary goal of developing a fault tolerant or Auto Depannage system is to deal with faults that can occur in the target system. Other faults that might occur in additional hardware are not considered. Hence, the secondary faults that can occur in the additional functional hardware should be considered as well in the consideration of the cost and frequency. This means that addressing possible faults in the additional functional hardware remains as a topic for further study.

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