Design and Simulation of OTA-C Based Filter for ECG Signal Detection

Ajit Singh, Uma Sharma

Abstract— This paper presents designing of OTA-C based filter for biomedical applications. In this design various techniques are used such as current splitting, source degeneration to increase the linearity of the device. The MOSFETs are bulk driven and are in cut-off mode due to which power dissipation is reduced. Simulation is done in 180nm technology on tanner tool and operating under ± 0.75 V. From the schematic simulation, this filter provides following results - Bandwidth 252Hz, total power consumption of 2.292 μ W.

Index Terms— Bulk driven, cascode mirror, current splitting, ECG, linear range.

I. INTRODUCTION

In the present era technology rises continuously due to need of various applications. In biomedical applications such as ECG signal detection requires approximately 250hz cut-off frequency low-pass filter [7][8][9]. To achieve such a small frequency, a small Gm typically few nA/V requires (bulk driven technique is used to get small Gm) [1]. The devices used for biomedical applications need to be small, light weight, portable and most importantly low power. Scaling down of device helps to achieve these needs however by doing so, the linearity degraded moreover gain reduces due to limited output impedance[10]. So various methods to enhance linearity such as source degeneration, gate generation, bump linearization in OTA proposed in [3]. But it uses simple current mirror which requires offset voltage. This paper is organized as follows: in section II, basic concept of bulk driven is discussed. In section III, basic operation of OTA, modification by tunability concept (current splitting) is discussed. In section IV, designing of Butterworth filter is done by using the proposed OTA. In section V, simulation results discussed. Finally at the end conclusion of the paper in section VI.

II. BASIC CONCEPT OF BULK DRIVEN

When a MOSFET is using as an amplifier, input signal is given through gate terminal of the MOSFET. The bulk is tied to the bias voltage. This technique is called gate-driven in which output current is a function of input gate-to-source voltage. On the other hand in bulk-driven technique input is

Ajit Singh, Deptt. of E.C.E, A.K.G. Engineering College. Uttar Pradesh Technical University Ghaziabad, India, Phone/ Mobile No -+919873446273,

Uma Sharma, Deptt. of E.C.E, A.K.G. Engineering College. Uttar Pradesh Technical University, Ghaziabad, India, given through the bulk of MOSFET, in which the threshold voltage is a function of bulk-to-source voltage which ultimately controls output current [12]. In gate-driven, a minimum threshold voltage is required at the input to make device active whereas in bulk-driven which acts like depletion MOS do not require any input voltage to make circuit active. So the circuit will work at zero-bias voltage. This is the fundamental advantage of the bulk-driven technique [2]. There are few more benefits of using this method. Significantly improvement in input common range used for low frequency applications due small Gm [11].

There is always two sides of a coin, so instead of having these advantages there are some drawbacks also, Most importantly its low dc gain. For a standard digital CMOS technology (i.e. n-well process), only PMOS can be bulk-driven. There is a requirement of twin-well technology if both polarities need to be bulk driven.

The current equation for a well-driven MOS in sub-threshold conduction is given by

$$I = I_o e^{-kVgs/Vt} e^{-(1-k)Vws/Vt}$$
(1)

Where V_{gs} , V_{ws} are the gate to source and well to source voltage, V_t is threshold voltage, k is the sub-threshold conduction coefficient which is generally greater than 0.5. The gate modifies the current through k exponential term whereas well modifies it by (1-k) exponential term. It shows that only one term is active at a time either gate or well.

III. BASIC OTA

An OTA is a voltage controlled current source device (VCCS) because in this output current is function of input voltage as shown in Fig. 1. Therefore the transfer function of the device is a transconductance denoted by Gm. There are various technique used in designing OTA[3] for increasing its linearity such as differential input mode, source generation, gate generation and bump linearization. By using these techniques linearity of 1.7 volt is achieved.

The limitation of this design is the requirement of the offset voltage. To overcome this problem simple current mirror is replaced by cascode current mirror[5]. This technique helps to provide high d.c gain due to its high output impedance and also remove the problem of offset voltage requirement. Moreover this technique helps to increase the open loop gain of the device.

Manuscript received Sept, 2014.



The total transconductance of the circuit is given by

$$g = \frac{1-k}{1+\frac{1}{kp}+\frac{1}{kn}}$$
 (2)

Where 1/kp and 1/kn are the loop gains of source degeneration and gate degeneration respectively. The output current of the circuit is given by,

$$= I_{\rm B} \tanh \left(V_{\rm d} / V_{\rm L} \right) \tag{3}$$

Where I_B is the bias current, V_L is the linear range of the OTA which is given up by,

$$V_{\rm L} = 2V_{\rm T}/g \tag{4}$$

Now if we expand the term tanh,

From equation no (3), we come to know that V_L will be decrease if g will increase. Due to which the higher order term of tanh i.e cubic term, can be ignored in output current equation(2). So output current will become linear function of the bias current due to which non-linearity will reduced. Further if we apply the bump linearization calculation, linearity will further increased. Output current for bump linearized circuit given by

$$I_{OUT} = I_{B} \frac{\sinh(2x)}{1 + \frac{w}{2} + \cosh(2x)}$$
(5)

Where $x = V_d / V_L$, w is scaling factor. For w=2,

$$I_{OUT} = I_B \frac{\sinh(2x)}{2 + \cosh(2x)}$$
, also

So according to the equation (4)(5)(6), we get that output current is further linearized.

A. Concept of programmability using current splitting technique.

The device bandwidth can be change by changing its transconductance. By using this technique we can digitally program the transconductance moreover by reducing transconductance, the device can be used for biomedical applications. In this technique parallel MOSFET is implemented with the input MOS due to which current get splitted between the MOSFET [6]. These parallel MOSFETs can be digitally controlled, by controlling their gate-to-source voltages.

Basic circuit diagram of the current splitting technique is shown in Fig. 2.



The transconductance of the modified circuit is reduced by M+1,

$$Gm = \frac{g}{M+1}$$
(7)

Where g is transconductance before current splitting, M is scaling factor.

B. Proposed OTA

In the proposed OTA, simple current mirror is replaced by cascode mirror which provide high impedance and high dc gain. In this model, transconductance of the device is reduced for the use in biomedical applications. Biasing current of nA/V is provided by is provided by a separate circuit attached to it.

Various techniques mentioned above such as current splitting technique, source degeneration are implemented due to which non-linearity of the circuit is reduced. Further the power dissipation is reduced by using MOSFETs in cut-off mode. The bulk driven technique help to reduce transconductance and also increases linearity of the circuit. Using all these techniques proposed OTA implemented as shown in Fig. 3.

International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 3, Issue 9, September 2014



IV. PROPOSED FILTER

In this section Butterworth filter is designed by using the proposed OTA for the detection of ECG signal detection as shown if Fig. 4. The bandwidth of this filter is 252Hz and have very small power dissipation of 2.292μ W.



Fig. 4 Proposed filter

V. SIMULATION RESULTS

The proposed filter provides a bandwidth of 252hz and power dissipation of 2.292μ W as shown in Fig. 5. Various results are calculated as shown in Table. I.



Table I. Comparison of proposed filter with the previous

WORK			
Parameters	2009 [13]	2013 [14]	Proposed
			Filter
CMOS	180nm	250nm	180nnm
Technology			
Supply voltage	±1V	±0.8V	±0.75
Vth	0.5V	0.53V	0.5V
Order	5	5	5
Bandwidth	250hz	243hz	252hz
Power	0.453µW	30µW	2.292µW
dissipation			

VI. CONCLUSION

An OTA-C low-pass filter is designed for ECG signals. This filter uses low-voltage supply and low distortion. The use of tunable OTA will change the bandwidth of the filter according to the value of the Gm that will give more range of covered frequencies with similar noise. The objective of this LPF design is to achieve high linearity (by using linear programmable OTA), low power consumption.

ACKNOWLEDGMENT

We would like to thank Ajay Kumar Garg Engineering College for providing all the resources required for this work and their faculty member guidance.

REFERENCES

[1] S. Solis-Bustos, J. Silva-Martinez, F. Maloberti, and E. Sanchez-Sinencio, "A 60 db dynamic-range CMOS sixth-order 2.4 Hz lowpass filter for medical applications," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. Conj, vol. 47, pp. 1391-1398, Dec. 2000.
[2] P. M. Furth and A. G. Andreou, "Linearised differential transconductor in

[2] P. M. Furn and A. G. Andreou, Elnearised differential transconductor in subtreshold CMOS," Electron. Lett., vol. 31, no. 7, pp. 547-554,1995.

R. Sarpeshkar, R. F. Lyon, and C. A. Mead, A low-power widelinearrange transconductance amplifier, Analog Integrated Circuits Signal Processing, vol. 13, pp. 123-151, 1997.

[3] L. Ferreira., T. Pi menta and R. Moreno, "An ultra-low voltage ultralow-power CMOS miller OTA with rail-to-rail input output swing," IEEE TCAS II, vol. 54, no. 10, pp. 843-847,2007.

[4] G. Palumbo, "Frequency behaviour of the Wilson and improved Wilson MOS current mirrors: analysis and design strategies," Microelectronics Journal, vol. 27, pp. 79-85,1996.

International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 3, Issue 9, September 2014

[5] Anand Veeravalli, Edgar Sánchez-Sinencio, José Silva-Martínez," Transconductance Amplifier Structures With Very Small Transconductances: A Comparative Design Approach," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 37, NO. 6, JUNE 2002

[6] L. C. Stotts, "Introduction to implantable biomedical IC design," IEEE Circuits Devices Mag., pp. 12–18, Jan. 1989.[7] P. Kinget and M. Steyaert, "Full analog CMOS integration of very large

[7] P. Kinget and M. Steyaert, "Full analog CMOS integration of very large time constants for synaptic transfer in neural networks," Analog Integr. Circuits Signal Process., vol. 2, pp. 281–295, 1992.

[8] R. L. Geiger and E. Sánchez-Sinencio, "Active filter design using operational transconductance amplifiers—a tutorial," IEEE Circuits Devices Mag., no. 1, pp. 20–32, 1985.

[9] W. H. G. Deguelle, "Limitations on the integration of analog filters below 10 Hz," in Proc. IEEE ESSCIRC'88, 1988, pp. 131–134.

[10] R. Fried and C. C. Enz, "Bulk-drivenMOStransconductor with extended linear range," Electron. Lett., vol. 32, pp. 638–640, 1996.
[11] A. Guzinski, M. Bialko, and J. C. Matheau, "Body-driven differential

[11] A. Guzinski, M. Bialko, and J. C. Matheau, "Body-driven differential amplifier for application in continuous-time active-C filter," in Proc. IEEE Eur. Conf. Circuit Theory and Design (ECCTD'87), 1987, pp. 315–319.

[12] Shuenn-Yuh Lee, Member, And Chih-Jen Cheng, Student Member, "Systematic Design And Modeling Of A Ota-C Filter For Portable Ecg Detection", *IEEE Transactions On Biomedical Circuits And Systems*, Vol. 3, No. 1, pp.53-64, 2009.

[13] Soliman A. Mahmoud , Ahmed Bamakhramah , Saeed A. Al-Tunaiji, "Low-Noise Low-Pass Filter For Ecg Portable Detection Systems With Digitally Programmable Range", *Circuits Syst Signal Process* , Vol 32, pp.2029–2045, 2013.



Ajit Singh received his B.Tech degree in Electronics and Communication Engineering from H.N.B. Garhwal University, India in 2011. This author is pursuing M.Tech in VLSI Design from A.K.G. Engineering College, Ghaziabad, Uttar Pradesh, India. His major areas of research interest include Analog Filter Circuit Design, Low Power and High Speed Signal Processing Circuits and Communication Systems.



Uma Sharma received her M.Tech degree in VLSI Design from Banasthali Vidyapeeth College, India in 2012. This author is currently teaching as an Asstt. Prof. at A.K.G. Engineering College, Ghaziabad, Uttar Pradesh, India. Her major areas of research interest include Micro Electronics, Analog Filter Circuit Design, Low Power and High Speed Signal Processing Circuits and Communication Systems.