International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 3, Issue 9, September 2014

High Speed Low Power Operations for FFT Using Reversible Vedic Multipliers

Malugu.Divya
Student of M.Tech, ECE Department (VLSI),
Geethanjali College of Engineering & Technology
JNTUH, India.

Mrs. B. Sreelatha
Associate Professor, ECE Department,
Geethanjali College of Engineering & Technology
JNTUH, India.

Abstract

Vedic mathematics can be aptly employed here to perform multiplication. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution. Vedic mathematics is world renowned for its algorithms that yield quicker results, be it for mental calculations or hardware design. Power dissipation is another important constraint in an embedded system which cannot be neglected. In this paper we bring out a Vedic multiplier known as "Urdhva Tiryakbhayam" meaning vertical and crosswise, implemented using reversible logic, which is the first of its kind. This multiplier may find application in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications. The Fast Fourier Transform (FFT) has become almost ubiquitous and most important in high speed signal processing. Another important area which any DSP engineer has to concentrate is the power dissipation, the first one being speed. There is always a tradeoff between the power dissipation and speed operation. The reversible computation is one such field that assures zero power dissipation. The goal of this paper is to develop a methodology to synthesize binary combinational reversible logic circuits in regular and non-regular structures, in binary logic, for multi-output functions, and minimizing a complex cost function.

***Key Words*- CI, FFT, GO, Optimized Design, Vedic Multiplier, Reversible Logic Gate, Urdhva Tiryakbhayam, Quantum Cost, NG, And Total Reversible Logic Implementation Cost.**

I.INTRODUCTION

Vedic Mathematics:

India has produced many mathematicians whose discoveries have benefited the world. One such mathematician was Swami Bharati Krishna Tirtha (1884 – 1960). As a student of the Vedas from 1911 – 1918, he stumbled upon few sutras (aphorisms on word-formulae). After extensive research on these sutras, he reconstructed 16 Sutras and 13 Upa-Sutras using which numerical calculations can be done in simpler and faster ways. In Vedic Mathematics, unlike the conventional methods, there are many ways to arrive at a solution for a problem. This is the beauty of Vedic Mathematics; it can be understood easily by people of any caliber. It enhances the ability to approach and solve any mathematical problem.

Vedic Mathematics is one of the most ancient methodologies used by Aryans in order to perform mathematical calculations. This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts put by Jagadguru Swami Sri Bharathi Krishna Tirtha Maharaja to introduce Vedic mathematics to the commoners. Vedic Algorithms are divided into 16 categories or Sutras which are acknowledged and appreciated.

This paper is organized as follows: The section II gives the scope of Reversible Multipliers and parameters. Section III gives the basic reversible logic gates. Section IV explains the Urdhva Tiryakbhayam algorithm. Section V describes the modifications to evolve the optimized design. Section VI Introduction to FFT. Section VII compares the proposed design with the other non-Vedic multipliers as well as the previous Vedic Multiplier design and draws a conclusion of Reversible UT Multiplier.

ISSN: 2278 – 909X

II. SCOPE OF REVERSIBLE MULTIPLIERS

According to Moore's law the numbers of transistors will be doubled every 18 months. Thus energy conservative devices are the need of the day. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information.

Charles Bennett showed that energy loss could be avoided or even eliminated if the computations are carried out in reversible logic and also proved that circuit built from reversible gates have zero power dissipation. Thus reversible logic appears to be promising in future low power design applications.

The reversible circuit/gate has the following characteristics:

(i) Has equal number of inputs and outputs.
(ii) The gate output, which is not used as primary output in the circuit, is called garbage output.
(iii) The input which is used as control input to the gates is called constant/garbage input
(iv) The fan-out of each gate is equal to one. A copying circuit is used if two copies of a signal are required and
(v) The resulting circuit is acyclic. An efficient design in reversible logic should have the following features:
    a) Use minimum number of reversible logic gates
    b) Should have less number of garbage outputs
    c) Less number of constant inputs, and
    d) Minimization of quantum cost.

Optimization parameters for reversible logic circuits:

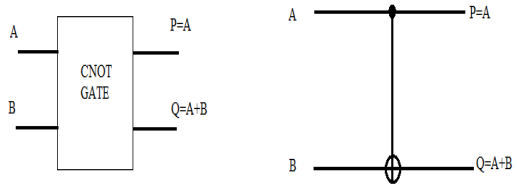
The important parameters which play a major role in design of an optimized reversible logic circuit are as listed:

- **Constants (CI)**
- **Garbage (GO)**
- **Gate count (NG)**
- **Flexibility**
- **Quantum cost (QC)**
- **Gate levels**
- **Total Reversible Logic Implementation Cost (TRLIC)**

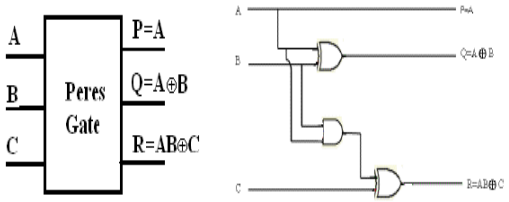
$$TRLIC \quad \sum(NG + CI + GO + QC) \ldots 1$$

III. REVERSIBLE LOGIC GATES

CNOT Gate

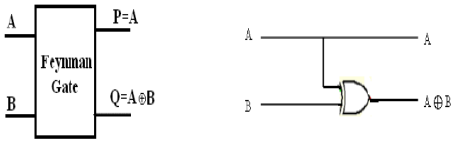


PERES Gate



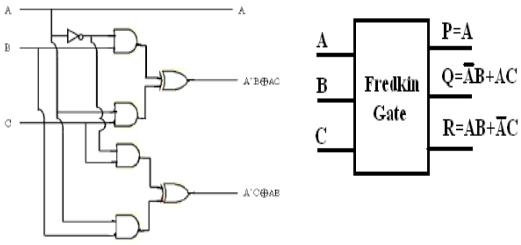
peres gate and its logic ciruit

FEYNMAN Gate



feynman gate and its logic ciruit

FREDKIN Gate



fredkin gate and its logic ciruit

HING Gate

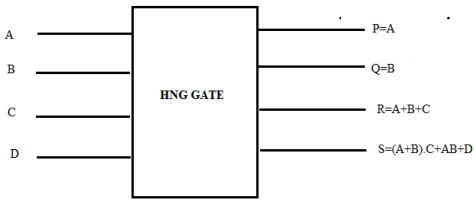


Fig 1: Reversible Logic Gates

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IV. URDHVA TIRYAKBHAYAM MULTIPLICATION ALGORITHM

Urdhva Tiryakbhayam (UT) is a multiplier based on Vedic mathematical algorithms devised by ancient Indian Vedic mathematicians. Urdhva Tiryakbhayam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". Urdhva Tiryakbhayam Sutra can be applied to all cases of multiplications via. Binary, Hex and also Decimals. It is based on the concept that generation of all partial products and their summation is obtained using Urdhva Tiryakbhayam.

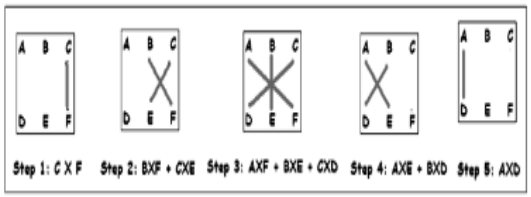

Fig 2: Urdhva Tiryakbhayam procedure for Multiplication

The Algorithm:

Multiplication of 101 by 110

1. We will take the right-hand digits and multiply them together. This will give us LSB digit of the answer.
2. Multiply LSB digit of the top number by the second bit of the bottom number and the LSB of the bottom number by the second bit of the top number. Once we have those values, add them together
3. Multiply the LSB digits of the bottom number with the MSB digits of the top one, LSB digit of the top number with the MSB digit of the bottom and then multiply the second bit of both, and then add them all together.
4. This step is similar to the second step, just move one place to the left. We will multiply the second digit of one number by the MSB of the other number.
5. Finally, simply multiply the LSB of both numbers together to get the final product.

V. OPTIMIZATION OF THE URDHVA TIRYAKBHAYAM MULTIPLIER

The conventional logic design implementation of a 2x2 Urdhva Tiryakbhayam multiplier using the irreversible logic gates. In the four expansions for the output bit are derived from this figure and is used to obtain the reversible implementation as shown in Figure 3. The circuit uses five Peres gates and one Feynman gate.

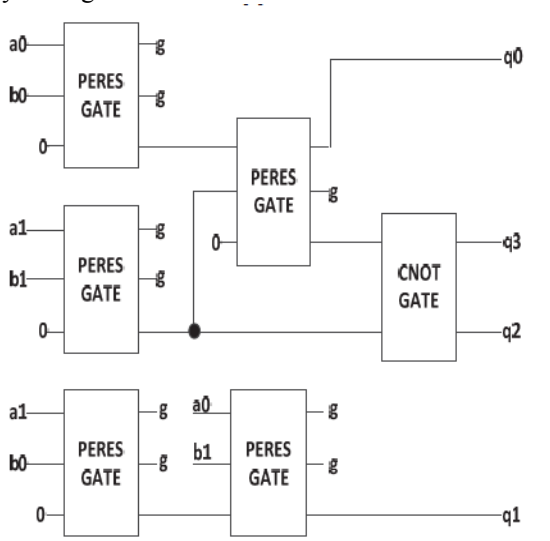

Fig 3: Reversible 2x2 UT Multiplier

Design of 4x4 Urdhva Tiryakbhayam multiplier:

The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design emanates from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure 4. It consists of four 2X2 Multipliers each of which procures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. Two zeros are concatenated with the upper two bits and given as input to the ripple carry adder and obtained from the second 2X2 multiplier. Likewise the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these four bit ripple carry adders are in tum 5 bit each which need to be summed up.

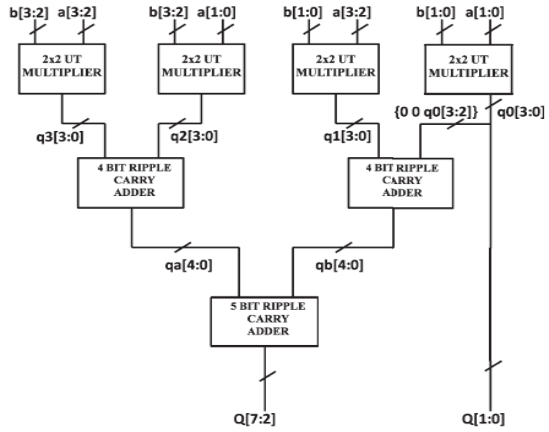

Fig 4: Reversible 4x4 UT Multiplier

ISSN: 2278 – 909X

VI. INTRODUCTION TO FFT

Digital signal processing is an area of science and engineering that has developed rapidly over the past 30 years. This rapid development is a result of the significant advances in digital computer technology and integrated-circuit fabrication. The digital computers and associated digital hardware of three decades ago were relatively large and expensive and, as a consequence, their use was limited to general-purpose non-real-time (off-line) scientific computations and business applications. These inexpensive and relatively fast digital circuits have made it possible to construct highly sophisticated digital systems capable of performing complex digital signal processing functions and tasks, which are usually too difficult and/or too expensive to be performed by analog circuitry or analog signal processing systems. Hence many of the signal processing tasks that were conventionally performed by analog means are realized today by less expensive and often more reliable digital hardware.

Radix-2 FFT Algorithms:

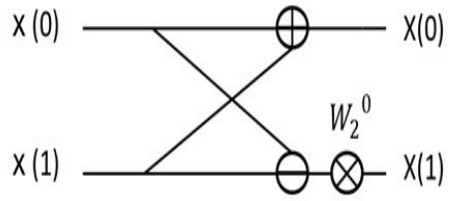

Fig 5: Radix-2 FFT

Radix- 4 FFT Algorithms:

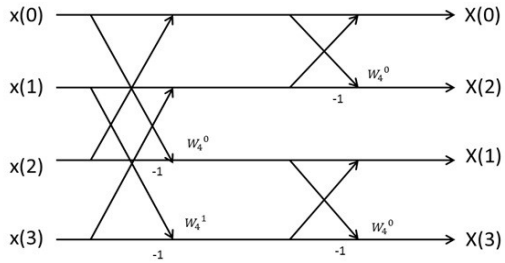

Fig 6: Radix-4 FFT

VLSI EDA Tools:

Xilinx ISE: Integrated Software Environment (ISE) enables to quickly simulation of HDL source, Synthesis of HDL based RTL design and FPGA Implementation (Placing, Routing, and Mapping) and Bit Stream Generation.

Languages (HDL): Verilog/VHDL.

VII. EXPERIMENTAL RESULTS

The design of the reversible 2x2 and 4x4 multipliers is logically verified using XILINX 9.2i and MODELSIM. The simulation results are as shown in figure.

The following are the important design constraints for any reversible logic circuits.

1. Reversible logic circuits should have minimum quantum cost.
2. The design can be optimized so as to produce minimum number of garbage outputs.
3. The reversible logic circuits must use minimum number of constant inputs.
4. The reversible logic circuits must use minimum number of reversible gates.

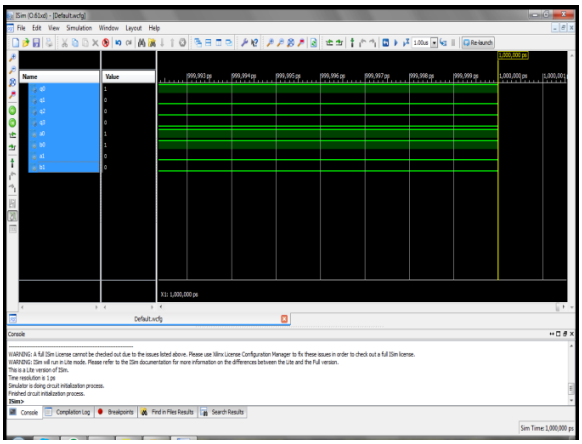

Fig 7: Simulation result of 2x2 multiplier

Logic Utilization	Used
Number of 4 input LUTs	35
Logic Distribution	
Number of occupied Slices	20
Number of Slices containing only related logic	20
Number of Slices containing unrelated logic	0
Total Number of 4 input LUTs	35
Number of bonded IOBs	17
Total equivalent gate count for design	210
Additional JTAG gate count for IOBs	816

Fig 8: Reversible gates parameters for 2x2 multipliers.

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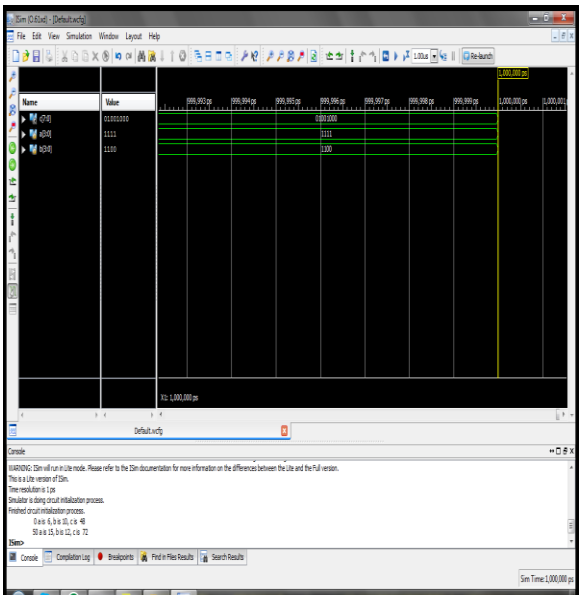

Fig 9: Simulation result of 4x4 multiplier.

TOP MODULE:

Reversible FFT-16 Radix 2

Logic Utilization	Used
Number of Slices	47
Number of 4 input LUTs	83
Number of bonded IOBs	128

Fig 10: Rev FFT-16 Radix 2 parameters

Reversible FFT-16 Radix 4

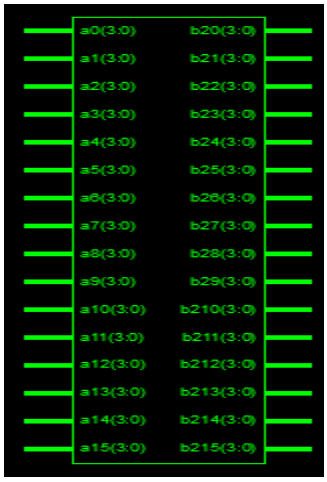

Fig 11: Rev FFT-16 Radix 4

Logic Utilization	Used
Number of 4 input LUTs	68
Logic Distribution	
Number of occupied Slices	36
Number of Slices containing only related logic	36
Number of Slices containing unrelated logic	0
Total Number of 4 input LUTs	68
Number of bonded IOBs	128

Fig 12: Rev FFT-16 Radix 4 parameters

Reversible FFT-32 Radix 2

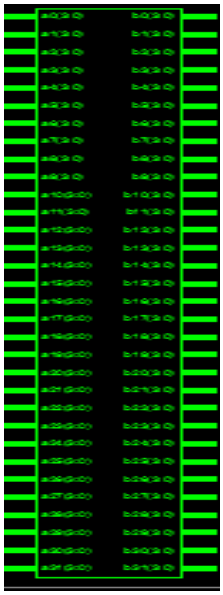

Fig 13: Rev FFT-32 Radix 2

Logic Utilization	Used
Number of 4 input LUTs	166
Logic Distribution	
Number of occupied Slices	92
Number of Slices containing only related logic	92
Number of Slices containing unrelated logic	0
Total Number of 4 input LUTs	166
Number of bonded IOBs	256

Fig 14: Rev FFT-32 Radix 2 parameters

VIII. CONCLUSION

Since Vedic multiplier is designed, the delay has been considerably reduced to 16.910ns. For the array reversible logic multiplier the delay is found to be 20.035ns. The gate count is also reduced by 35 instead of 52 for the array reversible logic multiplier. The power consumption is found to be 52mW. Thus we can say that the design is optimized in terms of area, speed, power and quantum cost.

ISSN: 2278 – 909X

This paper presents the Urdhva Tiryakbhayam Vedic Multiplier realized using reversible logic gates. First 2x2 UT multiplier is designed using Peres gate and Feynman gate. The ripple carry adders which were required for adding the partial products were constructed using HNG gates. This design has high speed, smaller area and less power consumption when compared with other reversible logic multipliers.

ACKNOWLEDGEMENTS

We would like to thank our parents and teachers who have been a source of encouragement for all our works.

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ISSN: 2278 – 909X