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DEVELOPMENT OF HIGH PERFORMANCE STANDARD CELL LIBRARY IN UMC180nm TECHNOLOGY

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Abstract— **Designs based on different technology at competitive cost has always been challenges to manufacturers .Some of the driving factors including portability, mobility, accuracy and increased performance demands. This brings the manufacturers to adapt certain methods such as decrease component sizes, increase its performance simultaneously, improve heat tolerance materials and so on. To design every logic gate at different driver strength will be time censuring. So this thesis will try to solve the problem by creating own standard cell library with specified specifications at different driving strengths. So, this can ensure us about the ability of precharacterised, preverified cells for utility in designing complex circuits. In high performance standard cell library, the main objective is to increase performance of logic cells that satisfies the given specifications. The benefit of high performance cell library is used in processors, high computational IC's etc. designs where density will be neglected to meet the performance. The software used for the design is cadence software.**

***Index Terms*— Cadence Software, ASIC, LVS, DRC, VHDL, CAD**

I. INTRODUCTION

A. Basic Introduction

IC development is nowadays a huge industry. There is an almost infinite amount of consumer products like mobile phones, processors, televisions, cameras, refrigerators, ovens and cars that in one way or another uses custom IC components. A digital integrated circuit can be manufactured with a number of different approaches, but they all contain the same basic steps. It all starts with transistors, wiring and all the things that make up the circuit being placed in a layout, designed in a CAD (Computer Aided Design) tool and ends up with that layout being physically created on a chip[11]. The way to create this layout differs depending on design requirements.

Standard cell library contains a collection of components that are standardized at the logic or functional level, and consists of cells or macro-cells based on the unique layout. The economic and efficient accomplishment of an IC design depends heavily upon the choice of the library. Therefore, it is important to build library that fulfills the design requirement.

A library of logic cells is the set of building blocks for the ASIC design flow. The library is typically called a standard cell library because of its common interface implementation and regular structure. One way to understand the required layout characteristics of standard cells is to understand their history and the reasons behind their development. Once the concepts and methodologies behind this design process are understood, it is easier to fully appreciate the layout requirements for the cells themselves. There are three basic ways as given below.

i) Full Custom

Full custom design is when everything in the layout is created manually. Every single transistor used can be set up as desired, optimized for speed, area or capacitive load etc. Every single wire in the layout is placed manually and the designer has total control over the layout. This is done when the design has very strict requirements and needs to be optimized in one way or another. The obvious advantage is that the layout can be created very carefully to fit the need. On the other hand, this requires a lot of work and time.

ii) Semi Custom

Semi custom design is when the designer works on a logical gate level. This means that the designer can use gates like NAND, Inverters, Buffers, Flip-Flops etc. that have already been created and distributed as a cell library by a supplier. The idea is to reuse blocks of logic instead of creating them manually over and over again. Instead of placing every transistor and wire, the designer places logic blocks in the layout that corresponds to the desired function. The good thing with semi custom layout is that the required time is decreased and it is far less advanced compared to full custom layout. The downside is that the possibility to optimize the given gates is very limited, so the designer loses some control of the layout. A combination of full and semi custom layout can often be a good approach, where the logical gates are created manually and optimized and then used in a semi custom layout instead of using gates created by a supplier.

iii) Automatic Design

Automatic design is similar to semi custom design in that it uses pre- created standard cell libraries. The difference is that in the automatic design approach, the layout is created automatically. The work of the designer in this case, is to describe the design in a high level programming language like VHDL or Verilog. The high level description is then fed to the automatic design tools which create a layout that corresponds to the description. Automatic design therefore

suffers from creating less optimized layouts compared to full custom design and even semi custom design. As mentioned, the automatic design process uses standard cell libraries created by some supplier, generally the one that has supplied the technology that is being used (90nm, 65nm, 45nm and so on). While these standard cell libraries are quite flexible they may not fit the requirements. A solution to this would be to create a standard cell library manually and use that in the automatic design. This would give the designer total control of the cells in the library and still make it possible to use automatic design tools when creating layouts, thus allowing both the optimization of the design building blocks and rapid layout creation.

B. *Objective of the Project*

The objective of this project is to Design and implement High Performance Standard Cell Library according to the specifications and to perform transient analysis on the implemented designs. Finally to compare the pre-layout and post-layout results of the cells designed at different process corners.

C. *Methodology*

Survey of different types of standard cell libraries along with different approaches of IC implementations are done [3][5]. The methodology adopted in implementing this project is to start from the design of 1X load (drive strength), which is the base load. Continuing, the design of different combinational and sequential logic cells to drive different loads ranging from 1X-64X.The back annotation of layouts is carried out. Finally pre and post layout design results are compared and verified.

II. LITERATURE SURVEY

A. *IC Implementation Approaches*

Integrated Circuit (IC) technology has gone through a spectacular revolution in the last two decades. The number of transistors that can be integrated on a single die has been exponentially increasing with time following the Moores Law. Present day microprocessors have more than one million transistors and are clocked at Giga Hertz (GHz) clock speeds. Bringing these high development cost associated high performance designs to the market at a competitive cost and in a lesser design time has always been a challenge for IC manufactures. To meet these challenges, different IC implementation approaches have been adopted ranging from custom design approach used for microprocessors and memories to the fully programmable designs for medium to low performance applications [1]. A classification scheme for the various implementation approaches is shown in Fig 1.

i) Cell Based Semi-Custom Design

With the advancement of design automation, Cell Based Semi-Custom IC implementation approaches have been introduced to shorten and automate the design process. The idea behind Cell Based design is to reduce the design cost and design time by reusing a library of cells called Standard Cell Library. The disadvantage is that the cells in the library decide the integration density and/or performance reducing the ability to fine-tune the IC design.

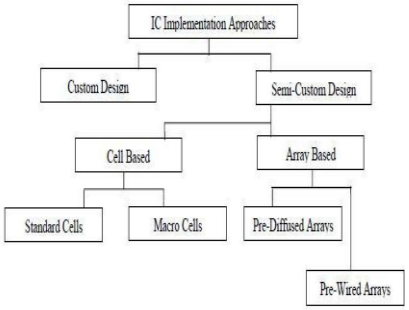

Figure 1: IC Implementation Approaches

ii) Standard Cell Library

The Standard Cell Library contains a collection of logic gates over a range of fan-in and fan-out. Besides the basic logic function, such as inverter, NAND, NOR, XOR and Flip-Flops, a typical library also contains more complex functions such as Multiplexers, Full-Adder, Comparator, etc. As shown in Fig 2, the Standard Cell Library is used in the Semi-Custom Design Flow to shorten the design process[1].

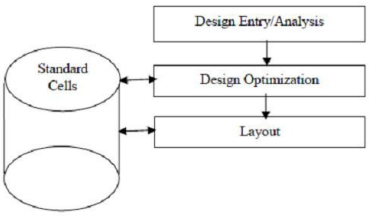

Figure 2: Semi-Custom Design Flow

B. *Standard Cell Library Design*

The Cells or logic gates selected to build the library depends on the design requirement. These cells when used in the Semi-Custom Design Flow have to meet certain functions and performance. In this library Software used to design same is cadence software .The cells are either area optimized or speed optimized. The area optimized cells uses minimum sized transistors while the speed optimized cells uses larger transistors to provide good driving capabilities. The Standard Cell Library development process can be depicted using a flow chart as shown in Fig 3.

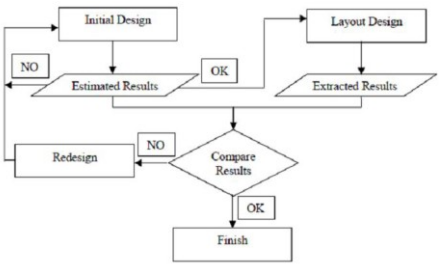

Figure 3: Standard Cell Library Development Methodology

The design specification of a particular cell in the library is decided and the initial design is done. It is checked whether the design meets the required specification. After this, the Layout of the designed cell is carried out and a net list is extracted from the Layout. The net list obtained from

the Layout is compared with the initial design. If the results match, then the design cycle is complete else, redesigning has to be carried out and the cycle is repeated. The flow chart given in Fig 3 does not show the sub-levels involved in the Standard Cell Library development like Schematic Capture or Layout Verses Schematic (LVS) analysis. The sizes of PMOS (Wp) and NMOS (Wn) of the transistors in the Cells are selected to meet design specifications such as power dissipation, delay, noise immunity and area. Therefore, the sizing constraint for Standard
Library Cells is similar to any MOS circuit design requirement of minimum area subject to delay less than or equal to the required timing specification. Therefore, Wp and Wn are determined by[1][2].

- DC switching point.
- Drive capability of the cell.

It should be noted that while designing the cells and deciding the sizes of the cells, process variations should also be considered for proper functioning of cells at the end of fabrication.

i) Number of Cells in Standard Cell Library

As explained before, an efficient implementation of a Semi-Custom Design depends on the Cells in the library. Standard Cell Libraries often provide 300 or even 500 Cells. It appears obvious that the design automation tool could do a better job if the number of cells is large. But in newer libraries, the number of functions as well as the number of layouts is reduced. This is because recent experiments demonstrate that with fewer Cells, the design automation tool is more efficient as it has a limited set of well-chosen cells to synthesize. With a fewer number of cells, the automation tool can easily produce an optimized result, without getting lost in some optimization loops due to large number of cells.

ii) Purpose and Development of the Standard Cell Library

Bringing high development cost associated high performance designs to the market at a competitive cost has always been a challenge for IC manufactures, especially start-up companies. The rising NRE cost can be tamed to a certain extent by using open source software for designing Standard Cell Library and adopting a Cell Based IC implementation approach. A large number of good quality CAD tools are available for VLSI design in open source domain. Thus the need to use high cost associated CAD tools and Standard Cell Libraries provided by commercial vendors can be avoided.

III DESIGN SPECIFICATIONS FLOW

The Bottom-Up design flow starts with a set of design specifications. The specs typically describe the expected functionality of the designed circuit as well as other properties like delay times, area, etc. To meet the various design specifications certain design trade offs (area verses delay) are required. Fig 4 shows design flow [4][6].

A. Schematic Capture

A Schematic Editor is used for capturing (i.e. describing) the transistor- level design. The Schematic Editors provide simple, intuitive means to draw, to place and to connect individual components that make up the design. The resulting schematic drawing must accurately describe the main electrical properties of all components and their interconnections. Also included in the schematic are the supply connections (Vdd and Gnd), as well as all pins for the input and output signals of the circuit. From the schematic, a net list is generated, which is used in later stages of the design. The generation of a complete circuit schematic is therefore the first important step of the transistor-level design[9].

B. Symbol Creation

A symbol view of the circuit is also required for some of the subsequent simulation steps or for documentation purposes. Thus, the schematic capture of the circuit topology is usually followed by the creation of a symbol to represent the entire circuit. The shape of the icon to be used for the symbol may suggest the function of the module (logic gates AND, OR, etc.), but the default symbol icon is a simple rectangular box with input and output pins. The symbol creation will also help the circuit designer to create a system level design consisting of multiple hierarchy level.

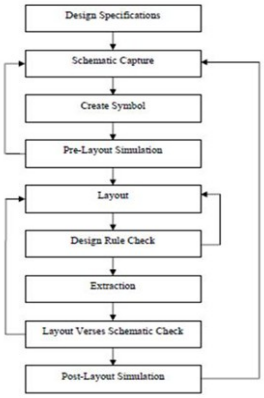

Figure 4: Design Flow

C. Pre-Layout Simulation

After the transistor-level description of a circuit is completed using the Schematic Editor, the electrical performance and the functionality of the circuit must be verified using a simulation tool. Based on simulation results, the designer usually modifies some of the device properties in order to optimize the performance. The initial simulation phase also serves to detect some of the design errors that may have been created during the schematic entry step.

D. Layout

The creation of the mask layout is one of the most important steps in the full-custom design flow, where the designer describes the detailed geo-metrics and the relative positioning of each mask layer to be used in actual fabrication, using a Layout Editor. Physical layout design is very tightly linked to overall circuit performance since the physical structures determines the transconductance of the transistors, the parasitic capacitances and resistances, and obviously the silicon area which is used to realize a certain function. But the process is very intensive and time-consuming design effort. It is also extremely important that the layout design must not violate any of the layout design rules, in order to ensure a defect free fabrication of the design. The layout

process can be a manual process, in which layout of each design is done manually or an automatic process using a CAD tool. But the quality of the layouts produced using automatic processes are still far from hand optimized layouts [7].

E. Design Rule Check (DRC)

The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects. A tool built in to the layout editor called Design Rule Checker, is used to detect any design rule violations during and after the mask layout design. If errors are detected, they should be removed from the mask layout, before the final design is saved.

F. Circuit Extraction

After the mask layout has been made free from design rule errors, circuit extraction is performed to create a detailed netlist for the simulation of the circuit. The circuit extractor identifies the individual transistors and their connections as well as the parasitic capacitances and resistances that are inevitably present. The extracted netlist can give a very accurate estimation of the device dimensions and device parasitics that ultimately determine the circuit performance. The extracted netlist are used in transistor level simulations and in Layout Verses Schematic comparison.

G. Layout Verses Schematic Check

After the mask layout design of the circuit is completed, the design should be checked against the schematic circuit description created earlier. The Layout Verses Schematic (LVS) Check will compare the original network with the one extracted from the mask layout. The LVS step provides an additional level of confidence for the integrity of the design, and ensures that the mask layout is a correct realization of the intended circuit topology. Also it should be noted that a successful LVS would not guarantee that the extracted circuit would actually satisfy the performance requirements since LVS check guarantees only a topological match. If any errors show up during LVS, then it should be corrected before proceeding to post layout simulation.

H. Post-Layout Simulation

The electrical performance of a full custom design can be best analyzed by performing a post-layout simulation on the extracted circuit netlist. The detailed simulation performed using the extracted netlist will provide a clear assessment of the circuit speed and the influence of circuit parasitic. If the results of the post-layout simulation are not satisfactory, the designer should modify the transistor dimensions or the circuit topology, in order to achieve the desired circuit performance. Thus, it may require multiple iterations on the design, until the post layout simulation results satisfy the original design requirements. Finally, it should be noted that a satisfactory result in post-layout simulation is still no guarantee for a completely successful product, since the actual performance of the chip can be only be verified by testing the fabricated prototype.

IV STANDARD CELL LIBRARY SPECIFICATIONS

Specifications

Parameters	High Performance Library
Operating Frequency	500MHz
Number of tracks	12
Cell Height	8.64um
Output Rise time/Fall time	50ps +10 %
Supply Voltage	1.8V
Temperature Range	-40oC to 125oC

Table 1: Specifications of high performance standard cell library

Process Corners

In semiconductor manufacturing, a process corner is an example of a design-of-experiments (DoE) technique that refers to a variation of fabrication parameters used in applying an integrated circuit design to a semi- conductor wafer. Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly. A circuit running on devices fabricated at these process corners may run slower or faster than specified and at lower or higher temperatures and voltages, but if the circuit does not function at all at any of these process extremes the design is considered to have inadequate design margin. Figure 5 Shows different process corners.

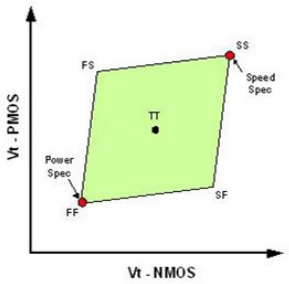

Figure 5: Different Process Corners

V DESIGN AND LAYOUT GUIDELINES

In this section we will discuss the design of the cell itself. The goal is to give an understanding of the standard cell design so that it is compatible with an ASIC design flow. There are many issues to consider. First and foremost, however, is that the library of cells be compatible with the specific limitations or features of the manufacturing process to be used[7].

A. Standard Cell Characteristics

The design or architecture of the standard cells should be chosen based on the number of routing layers available in the target manufacturing technology. In certain special cases the design of the cells will depend on the characteristics of the available metal layers. The following is a list of characteristics that are common to all standard cell libraries.

i) Circuit design characteristics

- The functionality and the electrical characteristics of each cell is tested, analyzed, and specified. In general, a test chip is manufactured and the performance of the each cell is analyzed from silicon. In some cases, only a process

characterization step is completed to generate simulation models of the transistor characteristics, and library characterization tools use these models to create the simulation views of each cell.

- Multiple drive strengths for each cell type are created. In addition, the different drive strengths are multiples of a base or minimum size.

ii) Characteristics related to the shape of the cells

- During the layout design of the cells, the cells are built using a predefined template that will ensure that all the requirements are met. The template includes the height of the cell, the placement of wells, N-transistors, and P-transistors, and guidelines to follow so that the cell can be flipped vertically or horizontally and can be placed beside all other cells without creating errors such as DRC violations[7].
- Cells are rectangular.
- Cells for specific rows or chip areas are all the same heighta library may contain multiple sets of cells. For example, different cells will be used for logic, datapath, and I/O areas.
- Every cell length is rounded up to a multiple of a coarse grid. This grid is determined by either of the following: A specific design rule (such as the minimum well width) A desire to make placement easier and faster (using a coarse grid reduces the number of possible placement coordinates, thus accelerating the placement process).
- The power supply lines have a predefined width and position for the entire library the width of the supply over the cell length is always consistent.

iii) Characteristics related to the interface of the cells

- All the input and output ports have a predefined type, layer, position, size, and interface points. These characteristics are determined based on the placer and/or router to be used to implement the design. The ports are targets for the router and should be optimized with the router in mind for best results. An example of this would be that routing can be made faster and easier by using a signal pitch that is defined on a coarse grid. Routing tools will use fewer computing resources if a coarse grid is used because the arithmetic required of the tool is simplified[8].
- The interface of the cells can be designed to share certain connections. Examples would be source connections of transistors that are connected to power supplies. Alternatively, common substrate and tub contacts can be shared between cells.
- All non shared polygons have to be spaced from the boundary of the cell by a value equal to one-half of the layer spacing design rule. This ensures that abutting cells will be correct by construction.

B. Layout Guide Lines For Standard Cells

- The sizes, shapes and locations of all geometries in layers pertinent to routing are regularized. If, for example, a metal1 signal track inside the cell is 1um wide, all other metal 1 tracks inside the cell must also be 1um wide [9].
- The general shape of the cell is as follows:

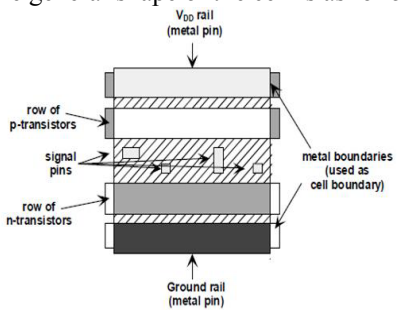

Figure 6: General shape of a standard core cell

- All metal tracks of the same layer (metal1, metal2, etc) for the same purpose (signal or power) must have the same width. If, for example, a metal1 track for signal connection is 0.5um wide, then all other signal connections in metal1 in the library must also be 0.5um wide. If a metal1 power pin is 2um wide, all cells in the library must use 2um wide metal1 power connections[7][8].
- All power / ground pins should have the same width and should run in same directions all horizontal or all vertical.
- Power / ground pins should be in the form of rail at the top/bottom ends of cell.
- Attempts must be made to lay signal tracks of the same layer in the same direction.
- For any two adjacent signal track in the same metal layer running in the same direction, center-to-center pitch (defined below) must be either the same, or an integer multiply of a minimal pitch value (called routing pitch).
- The routing pitch should at least line-to-via pitch, as defined in fig 6, where the closest separation (line to metal extension of via) still satisfies design rule for metal-to-metal separation. Ideally, it should be at least via-to-via pitch (see picture 7.c). This will allow the routing tool to drop via where necessary. Avoid using only line-to-line pitch as in 7.a, as the routing tool may fail since it is unable to drop a via when it is needed[7].

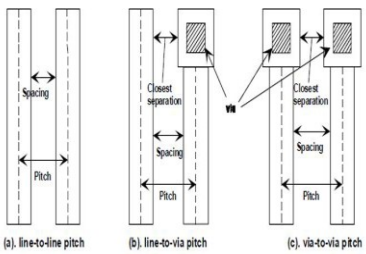

Figure 7: Definition of Routing Pitch

- All available of metal layers should follow the rules, even if there is no intention to actually use it for routing for example, in a ten-metal-layer process where it may not be critical that the first layer be usable. It should be possible to declare all metal layers as available for routing during the LEF file

generation later on, and it will allow the routing tool decides which metal layers will actually be used, which will likely result in better routing than if the cell designer explicitly prohibits the use of the first metal layer.

- Regardless of the number of metal layers provided by the technology, the number of metal layers used for internal connections within the cells should be limited. If possible, limit the metal track use to metal only, so that all higher metal layer tracks are freely available for use by the routing tool.
- The cell height must be a multiple of the horizontal grid spacing and the cell width must be a multiple of the vertical grid spacing in our case both grid are same[8].
- Regular Pins (not VDD VSS) should align at a grid point (aligned with both vertical and horizontal grids).

VI CELL DESCRIPTION

A. Combinational Cells

Inverter implementation in cadence software[10]

The inverter cell provides the logical NOT of input (A). The output (Y) is represented by the logic equation given below.

$Y = \bar{A}$

The schematic & symbol is as shown in fig 8 & 9,

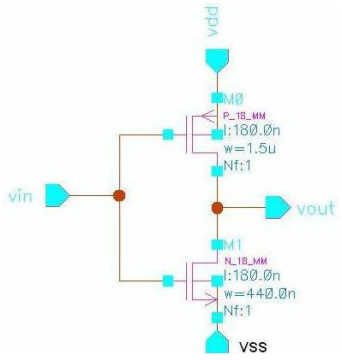

Figure 8: inverter schematic in cadence software

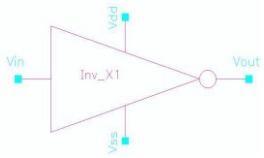

Figure 9: inverter symbol Inverter output

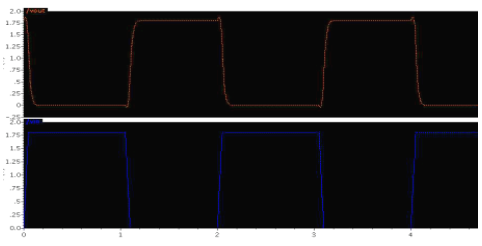

Figure 12: inverter waveform in cadence software

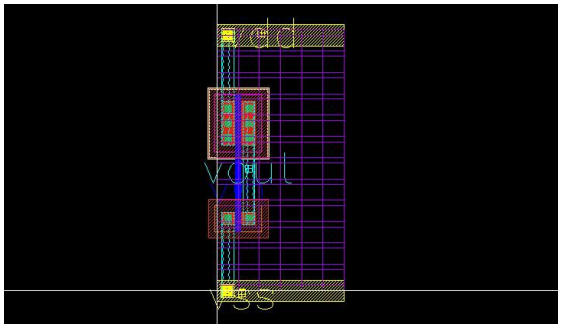

Figure 13: inverter layout in cadence software

Proces corners	rise time(ps)	Fall time(ps)	Propagation delay(ps)
tt	29.06	25.45	28.065
ss	31.85	30.49	32.745
ff	27.31	22.85	24.82

Table 2: Inverter1X

Proces corners	rise time(ps)	Fall time(ps)	Propagation delay(ps)
tt	37.39	33.27	31.4
ss	40.16	39.87	37.09
ff	35.07	30.9	28.29

Table 3: Inverter2X

B. Sequential Cells

D flip flop

The working of the D if op is similar to the D latch except that the output of D flip flop takes the state of the D input at the moment of a positive edge clock pin(or negative edge if the clock input is active low)and delays it by one clock cycle. That's why its commonly known as a delay flip flop. the advantage of the D flip flop over the D type transparent latch is that the signal on the D input pin is captured the moment the flip flop is clocked, and subsequent changes on the D input will be ignored until the next clock event[1]. The schematic & symbol is as shown in fig 10 & 11.

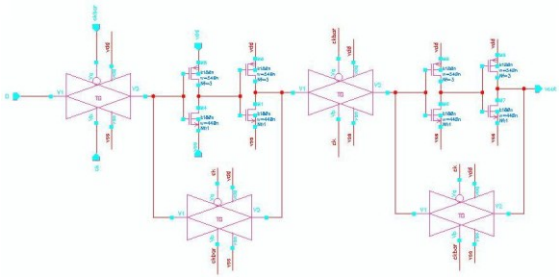

Figure 10: D flip flop schematic in cadence software

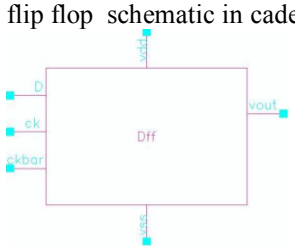

Figure 11: D flip flop symbol

D Flip Flop Output

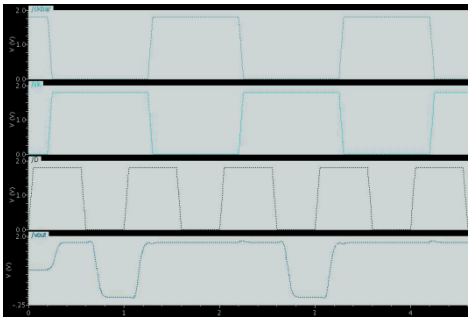

Figure 14: D flip flop waveform in cadence software

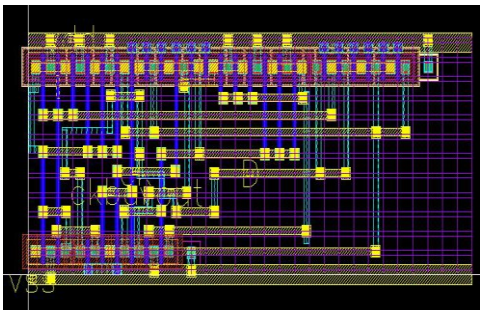

Figure 15: D flip flop layout in cadence software

Proces corner	rise time(ps)	fall time(ps)	Delay (ps)	Setup (ps)	Hold (ps)
tt	59.26	62.08	313.1	178	863
ss	71.68	77.02	399.8	178	863
ff	52.54	52.75	256.6	178	863

Table 4: D flip flop

VIII Conclusion and Future Scope

The main objective of project is to design high performance standard cell library and it is achieved by meeting the given specification. The required specifications to be met are cell height, rise & fall time, & propagation delay. This project meets pre layout and post layout results as per the design specifications. From the results we found that the designed library meets the required specification and is ready to be used in the semi custom design. The design use by using cadence software. In the future work we can generate a technology/timing library which is a text file containing information regarding timing and functional characteristics of an ASIC cell library. Several components of a technology library used by an ASIC design at various phases of design procedure are listed below:

1. Global parameters: These include PVT corner specifications, unit definitions, threshold values for input and output transitions and maximum output capacitance and slew limits.
2. Functionality for mapping during synthesis and functional simulations.
3. Area, power, timing constraints and delay values for optimization and delay simulation.
4. Pin locations, geometry of cells, routing blockages and grids for place and route.

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