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ANALYSIS and PERFORMANCE of 8x8 MIMO-OFDM SYSTEM design for 4G requirements realized using FPGA virtex 5

Geeta Karande, Rajesh S. Bansode , Devashree Patil

***Abstract*— OFDM system is combined with multiple-input multiple-output (MIMO) in order to increase the diversity gain and system capacity over the time variant frequency-selective channels. The current work is proposed to design an efficient scheme for orthogonal frequency division multiplexing (OFDM) using 8x8 multiple input multiple output (MIMO) antennas. However, the major drawback of MIMO-OFDM system is the transmitted signals on different antennas exhibit high peak-to-average power ratio (PAPR). In this paper the PAPR of 8x8 MIMO OFDM systems is simulated and is shown with the use of SLM technique and with 8-PSK modulation comprising of 1024 subcarriers and data rate of 792Mbps results in reduction of PAPR up to 4.2753 dB. The architecture utilizes 5% of shift register, 1% of slice LUTs,19% of flip flops, 29 % of IOB's, 3% of BUFG's and 4% of DSP 48Es.**

***Index Terms*— Multiple input multiple output (MIMO), orthogonal frequency division multiplexing (OFDM), peak-to-average power ratio (PAPR), selected mapping (SLM), partial transmit sequence (PTS).**

I. INTRODUCTION

In the present scenario, 3G data rates is not ever growing demands of multimedia services; online gaming etc. The need for more sophisticated technology is possible with higher and faster data transmission and reception. This can be achieved using 4G wireless technology.

MIMO-OFDM is considered as one of the promising solution for increasing high data rates in wireless communication systems. The main limitation of MIMO-OFDM system is its high peak-to average power ratio (PAPR) of the transmitted signals which is required to be reduced [1]. The various PAPR reduction schemes have been proposed for OFDM systems. Among these the dominant type based signal scrambling methods Partial Transmit Sequences (PTS) and Selective Level Mapping (SLM) [2] are attractive as they achieve low PAPR. The SLM is investigated to solve this problem, which selects the transmitted sequence to achieve least average PAPR for higher order MIMO-OFDM systems [3]. The SLM reduces the side information at the expense of a slight degradation of the PAPR performance.

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Section 2 briefs idea of OFDM multicarrier scheme to reduce ISI and increase spectrum utilization. Section 3 describes the system-level architecture of the transmitter [4] and the receiver [5]. Section IV gives detail idea of Simulink model and its parameters. Section V provides the detailed synthesis results for a Xilinx VirtexTM-4 xc4vsx35-10ff668 FPGA implementation and demonstrates that the entire transceiver system will fit onto a single chip.

II. TRANSCEIVER OF OFDM

Figure 1 shows the system model considered in this paper. At the starting end binary data is being inputted to the system. After that this binary data is going through to the process of digital to analog mapping. And this mapped signal is being modulated with proper modulation technique. This modulation signal is than converted into parallel signal by serial to parallel converter. This parallel data is being inputted to the IFFT operation block.

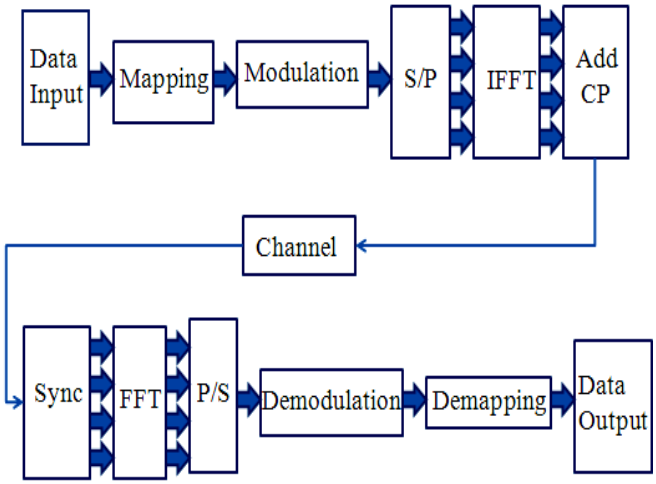

Figure 1 OFDM transceiver block diagram

This IFFT block converts the frequency domain signal to time domain signal for each subcarrier [6]. Cyclic prefix is being added with the time domain signal. After that this time domain signal is being transmitted through the channel after proper filtering and applications [7]. This transmitted signal is received by receiver and the receiver action is inverse of transmitter [8]. The starting end of receiver is a synchronizer. It is being used to equalize the received signal to prevent any channel effect and to get the proper signal.

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III. DESIGN METHODOLOGY

The design methodology used to synthesize each block is depicts in Figure 2. The algorithm of each block in the system is first verified using *Matlab* with double precision floating point. After the algorithms are verified, the hardware implementations are obtained by constructing block diagrams in *Simulink*. For block and system simulations, this method enables us to integrate different components and validate their performance by exploring design trade-offs between different sets of parameters. VHDL and/or Verilog code can also be imported into Simulink via the Xilinx System Generator block set, which gives flexibility to the design flow. Simulink and Xilinx System Generator create bit-true and cycle-accurate hardware models which can be programmed into FPGA prototyping boards [9]. The Xilinx integrated software Environment (ISE) is used as the synthesizer in the design flow diagram shown below. Model Sim can also be used to verify the hardware simulation of the blocks by using test vectors generated by the System Generator or HDL test benches. Finally synthesis and performance results of the blocks are reported using ISE, and bit streams are generated to program the FPGA boards.

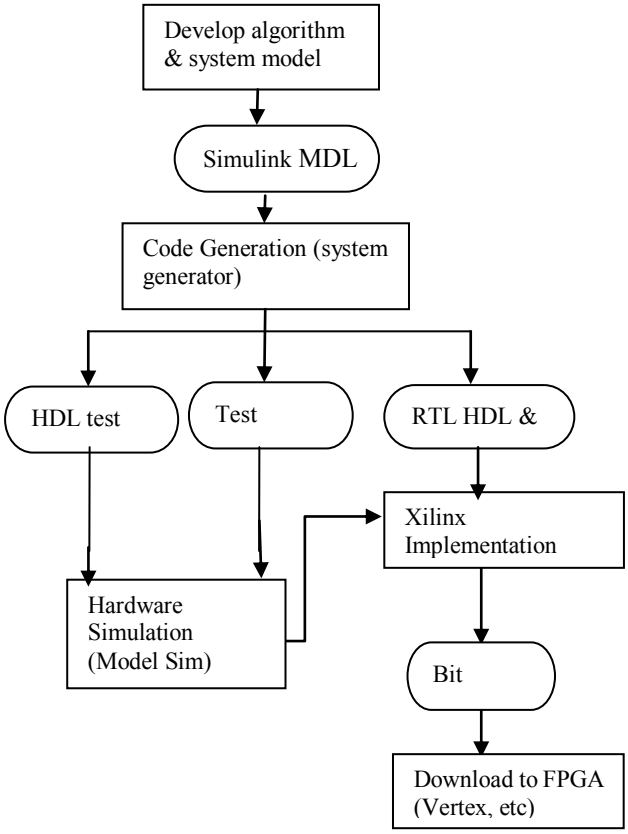

Figure 2 Methodology Diagram

IV. SIMULINK MODEL

The Figure 3 represents the complete 8 × 8 MIMO-OFDM simulink model. A signal is provided at the input by connecting the Gateway In to the workspace with the support of a manual switch. The Gateway_ In block is used to convert input which is of simulink type to Xilinx type [11]. The signal is then connected to the parallel to serial convertor and is later applied to the subsystem.

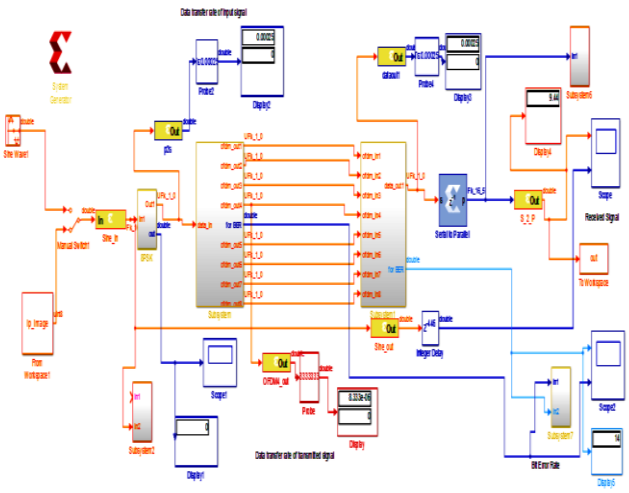

Figure 3 Simulink Model

Table 1 Simulink Parameters used in OFDM

Parameters	**Value**
Error correcting code	Convolution codes
Modulation scheme	8-PSK
Channel	Rayleigh
Interleaver	Random , Matrix
Coding Rate	½
Number of subcarriers	1024
Clock Frequency	100 MHz
Input data rate	792Mbps
Input sampling frequency	3.3 MHz
Data transfer rate	1.111e-08
Output Sampling frequency	99.09 MHz

Input image of size 120 × 120 pixels with resolution of 72 DPI is used for simulation as shown in Figure 4.

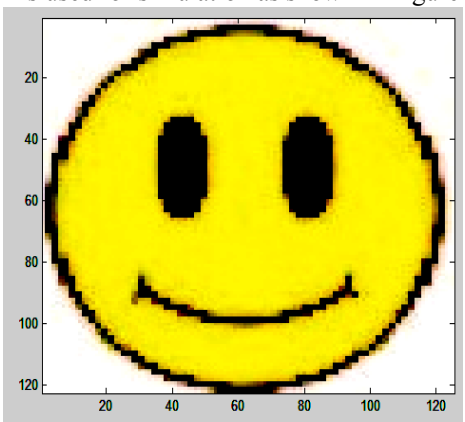

Figure 4 Image used for Simulation

The synthesis results for each block within the transmitter are summarized in Table 2 with the required numbers of slices, flip-flops, look-up tables (including those used for logic, route through and shifted registers), DSP48s and the total equivalent gate count of an ASIC implementation. Several additional blocks in the transmitter are presented in the sections below.

Table 2 Synthesis reports for the transmitter blocks

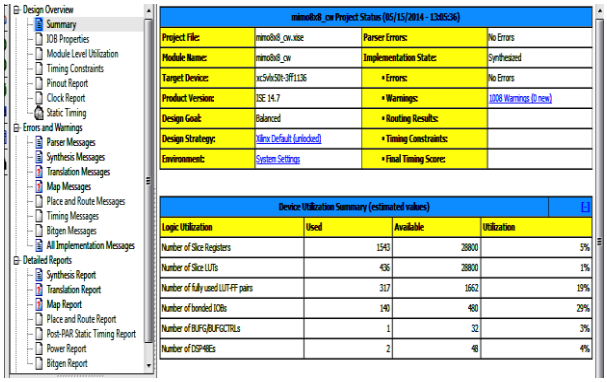

Table 3 depicts estimated values of device utilization which shows the architecture utilizes 5% of shift register, 1% of slice LUTs,19% of flip flops, 29 % of IOB's, 3% of BUFG's and 4% of DSP 48Es.

Table 3 Device utilization summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of shift register	1543	28800	5%
Number of slices LUT's	436	28800	1%
Number of fully used LUT's FF pair	317	1662	19%
Number of bonded IOBs	140	480	29%
Number of BUFG/ BUFGCTRLs	1	32	3%
Number of DSP 48Es	2	48	4%

V SIMULATION RESULTS

A Image output on Scope with and without SLM:

Final output with and without SLM is displayed on scope 1 of Simulink model. Scope 1 output is shown in Fig.ure 5 and Figure 6 where Figure 5 depicts output received for the image without SLM and Figure 6 depicts output received with SLM.

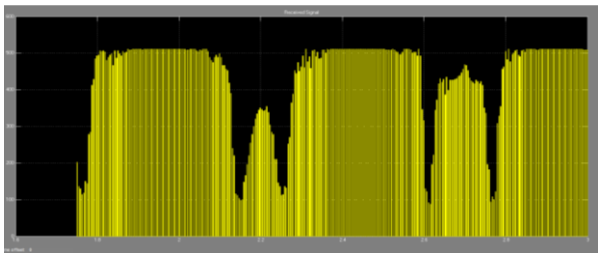

Figure 5 Signal output without SLM

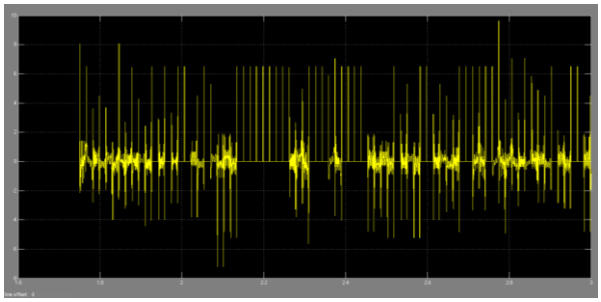

Figure 6 Signal output with SLM

B JTAG Co simulation model:

JTAG model shown in Figure 7 is used for hardware co simulation. In this model input image is given which acts as workspace input. After execution of this model test benches are generated this is shown in Figure10.

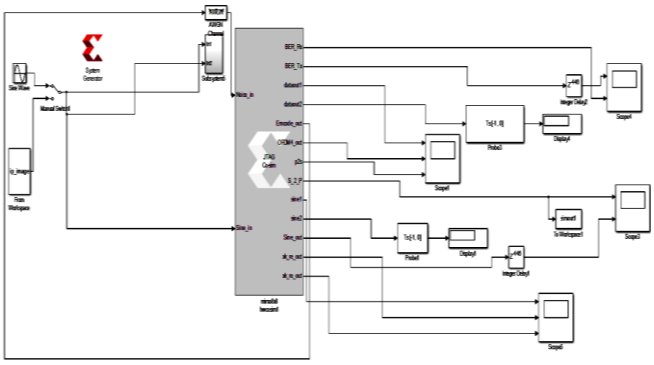

Figure 7 JTAG Co simulation for Image

C RTL Schematic:

In digital circuit design, register-transfer level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers and the logical operations performed on those signals.

Register-transfer-level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived. Design at the RTL level is typical practice in modern digital design.

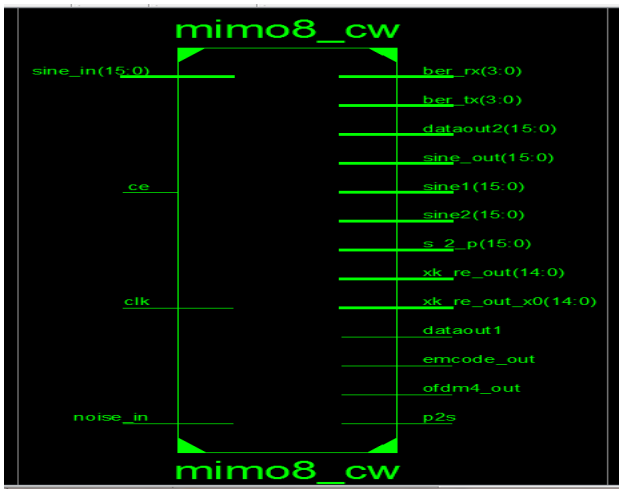

Figure 8 RTL Schematic

When designing digital integrated circuits with a hardware description language, the designs are usually engineered at a higher level of abstraction than transistor level or logic gate level. In HDLs the designer declares the registers (which roughly correspond to variables in computer programming languages), and describes the combination logic by using constructs that are familiar from programming languages such as if-then-else and arithmetic operations. This level is called register-transfer level. The term refers to the fact that RTL focuses on describing the flow of signals between registers.

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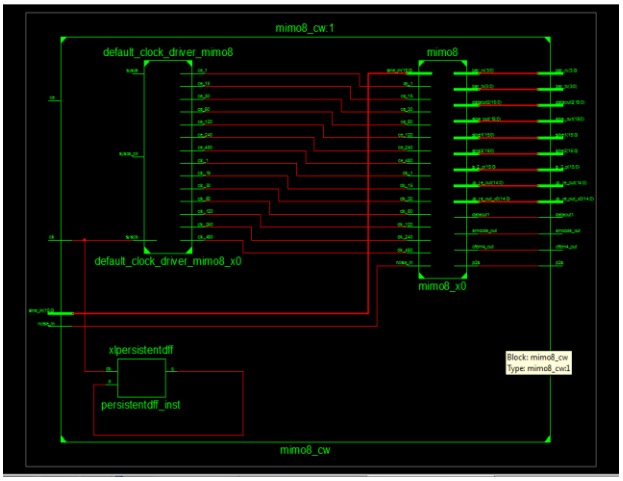

Figure 9 RTL Schematic inside mimo8_cw 1

D Test bench generated for input image:

Test bench is generated by configuring FPGA on JTAG co simulation. Figure 10 shows test bench generated for input image.

Figure 10 Test Bench generated for Image

E PAPR performance for phase variation of 0^0 to 360^0:

PAPR is calculated using Simulink model. Fig.ure 11 shows performance of PAPR for phase shift variation of 0^0 to 360^0 without SLM. Here PAPR reduction of 6.4455 dB is achieved at phase angle of 80^0.

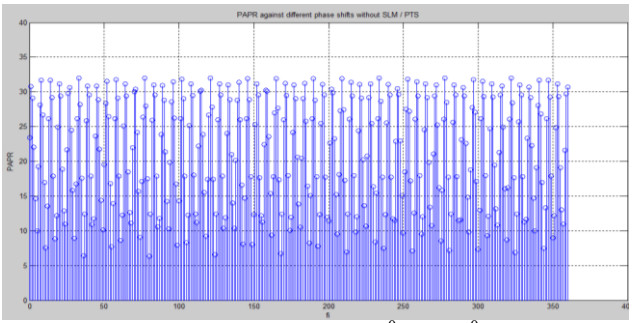

Figure 11 PAPR for phase shift of 0^0 to 360^0 (without SLM)

PAPR for phase shift variation of 0^0 to 360^0 with SLM is shown in Figure 12. Here PAPR reduction of 2.1702 dB is achieved at phase angle of 80^0.

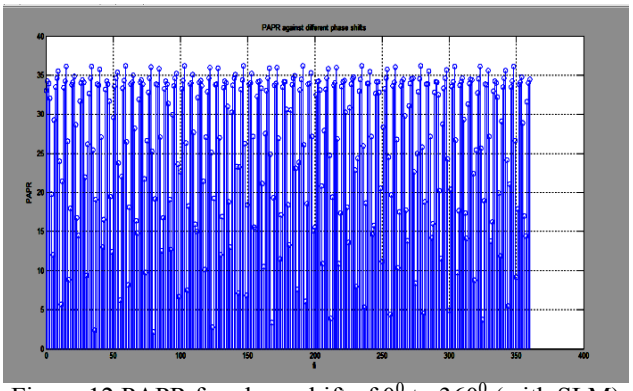

Figure 12 PAPR for phase shift of 0^0 to 360^0 (with SLM)

Table 4 PAPR in dB with different phase shift

Phase shift (in Degrees)	PAPR in dB With SLM	PAPR in dB Without SLM	Reduction in PAPR in dB
1	23.4435	26.206	2.7625
10	26.0162	29.6595	3.6433
30	22.3961	26.1146	3.7185
60	25.0618	28.4518	3.39
80	**2.1702**	**6.4455**	**4.2753**
90	33.8744	35.9054	2.031
120	34.9113	36.6173	1.706
150	20.396	24.2500	3.854
180	10.442	13.9843	3.5423
210	37.8465	39.5457	1.6992
240	35.9002	36.0783	0.1781
270	13.8544	15.4572	1.6028
300	26.3268	27.4487	1.1219
330	37.5996	38.1224	0.5228
360	36.0155	36.4456	0.4301

Above table shows PAPR in dB for phase sequence of 0^0 to 360^0. Lowest PAPR of 2.1702 dB is achieved at phase angle of 80^0 using SLM technique. Without SLM, PAPR of 6.4455 is dB is achieved. Hence reduction of 4.2753 dB is achieved.

F Plot of BER Vs SNR:

Maximum SNR achieved is 6.8 dB where error rate probability is almost zero. Figure 13 shows graph of BER Vs SNR where SNR increases BER reduces.

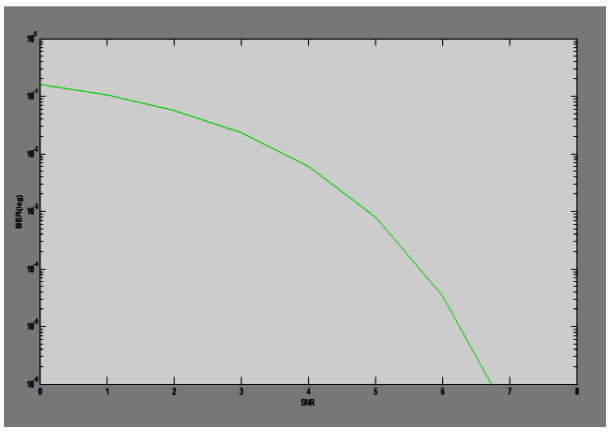

Figure 13 BER Vs SNR

Table 5 BER achieved with variation of SNR

SNR in dB	BER (Probability)
0	0.1587×10^{-6}
1	0.1040×10^{-6}
2	0.0565×10^{-6}
3	0.0230×10^{-6}
4	0.016×10^{-6}
5	0.008×10^{-6}
6	0.006×10^{-6}
7	0.001×10^{-6}

The following conclusions are drawn from simulation results:

1. SLM proposal has significantly improved the PAPR distribution of OFDM system, that is, significantly reduces the probability of large peak power signal.

2. SNR is increased up to 6.8 dB with low error probability.

3. BER probability of 10^{-6} is achieved.

VI RESULTS

SLM is the most promising PAPR reduction technique used in OFDM system. This paper depicts simulation results of OFDM with RTL schematic and synthesis report. The simulation results indicated that large PAPR reduction is possible with selective level mapping for 1024 subcarriers we get PAPR of 4.2753 dB at phase of 80^0. Simulation results demonstrate that SLM provides significant computational complexity reduction cost and better PAPR performance. High speed data transmission up to 792 Mbps is achieved using SLM. SNR of 6.8 dB with BER probability of 10^{-6} is achieved using SLM.

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