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Performance Optimization of CNFET-based Domino Logic circuits

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***Abstract*--- For many years VLSI Chip designers have been using Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). As the channel length of device is reducing, effects like parametric variations and increase in leakage current have caused V-I characteristics to deviate from those of traditional MOSFETs. Hence the development of devices at deep submicron retards to some extent. Carbon Nanotube Field Effect transistors (CNFETs) is one of the most promising device for future Integrated Circuits. Most of the fundamental limitations of traditional MOSFETs are overcome in CNFETs. Domino Logic offers smaller area and higher speed than complementary CMOS design. In this paper circuit performance of CNFET based domino logic circuits is compared with conventional MOSFET. The design of OR, AND and Half adder using Domino Logic are Simulated in Subthreshold region under same channel length and different operational parameters. The main aim of the analysis is to show that the performance of CNFET based domino logic circuit is far better than conventional MOSFETs.**

Keyword— Carbon Nanotube Field Effect Transistors (CNFETs), Domino Logic, Subthreshold region

I. INTRODUCTION

As per Moore's law, for every two years the number of transistors of an integrated circuit is increasing exponentially. Technology scaling has been pursued aggressively to meet the density and sustain the IC predicted by Moore's law. As the physical gate length is reduced to below 65 nm, many device-level effects (such as large parametric variations and exponential increase in leakage current) have substantially affected the I-V characteristics of traditional MOSFETs, thus resulting in major concerns for scaling down the feature size of these devices. A possible approach to meet the challenges of nano scale CMOS consists of utilizing new circuit techniques together with alternative technologies to replace conventional silicon and the current MOSFET-based technology. Recently, there have been tremendous advances in carbon nanotube (CNT) technology for nano-electronics applications.

The Carbon Nanotube Field Effect Transistor (CNFET) is one of the most promising devices among emerging technologies. The CNFET offers many potential advantages with respect to silicon-based technology. Its operation principles and device structure are similar to CMOS, and therefore the mature design infrastructure of this latter technology can be utilized, together with its fabrication process. As reported in the technical literature, the CNFET has been experimentally demonstrated to have excellent current capabilities; an estimate of the performance of CNFETs at single device level in the presence of process related effects and imperfections at 32 nm feature size. In this paper, a performance assessment and comparison against bulk nano CMOS are pursued at circuit level for delay and low power applications. The same gate length is utilized for the transistors of these two technologies. Different logic gates and the often used benchmark circuit of a Half adder are used to investigate the performance of this new technology.

The power consumption of conventional CMOS circuits is composed of dynamic and static parts. If a process is selected with sufficiently high threshold voltages and oxide thicknesses, static dissipation is small and the dynamic dissipation usually dominates while the chip is active. In this case most power consumption comes from dynamic power consumption. The generic Dynamic power model is given by the equation $p=CV^2f$, which represents that power consumption, is proportional to circuit loading (C), supplied voltage (V) and circuit clock frequency (f). The dynamic power is reduced by decreasing the activity factors, the switching capacitance, the power supply, or the operating frequency. Dynamic power consumption is large because the C supplies the circuit's parasitic capacitance during CMOS circuit switching and clock frequency boosting. In most low power techniques, power consumption can be limited by scaling down V and f to the circuit. The V and f can be adjusted as two independent variables. The dynamic logic circuits and especially the well studied domino CMOS circuits are favourable for implementing the high-speed circuits. The performance advantages have made dynamic logic circuits a main implementation option for high performance circuits. Since dynamic circuits inherently provide lower input capacitance and less transistor count than its static counterparts, introducing dynamic circuits in the design results in high speed and compact area.

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II. SUBTHRESHOLD REGION

In conventional CMOS the drain current (I_{DS}) dominates by transport of carrier due to drift but in subthreshold operation diffusion current dominates due to the carrier diffusion between the source and drain regions of the CMOS transistor in weak inversion region. When the gate to source voltage is smaller than but very close to threshold voltage (*Vth*) of the device the I_{DS} is not zero. Rather, a significant amount of I_{DS} still flows between source and drain of an ultradeep submicron (UDSM) device.

For Si-MOSFET, subthreshold leakage current is exponentially depends on gate voltage, threshold voltage and temperature.

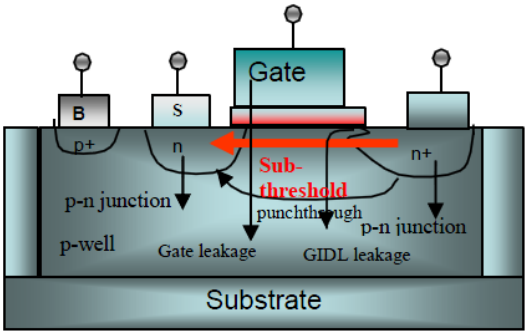

Figure 1. Leakage Effect in MOSFET

III. CARBON NANOTUBE FIELD EFFECT TRANSISTORS

The past few years witnessed a dramatic increase in nanotechnology research, especially in the nanoelectronics field. Among the nanoelectronic devices investigated till date, CNFET seems to have the brightest prospect as per its better electronic characteristics. Speed enhancement due to scaling down to 16-nm and 10-nm technology node has given the impetus to its use. Leakage current, high field effect, short channel effect and lithographic limit problems associated with MOSFET are largely taken care of in CNFET. Also fabrication related issues of CNFET have been solved and hence CNFET-based circuit will surely dominate in the industry in future. CNFET is produced by replacing the channel of a conventional MOSFET by an array of semiconducting carbon nanotubes (CNTs) as shown in Figure. 2. CNT is basically a long, thin allotropic carbon tube which provides a single path between source and drain. CNTs are sheets of graphite rolled into hollow cylinders of diameters varying from 0:4 nm to 4 nm. Depending on the direction in which they are rolled (called chirality) a CNT can be semiconducting with distinct bandgap or it can be metallic with no bandgap. The resulting structure is called single-walled carbon nanotube (SWCNT). If several SWCNTs with varying diameter are rolled concentrically inside one another, then the resulting structure is called multi-walled carbon nanotube (MWCNT), its diameter ranging from several nm to tens of nm. An SWCNT can work as semiconducting or metallic depending on its chirality (n_1; n_2), the direction in which it is rolled up. The CNT acts as metal if $n_1 = n_2$ or $n_1 - n_2 = 3i$, where i is an integer. Otherwise, CNT works as semiconductor.

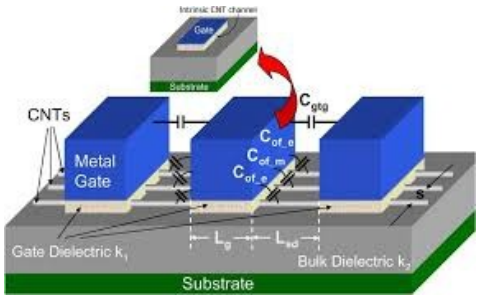

Figure 2. CNFET Structure

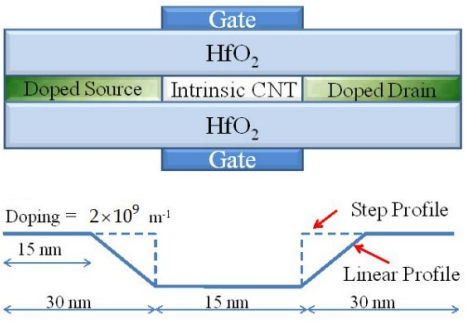

Figure 3. Distribution of Dopants in Channel of CNFET

IV. DOMINO LOGIC

As domino logic design offers smaller area and higher speed than complementary CMOS design, it has been very commonly used for high-performance processors; however, the average power consumption of the domino circuits is larger than that of the static circuit. This power dissipation problem needs to be solved for the domino circuits. The power consumption of conventional CMOS circuits is composed of dynamic and static parts.

It is reported that, the domino circuit has a 42% delay time reduction in comparison with the static circuit. However, the average power consumption of the domino circuit is 95% larger than that of the static circuit. Moreover, the peak current of dynamic circuit is 99% larger than that of static circuit. This power dissipation problem needs to be solved for the domino circuits. A low power voltage scaling technique (LPVS) is used to reduce power consumption for domino circuits without degrading the speed of the circuit. The LPVS module controls PMOS transistors that connect the power supply to the circuit blocks, to degrade the voltage level during

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circuit operation. Numerous PMOS transistors ensure sufficient current supply to the circuit. The PMOS either work in saturation, linear or cutoff region. In linear region, the V_{dd} voltage level applied to the circuit is scalable.

The power consumption of conventional CMOS circuits is composed of dynamic and static parts and is compared with CNFET. If a process is selected with sufficiently high threshold voltages and oxide thicknesses, static dissipation is small and the dynamic dissipation usually dominates while the chip is active and for same channel length. In this case most power consumption comes from dynamic power consumption. The generic Dynamic power model is given by the equation $p=CV^2f$, which represents that power consumption, is proportional to circuit loading (C), supplied voltage (V) and circuit clock frequency (f). The dynamic logic circuits and especially the well studied domino CMOS circuits are favourable for implementing the high-speed circuits. The performance advantages have made dynamic logic circuits a main implementation option for high performance circuits. The Logics can be achieved by integrating the Domino Logic with CNFET which can provide better results. Figure 4 shows the domino AND gate which can be realized by using CNFET. The same technique is applied to realize OR gate and Half Adder which provides basis for other digital circuits.

The circuit operates in two phases. In one phase the output node get charged to V_{dd}. In other phase the output is calculated using the logic. Here the control is provided by the Clk signal. Figure 5 shows the Domino Half Adder. The same analysis can be made for the Adder where separate circuits are designed for SUM and CARRY. For the above circuits circuit parameters like delay, power its product are calculated and compared with the CNFET and MOSFET.

The reason for choosing the AND, OR and Adder is that the adder plays an important role in arithmetic circuits and in multiplications both AND and OR also used.

Logic Family	Power Dealy product(j)			Variance		
	AND	OR	Half Adder	AN	OR	Half Adder
Static CMOS	3.6 E -19	3.5E -19	5.6 E -19	0.91	0.6	3.56
DCVSL	4.5 E -20	4.1E -20	6.5 E -20	2.7	2.5	7.9
Pseudo NMOS	2.9 E -19	2.6E -19	4.9 E -19	0.6	0.5	3.25
Domino CNFET	9.34 E -21	9.2E -21	3.3 E -22	0.24	0.21	2.5

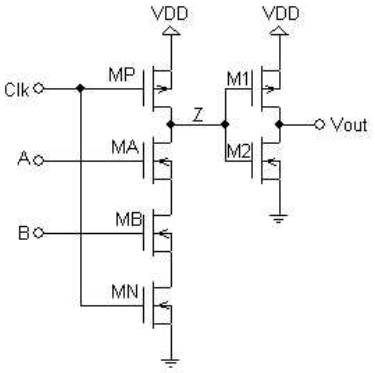

Figure 4. Domino AND Gate

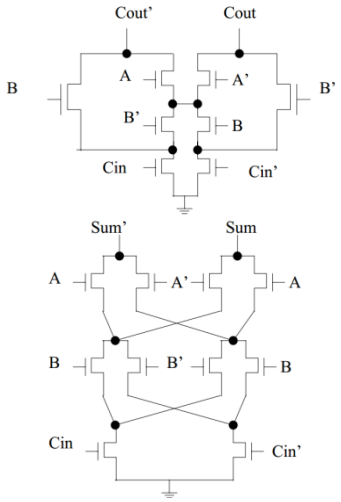

Figure 5. Domino ADDER

V. PERFORMANCE ANALYSIS

This Section presents estimation of various design metrics which are estimated during simulation on HSPICE using the experimentally validated Stanford CNFET model. Here the AND, OR and HALF ADDER is simulated using DOMINO Logic and the Delay and variance of different logics are compared.

Logic Family	Dealy (μS)			Variance		
	AND	OR	Half Adder	AND	OR	Half Adder
Static CMOS	46.11	45.12	89.99	0.94	0.62	4.56
DCVSL	89.16	88.34	102.43	3.7	2.8	7.9
Pseudo NMOS	32.11	31.45	76.7	0.8	0.7	3.25
Domino CNFET	29.34	29.11	65.90	0.34	0.31	2.98

Table 1. Delay and variance

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Table 2. Power Delay Product and Variance

VI. CONCLUSION

The Carbon Nanotube Field Effect Transistor (CNFET) is one of the most promising devices among emerging technologies to extend and/or complement a traditional Si MOSFET. In this paper, delay and power delay product of Si MOSFET and CNFET have been assessed and compared using the same minimum gate channel length for AND, OR and half adder circuit. Simulation results have shown that the DELAY and PDP of CNFET device have compromising results when compared to SI MOSFET.

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