High Speed Low Power Noise Tolerant Multiple Bit Adder Circuit Design Using Domino Logic

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Abstract— Dynamic gates have been excellent choice in the design of high-performance modules such as adders, subtractors, multipliers, registers, multiplexers and comparators in modern microprocessors. However, the main drawback of dynamic gates is their relatively low noise margin compared to that of standard static logic gates. Traditionally, this problem has been resolved by employing a PMOS keeper transistor in the pull up network that compensates for the sub threshold leakage current of the pull-down NMOS network. In the earlier dynamic technologies, the PMOS keeper transistor could improve the reliability of the dynamic gates with minor performance degradation. However, the shrinking device size towards 16 nm along with increasing levels of process variations have reduced the effectiveness of the traditional PMOS keeper transistor approach. In this paper, a 4-bit ripple carry adder circuit is designed using an adaptive keeper technique called rate sensing keeper (RSK) that enables faster switching and tracks the variation across different process corners[14] and its performance is compared with 4-bit adder circuit designed using twin transistor technique and current mirror techniques. In this paper the multiple bit domino adders are implemented with L=0.12µm technology along with a supply voltage of 1.2V.

Index Terms— Domino logic, high-speed domino circuit, leakage power, noise tolerance, transistor sizing.

1. INTRODUCTION

Dynamic logic gates and circuits have been excellent choice in the design of high-performance modules such as multiple bit adders, subtractors, multipliers, comparators, multiplexers, registers, etc in modern VLSI microprocessors [1]. The advancement in fabrication technology along with the shrinking device size has allowed for placement of nearly two billion transistors on Intel’s latest processor [2]. The digital logic gates and circuits designed using dynamic domino technique is considerably faster than the logic gates and circuits designed with standard static logic style. The aggressive technology scaling to improve the performance as well as the integration level makes the noise play a major role in design parameters like area, power and speed [3]. Therefore the digital integrated circuit noise has become one of the most important issues in the design of deep submicron VLSI chips [4]- [9]. The robustness and performance of wide fan-in dynamic circuits significantly degrade with increasing levels of process variations and sub threshold leakage.

A number of design techniques such as PMOS feedback keeper transistor method to prevent the dynamic node floating problem, precharging the internal nodes to eliminate the charge sharing problem and weak complementary p-network is constructed to improve the noise tolerance to the level of skewed static CMOS logic gates, have been developed in the past three decades to minimize the effect of noise in dynamic circuits [6]. It is also shown that voltage scaling aggravates the crosstalk noise in the dynamic circuits and reduces circuit noise immunity, motivating the need for noise-tolerant circuit design [10]-[12]. To design a high performance domino logic circuit, there are two most important factors to be considered when designing a keeper circuit. The first factor is the additional loading caused by the keeper and its control circuits and the second factor is the keeper circuit should be capable of switching off very fast [13]. If the keeper circuit remains ON during evaluation it will compete for longer time with the NMOS network during the pull down process. Designing feedback keeper circuit for wide fan-in gates is a challenging task since the leakage current largely depends on increase in variability [14].

In this paper, a 4-bit ripple carry adder circuit is designed using an adaptive keeper technique called rate sensing keeper (RSK) that enables faster switching and tracks the variation across different process corners[14] and its performance is compared with 4-bit adder circuit designed using twin transistor technique and current mirror techniques. One method to reduce the sub threshold leakage current in the pull down NMOS network is the use of a leakage current replica keeper circuit with proper transistor sizing [15]. This type of domino circuits consists of an analog current mirror to replicate the leakage current of a dynamic gate pull-down stack and thus tracks process, voltage, and temperature. In this paper the effect of temperature on the circuit performance is analyzed in detail by sweeping the temperature from 25°C to 70°C.

The performance of the dynamic circuits can be significantly improved by precise design and properly sizing the transistors. Usually in all the digital circuits the transistor gate length remains uniform. So the size of the transistor in digital circuits depends on the width of the transistor. In this paper the multiple bit domino adders are implemented with L=0.12µm technology along with a supply voltage of 1.2V. The noise sensitivity of the domino circuits depends on the threshold voltage of the transistors used in the circuit and

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since the transistor size is decreasing year by year due to aggressive scaling trends in modern electronics, due to the low threshold voltage, the circuits should be more sensitive to noise that necessitates the use of noise tolerant circuits design techniques. The paper is organized as follows. Section II details the circuit implementation and operation of the 4-bit adder using three different domino techniques. Section III compares the performance of these full adder circuits using the simulated results. Section IV concludes the paper.

1.1 CIRCUIT DESIGN

The circuit diagram of a full adder circuit implemented using current mirror domino (LCR) technique is shown in fig.1 and its layout is shown in fig.2. The full adder circuit implemented using leakage current replica (LCR) keeper domino technique uses an analog current mirror to replicate the leakage current of the pull-down network and it tracks process, voltage, and temperature. The block diagram of the 4-bit adder circuit implemented using the LCR technique is shown in fig.3 and its layout is shown in fig.5. The timing diagram of the 4-bit adder using LCR technique is shown in Fig.4.

Fig.1. Full Adder circuit using current mirror domino logic
Fig.2. Layout of the Full Adder circuit using current mirror domino logic
Fig.3 Block diagram of 4-Bit adder using current mirror domino logic
Fig.4 Timing diagram of the 4-bit adder using high current mirror logic
Fig.5 Layout of the 4-bit adder using current mirror domino logic
Fig.6 Voltage Vs Time waveforms of 4-bit adder using current mirror domino
Fig.7 Effect of temperature on the performance of 4-bit adder using LCR

The output voltage Vs Time characteristic of the 4-bit adder is shown in fig.6. This eye diagram shows the precharging and evaluation of the circuit. In this full adder circuit a current mirror is connected to the keeper which compensates for the sub threshold leakage current of the pull-down network. This current mirror circuit can be shared...
for all the logic gates in the circuit. In this configuration the keeper and current mirror circuit minimizes the delay of the circuit (delay in the order of pico seconds) by minimizing the effect of charge sharing. This circuit need proper selection of clock signal. If the clock frequency exceeds 500MHz, the performance of the 4-bit adder circuit degrades. The effect of temperature on the performance of 4-bit adder circuit is shown in Fig. 7. In this work the temperature is varied from 25°C to 70°C. From the fig. 7 it is clear that as the temperature increases the transition delay also increases due to the increase in leakage current. The circuit is implemented using L=0.12µm technology with VDD=1.2V. The simulation results shows that the circuit performance is superior in terms of speed and power compared to the adder circuits implemented using standard static logic circuit techniques.

The full adder circuit implemented using twin transistor domino technique is shown in figure-8 and its layout is shown in figure-9. The twin transistor technique improve the noise immunity of the full adder circuit by increasing the threshold voltage of the NMOS transistor which is connected to the input through a cross coupled transistor called twin transistor. It has been shown that the full adder circuit implemented using twin transistor technique is more energy-efficient than existing noise-tolerant full adder circuits designed using other dynamic techniques. Since the twin transistors increase the node capacitance of the full adder circuit, the circuit delay will be increased. Twin-transistors also reduce the charge-sharing problem that occurs in dynamic logic circuits. The block diagram of 4-bit adder circuit implemented using twin transistor domino technique is shown in figure-10 and its layout is shown in figure-11. Experimental results show that the full adder designed using twin transistor technique provides a significant improvement in the noise immunity of dynamic circuits with a slight increase in power dissipation and no loss in throughput. The carry outputs of the 4-bit adder implemented using twin transistor technique are shown in fig.12.

Fig.8. Full adder circuit using Twin transistor domino logic style 25°C

Fig.9. Layout of the Full adder circuit using Twin transistor domino

Fig.10. Block diagram of 4-bit adder using Twin transistor domino

Fig.11. Layout diagram of 4-bit adder using Twin transistor domino

Fig.12. Carry outputs of the 4-bit adder using Twin transistor domino

Fig.13. Voltage Vs Time waveforms of 4-bit adder using twin transistors

Fig.14. The pre-charge & Evaluation phases of sum bit S3 in a 4-bit adder
The output voltage Vs Time characteristic of the 4-bit adder implemented using twin transistor domino logic style is shown in fig.13. The pre-charge and evaluation phases of the sum bit s3 of a 4-bit adder circuit designed using twin transistor domino logic style are shown in Fig.14. As the clock frequency increases the output voltage decreases due to the parasitic capacitances. The operation of the circuit is as follows. When clock goes low, the dynamic node will be precharged to VDD (precharge phase) and the output remains low in this condition. When the clock signal changes the state from low to high the circuit evaluate the logic function (evaluation phase). The circuit consume an additional 10 – 15 % power to improve the noise tolerance. Another limitation of this circuit is in terms of the area.

The full adder circuit implemented using rate sensing keeper (RSK) technique is shown in figure-15 and its layout is shown in figure-16. The full adder circuit implemented using rate sensing technique works based on the difference in the rate of change of voltage at the dynamic node of the circuit during the ON and the leakage condition and the average of these two rates called reference rate is used to control the keeper transistor. This technique helps to achieve high speed and low noise. The pin diagram of the full adder module constructed using RSK technique is shown in fig-17. This full adder has an extra input terminal called Vbias terminal. The block diagram of the 4-bit adder circuit designed using RSK technique is shown in Figure-18 and its layout is shown in Figure 19. This circuit is also simulated using L=0.12µm technology with VDD=1.2V. The simulation results show that the 4-bit adder implemented using RSK technique gives superior performance compared to the other alternatives such as Conditional Keeper (CKP) and current mirror-based keeper (LCR). The power and current Vs Time characteristic of the 4-bit adder implemented using RSK domino style is shown in fig.20 and the timing diagram of the 4-bit adder implemented using RSK logic style is shown in Fig.21.

In this paper three types of four bit adders are presented with L=0.12µm technology and with a supply voltage of 1.2V. These high performance domino styles improve the scalability of multiple bit domino logic adders. Using these methods it is possible to implement the adder circuits with a transistor gate length of L=16nm along with a supply voltage of 0.8V. These adder circuits are superior in performance compared to conventional static logic adders. These adder circuits minimize the chip area, minimize the leakage power, and improve the noise tolerance without much speed degradation. Also the delay between the gates is now reduced to the order of pico seconds. These types of domino logic circuits can be used in high performance microprocessors.
2. SIMULATION RESULTS

The simulations were performed using $L=0.12\mu m$ technology along with the supply voltage $V_{DD}=1.2V$. In this paper a 4-bit adder is constructed using three different domino techniques such as leakage current mirror keeper, twin transistor method and rate sensing keeper. Since a single current mirror structure can be shared among more than one domino logic circuits, the LCR technique is useful for constructing wide fan in circuits such as multiple bit adders, registers, multiplexers etc. This adder circuit has the area overhead of an extra NMOS transistor which is connected to the keeper from the current mirror circuit. This adder circuit has much better noise margin, low leakage current and low power consumption compared to the adder circuits designed using domino logic styles with traditional feedback keepers. The adder circuit designed using twin transistor domino logic has very good noise immunity but it consumes some additional power due to the twin transistors. The power time characteristics of the 4-bit adder circuit designed using various domino logic styles is shown in figure-22.

3. CONCLUSION

As the technology scales down, the leakage current of the pull down evaluation network increases, especially in wide fan in dynamic gates such as wide OR gates, wide AND-OR gates used in microprocessors. This will increase the power consumption and reduce the noise immunity. In this paper the performance of 4-bit adder circuit designed using three domino circuit techniques (LCR, Twin Transistor logic, and RSK) is analyzed in detail and its performance is compared with other adder circuits. The 4-bit adder circuit is simulated using $L=0.12\mu m$ technology along with supply voltage $V_{DD}=1.2V$. The experimental results shows that these adder circuits gives superior performance compared to adder circuits designed using conventional domino techniques.

REFERENCES


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