International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 3, Issue 10, October 2014

# A low power Custom DSP with a Programmable Truncated Multiplier

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***Abstract*—Most signal processing application performs truncated multiplication in order to reduce the growth in word size. When direct truncation is used it provide significant savings in power, area, complexity and timing at the same time introduces large amount of error in the output. so here in this paper a programmable truncated multiplier(PTM) is presented that enables programmable truncation .In a PTM a full width multiplier is implemented but the number of bits to be truncated can be decided at run time depending on the application . This is achieved by selecting the active sections of the partial product matrix dynamically at run time. The PTM provide reduction in the dynamic power consumption. Efficient design and implementation of the PTM in a custom DSP processor is also presented. Experimental results and power measurements are obtained after implementing the system in a sparten 3e device.**

***Index Terms*—PTM, ALU, Custom DSP.**

## I. INTRODUCTION

Within every DSP systems multipliers are the most important as well as fundamental building blocks in terms of power consumption. Also multiplication is frequently required in signal processing applications. Normally in signal processing truncation is performed to avoid the growth in word size. The increased demand for portable communication and computing devices and also the advances in mobile multimedia systems has made the systems. In a direct multiplier implementations [1] of an n x n bit multiplication yields a 2n-bit product. so the DSP architecture would need an ever-growing bit width in order to keep the full accuracy of the system that would be impractical to implement. In order to avoid this the results are usually rounded down or truncated to keep the results within the limits of the bit width of the DSP architecture. In this paper the architecture for the PTM describes a full precision multiplier in which the elements of the partial product matrix can be disabled in a column wise manner through an external control word .These disabled columns in the partial product matrix provide the reduction in the dynamic power consumption. The advantages of the PTM include

- Dynamic power reduction
- Flexibility on accuracy selection

The paper is organized as follows. Section II presents a review of truncated multiplication. The proposed architecture of the PTM is presented in Section III. Section IV describes the custom DSP . In Section V the simulation results are analyzed. Section VI describes the implementation results and the power measurements. Finally, the conclusion section VII summarizes the effectiveness of the architecture presented .

## II. TRUNCATED MULTIPLICATION

In systems where it is not essential to compute the exact least significant part of the product of multiplication ,truncated multipliers achieve power, area and timing improvements by skipping the computation of of the least significant part of the partial product matrix. Instead of computing the full-width output, the output results from the sum of the most significant column.. Direct truncation is the simplest scheme to obtain a truncated multiplier by removing the lower columns of the partial product matrix that form the least significant part of the product result. Thus truncation helps in reducing the complexity of the multiplier unit by eliminating the lower parts of the partial product matrix. But this kind of direct truncation introduces most of the error in the lower weighted bits of the output that are eliminated when converting the product output back to the original bit width. By performing this kind truncation significant savings in power and complexity can be achieved, at the expense of signal degradation. By direct truncation the multiplier requirements are almost halved in both area and power, at the price of large errors.

## III. PROGRAMMABLE TRUNCATED MULTIPLIER

Generally DSP systems need flexibility to support the generation of large output results where the magnitude of the output is bigger than the multiplier inputs. They also need to deal correctly with the small size operands. But in direct truncation it was not possible to deal with small size



ISSN: 2278 – 909X 

operands. The multiplier architecture proposed here implements a full width 16x16 multiplier and within which the truncation is made programmable. That is the number of bits to be truncated can be decided at runtime by selecting the active section of the partial product matrix through an external control word. Thus the architecture presented in this paper provides a method to adjust the active width of the multiplier in a column-wise manner ,thus allowing a flexible truncation scheme which makes the system capable of adapting the power consumption as per requirements of the application. The following equation represents a programmable truncated multiplication.

$$P_{PTM} = X * Y$$
$$= 2^{1} + 2^{-N} + \sum_{i=0}^{N-2} \sum_{j=0}^{N-2} t(i+j).ppt[i,j].2^{i+j-2N+2} \quad (1)$$

Equation 1 represents the truncated multiplication for signed numbers. Where $t_{(i+j)}$ is the control input of size( 2N-1) and ppt(i,j) is the terms in the partial product matrix. The column-based controllability of the partial product terms is achieved by replacing the 2-input AND gates by 3-input AND gates. And every 3 input AND gate have the inputs $a_i$, $b_j$ corresponding $t_{(i+j)}$ bit. So when the truncation is made programmable it will results in a maximum area penalty of 20% of the partial product matrix. It is the value of the vector **t** that determines the number of bits to be truncated or the truncation level. In the case of an 8x8 multiplier if the value of t=0x7fff ,then there will not be any effect of truncation in the output. If value of t=0x7f00 then LSB of the partial product matrix is disabled which is same as that of direct truncation. So by selecting a suitable value for 't' we can have any level of truncation.

## IV. ARCHITECTURE OF THE CUSTOM DSP

Here a custom DSP with a programmable truncated multiplier is presented so as to analyze the advantages as well as disadvantages of the DSP in terms of truncation error and power reduction benefits. The DSP is designed with a minimum control logic. Within the DSP system the arithmetic and logic section is the most important and distinct part that includes the PTM. The PTM provides the dynamic power reduction benefits also makes the DSP system capable of adjusting the accuracy as per the requirements of applications. Fig.1shows the architecture of the custom DSP. It consists of a control unit that operates in a 5 stage pipelined mode, program memory, two data memory blocks, ALU and finally the input and output port. The following gives the description of the main components of the DSP architecture.

*1)Control unit :* The control unit is a simple 5 stage pipeline which fetches and decodes the instruction also controls the data flow ,controls the ALU operations.

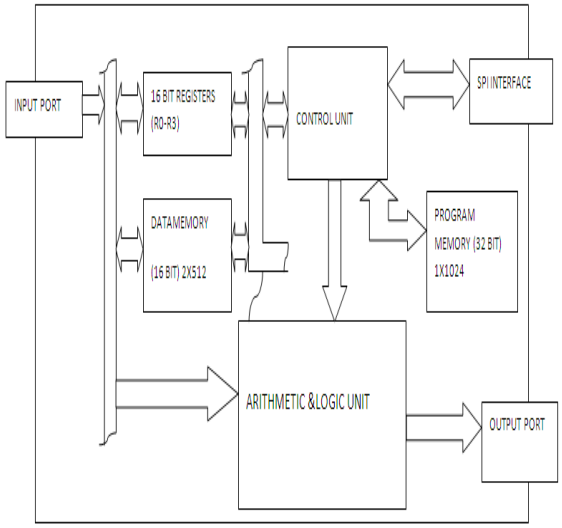


Fig 1: Custom DSP architecture

. The main aim of the design of the control unit is to reduce the power consumption of the internal blocks other than the arithmetic block. it allows the access of two data memory blocks and the program memory block during the instruction read operation.

*2)Custom Instruction Set***:** `a custom instruction set is implemented for the DSP so as to maximize the utilization of the ALU. This will help in optimizing the power reductions offered by the programmable truncated multiplier. All the Instructions designed are 32 bits wide. The set of instructions include

- *Arithmetic and logic instructions :* The Arithmetic &Logic subset of instructions is displayed in Table I and Table II. The arithmetic instruction include addition operation, subtraction, multiplication with and without truncation and also other operations such as multiply and accumulate operation, shifting and rotation of the accumulator output also squaring of the accumulated value. All the arithmetic instructions utilizes the arithmetic unit effectively. logic instructions performs all the logic operations.
- *Flow control instructions:* the flow control instructions include instructions for jump operation, loop operations. Table III presents a list of such instructions.
- *Dataflow instructions:* Data Flow instructions are described in Table III. It include instructions for storing and loading data to and from different memory blocks.



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TABLE I: Set of Arithmetic instructions

| Mnemonics | Commands |
|---|---|
| ADD | 10XXXXXX |
| ADD_RD | 13XABBBB |
| SUB | 14XXXXXX |
| MULT | 20XXXXXX |
| MULT_T | 21XXXXXX |
| MULT_RD | 23XABBBB |
| MAC | 30XXXXXX |
| MAC_T | 31XXXXXX |
| MAC_RD | 33XABBBB |
| MAC_RD_T | 34XABBBB |
| SQUARE_ACC | 32XXXXXX |
| SHIFT_ACC | 90XXABCC |

TABLE II : Set of logic instructions

| Mnemonics | Commands |
|---|---|
| NOT_A | 91XXXXXX |
| NOT_B | 92XXXXXX |
| AND_AB | 93XXXXXX |
| OR_AB | 94XXXXXX |
| NAND_AB | 95XXXXXX |
| NOR_AB | 96XXXXXX |
| XOR_AB | 97XXXXXX |
| XNOR_AB | 98XXXXXX |

TABLE III : Set of flow control &data flow instructions

| mnemonics | commands |
|---|---|
| DATA_OUT | 61XXXXXX |
| REG_W | 60XABBBB |
| STORE_ACC | 70XXXXXX |
| STORE_IN_A | 71XXXXXX |
| INTO_ACC | 72XXAAAA |
| NOP | 00XXXXXX |
| JMP | 40XXXAAA |
| LOOP | 80XXAAAA |
| MEM_JMP | 50AAABBB |
| MEM1_JMO | 52XXXAAA |
| MEM2_JMP | 53XXXAAA |
| END_SIM | FFFFFFFF |

*3)Memory blocks :*The memory blocks include two data memory blocks a program memory block. Each data memory is of size 512 x16 bits and the program memory is of size 1024x32 bit. The data memory is used to store and load data, .and program memory is used to store the instructions. it is possible to access all the three memory blocks in a single clock cycle.

*4)Arithmetic and logic unit:* The ALU contains the 16 bit programmable truncated multiplier, a 40 bit carry select adder a 40 bit barrel shifter/rotator and a 40 bit accumulator. the ALU has a multiply and accumulate structure. . A block diagram of the Arithmetic Unit is displayed in Fig. The arithmetic unit consists of

- PTM : The PTM is designed to operate as a standard 16x16 bit multiplier that enables a programmable truncation. For that it includes an extra control input for enabling and disabling the columns in the partial product matrix. Thus the extra control input 'truncation control' is used to control the truncation level of the multiplier.

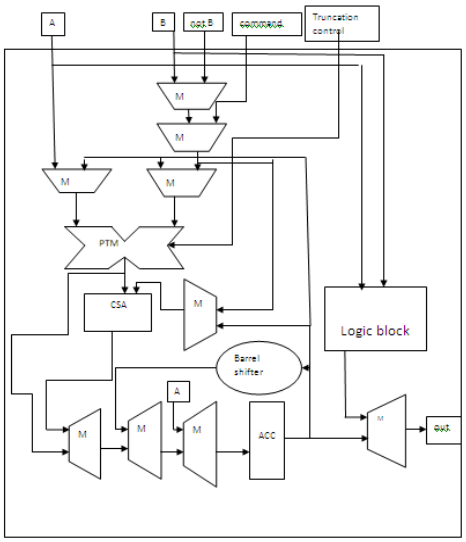


Fig 2 . ALU architecture

- Barrel shifter: a 40 bit barrel shifter/rotator is used for shifting as well as rotating the accumulated output. The shifter performs left shifting, left rotation, right shifting and right rotation on the 40 bit accumulator output.
- Accumulator : A 40 -bit accumulator stores the final result of the arithmetic operations. It is constructed from D flipflops.
- Carry Select Adder: A 40- bit carry select adder is used for addtion as well as subtraction operations. The carry select adder is a simple but high speed adder.

The logic unit performs all logic operations on the two input data.

## V. SIMULATION RESULTS

Xilinx ISE Design Suite 14.2 platform is used for the simulation and synthesis of the proposed architecture. The hardware description language verilog HDL is used for implementation of the proposed architecture.

Fig 3 . Simulation result for the PTM

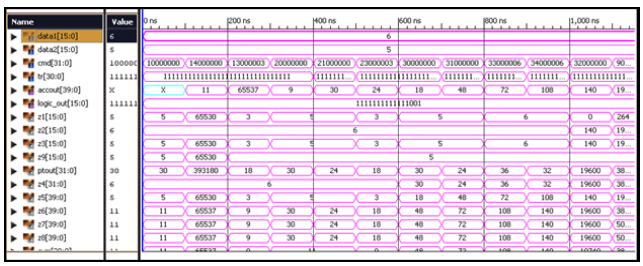

Fig 4. Simulation result for the ALU



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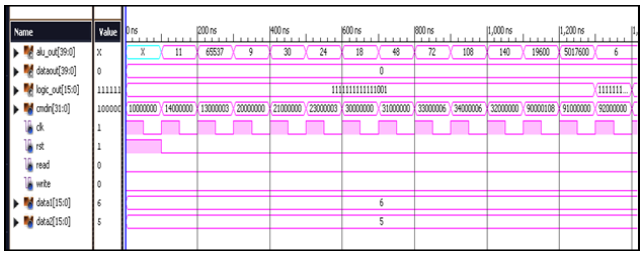

Fig 5.Simulation result for the DSP

## VI. IMPLEMENTATION AND POWER MEASUREMENTS

One of the Important aim of the proposed DSP architecture is to reduce the dynamic power dissipated by the 16x 16 multiplier. The programmable truncation implemented in the multiplier could provide the dynamic power reduction benefit to the whole system. Xilinix ISE Design Suite 14.2 platform provides a XPower Analyzer tool for estimating the total static and dynamic power utilized by the whole system. The power consumed by the standard 16x16 multiplier is compared with power consumed by the proposed 16x16 programmable truncated multiplier. The static power dissipated in both cases is the same. But the dynamic power dissipated by the proposed system was less than that of the old one .The Dynamic power consumed by the standard 16x16 multiplier is 0.006 W while that of proposed PTM architecture is only 0.002W.Thus, by analyzing the power report, it is clear that significant amount of dynamic power reduction is achieved by the PTM architecture.

The proposed DSP Architecture is implemented in Xilinx Spartan 3E FPGA.

## VII. CONCLUSION

Here a new method for truncation is presented and also compared with the previous methods. The use of programmable truncation provides dynamic power reduction benefits in the custom DSP presented here. Such a DSP multiplier is efficiently designed as well as implemented in a custom designed DSP. The multiplier with programmable truncation can be used in applications where accuracy and power consumption of the system is needed to adjust as per the requirements of applications.

## ACKNOWLEDGMENT

I would like to acknowledge the great support of the electronics and communication Engineering department, MACE for the technical facilities. I am also thankful to my beloved guide Mr.Thomas George (associate professor MACE) for the valuable guidance and encouragement which made me to complete the work successfully. Above all, I thank God Almighty for giving me strength, courage and blessings to complete this work.

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ISSN: 2278 – 909X 