

A FIR Algorithms Frequency Error Measurement of Source Signal Using a Digital Signal Processing Technique

Vivek Bargate, R.M. Potdar

Abstractt — This paper describes the design, computational facets, and implementation of a digital signal processing technique for finding error of operating frequency of source signal (like power system) dedicated to protection for error limit. This paper examines the effectiveness of the technique and presented some results from simulation. The proposed method estimates the off-line mode errors which occur while measuring off-nominal frequency.

Index Terms— Digital Signal Processing, frequency measurement, frequency Relay, digital method, power system measurement.

I. INTRODUCTION

FREQUENCY is an important operating parameter of a power system. Frequency of a power system remains constant if sum of all the loads plus losses equals total generation in the system. However, the frequency starts to decrease if total generation is less than the sum of loads and losses. On the other hand, the system frequency increases if total generation exceeds the sum of loads and losses. It is essential that the frequency of a power system be maintained very close to its nominal frequency, i.e., 60 Hz in North America and 50 Hz in Europe. The frequency changes that can be tolerated in a system are governed by the characteristics of the rotating equipment in the system. As an example, the steam turbine blades develop resonance, if operated in the vicinity of its rated speed that can damage the blades. The normal frequency levels should, therefore, be maintained as quickly as possible. For this reason, the North American Electric Reliability Council (NERC) provides operating criteria and guidelines to keep power system interconnection frequency at 60 Hz. A decrease in system frequency also reduces the reactive power supplied by capacitors, transmission lines, etc., and, therefore, upsets the reactive power balance and affects the voltage levels. The above discussion indicates that the system frequency should be maintained at its nominal frequency. If it deviates from nominal value, corrective actions should be taken. Under frequency and over frequency relays are provided in a power system. Under frequency relays are used to automatically shed blocks of loads for restoring the frequency to its nominal value. When generation in a system exceeds the load and losses, the frequency increases above the nominal frequency. Over frequency relays are used to detect this condition and shed some generation. Also, when a generating unit is suddenly separated from the system, its speed increases and the unit can be damaged. Over frequency relays are used to

detect this situation, and take corrective measures. Frequency relay having a measurement range from 40 Hz to 70 Hz are adequate for over- and under-frequency relaying. Frequency relays presently used are of electromagnetic, solid-state and microprocessor types. Accuracy of electromagnetic relays range from 0.1 to 0.2 Hz of the set frequency. Solid-state relays measure time duration between zero crossings and are adversely affected by presence of distortion and noise which shift the zero-crossings and create multiple zero-crossings. Microprocessor relays use algorithms that process the sampled and digitized values of the system voltage to estimate the frequency. These techniques are adversely affected by the presence of harmonics in the signals. Also, they may take from 50ms to few seconds to provide accurate estimates of the frequency. It is necessary to detect under frequency and over frequency condition very quickly so that necessary corrective actions can be taken. Quick estimation of frequency would provide extra time at the hands of operators to take corrective actions. On the other hand, accurate estimates aid in determining the correct loads and generation that has to be shed. Therefore, the problem is that of fast and accurate determination of the frequency of the power system using voltage waveforms which may be corrupted by noise and harmonic components. Recently, adaptive algorithms which may provide faster estimates of the system frequency have been proposed. However the algorithm proposed in requires considerable computational resources and, therefore, cannot be economically implemented with the presently available technology. This paper presents a technique for frequency estimation that provides accurate estimates in about 25 ms and requires modest computations. Theoretical basis and practical implementation of the technique are described. The proposed technique was tested using voltage signals obtained from a dynamic frequency source and from the Sask Power system. Test results demonstrating the performance of the proposed technique are included .

II. THE PROPOSED TECHNIQUE

The technique uses digitized values of samples of the voltage taken at a prespecified sampling rate. Consider a voltage signal having a fundamental of frequency of f_0 . The signal may also contain harmonics and noise. It is possible to use orthogonal FIR digital filters to extract real and imaginary parts of the fundamental frequency component of the signal .These filters must be designed so that they minimize noise effect and are not affected by the presence of harmonics. This means that the frequency response of the filters must have nulls at the harmonic frequencies that are expected to be

present in the signal. The procedure for designing such filters is discussed in the following paragraphs. Consider that the desired FIR filter is of length n and has real values coefficient a_0, a_1, \dots, a_{n-1} . The frequency response of the filter can be expressed as

$$H(z) = \sum_{k=0}^{n-1} a_k z^{-k}$$

For a frequency response corresponding to a frequency of f , the following two equations can be written:

$$\text{Re} \left[H \left(e^{-\frac{j2\pi f}{F_s}} \right) \right] = \sum_{k=0}^{n-1} a_k \text{Re} \left[e^{-\frac{j2\pi f}{F_s}} \right] \quad (2)$$

$$\text{Im} \left[H \left(e^{-\frac{j2\pi f}{F_s}} \right) \right] = \sum_{k=0}^{n-1} a_k \text{Im} \left[e^{-\frac{j2\pi f}{F_s}} \right] \quad (3)$$

Where Re and Im are the operators that provide real and imaginary parts, respectively, and F_s is the sampling frequency. Consider that there are m such frequencies at which the frequency response is defined. This will provided $2m$ equations which can expressed in matrix form as follows:

$$[H] = [A][a] \quad (4)$$

$(2m \times 1)(2m \times n)(n \times 1)$

It is clear that (4) can be solved to determine the coefficients of the desired filter as follows:

$$[a] = [A]^\# [H] \quad (5)$$

Where $[A]^\#$ is the pseudo-inverse of matrix $[A]$ and is given by $[A]^\# = [[A]^T [A]]^{-1} [A]^T$.

It is, therefore, possible to us and the desired frequency response at the selected frequencies to determine the filter coefficients. For designing a filter that extracts the real part of the fundamental frequency component, the magnitude of the frequency response must be unity at fundamental frequency and, zero at dc and harmonic frequencies. The phase shift at all frequencies should be zero. Similarly, a filter that extracts the imaginary part of the fundamental frequency component can be designed by considering that the magnitude of the frequency response is unity at fundamental frequency and, is zero at dc and harmonics frequencies. The phase shift is 90° at fundamental frequency and is zero at dc and other frequencies. It is clear from the above discussion that the design of filter requires that the following parameters be specified.

1. Sampling rate
2. The harmonics components that need to be eliminated and hence the value of m .
3. Filter length (n) which also equals the number of consecutive samples of the voltage signal needed to

compute real and imaginary parts. These consecutive samples are also termed as data window.

Sampling rate is fixed by the application. Generally, in power system measurement and control applications, a sampling rate in the range of 600Hz to 1440Hz is used. Composition of the signal is assumed based on the prior knowledge of the voltage waveforms and their harmonic content. The data window size affects the noise suppression capabilities. It can be seen from (4) that the minimum data window size or filter length (n) must equal $2m$. However, to achieve better noise suppression capabilities, the data window size should be larger than $2m$. The larger the data window, the better is the noise suppression capability of the filters. On the other hand, a large data window means more delay in the filter output. This signifies that a compromise between filter's delay and its noise suppression capabilities is required.

The filter coefficients are multiplied with the corresponding samples of the voltage signal with in a data window and the result are accumulated. Multiplication and accumulation using the filter's coefficient provide the real and imaginary parts of the fundamental frequency component of the signal. The real and imaginary parts computed using samples corresponding to the n^{th} data window can be used to represent the signal in the phasor form, i.e., \bar{V}_n , as follows:

$$\bar{V}_n = V_{rn} + jV_{in} \quad (6)$$

Where V_{rn} and V_{in} are the real and imaginary parts computed using samples from the n^{th} data window. As the next sample arrives, the data window is shifted by one sample. The real and imaginary parts of the fundamental frequency phasor, $V_{r(n+1)}$ and $V_{i(n+1)}$, corresponding to the $(n+1)^{\text{th}}$ data window can be computed using the data from the $(n+1)^{\text{th}}$ and the filters' coefficient as discussed earlier. Fig.1 depicts the fundamental frequency phasors corresponding to n^{th} and $(n+1)^{\text{th}}$ data windows.

As the phase angle difference, $(\theta_{n+1} - \theta_n)$, represents the rotation of the phasor as data window is advanced by one sample. The amount of this rotation can be estimated by using real and imaginary parts of the phasor corresponding to n^{th} and $(n+1)^{\text{th}}$ data windows as follows:

$$\theta_{n+1} - \theta_n = \tan^{-1} \left[\frac{V_{rn} V_{i(n+1)} - V_{in} V_{r(n+1)}}{V_{rn} V_{r(n+1)} + V_{in} V_{i(n+1)}} \right] \quad (7)$$

This rotation for a phasor having fundamental frequency of f_0 will equal to

$$(\theta_{n+1} - \theta_n) = (2\pi f_0) / F_s \quad (8)$$

However, (8) is only true if the phase angle θ_{n+1} and θ_n are computed by using the filters which are designed by assuming the fundamental frequency of the signal being equal to f_0 . In spite of this, (8) forms the basis for frequency estimation and estimate of the frequency, \hat{f} , can be obtain as follows:

$$\hat{f} = (\theta_{n+1} - \theta_n) / (2\pi / F_s) \quad (9)$$

One of the following two situations can exist.

- 1) The estimated frequency is equal to the fundamental frequency assumed for designing the filters that computed the phase angles difference $\theta_n - \theta_{n+1}$. This means that the estimated frequency is also the fundamental frequency of the signal.
- 2) The estimated frequency is not equal to the fundamental frequency assumed for designing the filters. This means that the estimated frequency is not the fundamental frequency of the signal. However, to achieve situation I, the phase angle difference needs to be calculated using filters which are designed by assuming the fundamental frequency being equal to the fundamental frequency of the signal. This can be achieved by using an iterative procedure as follows:
 - a) Design new filter by assuming the fundamental frequency of the frequency obtained from (9).
 - b) Compute the phase angles rotation, $\theta_{n+1} - \theta_n$, by using (7), the filters designed in step i), the samples corresponding to data window n and $(n + 1)$.
 - c) Estimate the frequency using (9) and the phase angles rotation compute in step b).
 - d) Check if the estimated frequency from step c) is equal to the fundamental frequency assumed for designing the filters in step a). If it is, the estimated frequency step c) is the fundamental frequency of the signal. Other the process reverts to step a).

III. IMPLEMENTATION

The proposed technique was implemented by using a DSP based general-purpose hardware which has been designed and developed at the University of Saskatchewan for implementing microprocessor-based relays. Fig. 1 shows the major blocks of the hardware. The hardware consists of isolation and analog scaling and microcomputer blocks. The isolation and analog scaling block consists of pluggable modules for processing voltages and current signals. The functions of this block are to reduce the levels of the signals, convert current signals to equivalent voltage signals and isolate the microcomputer block from the power system

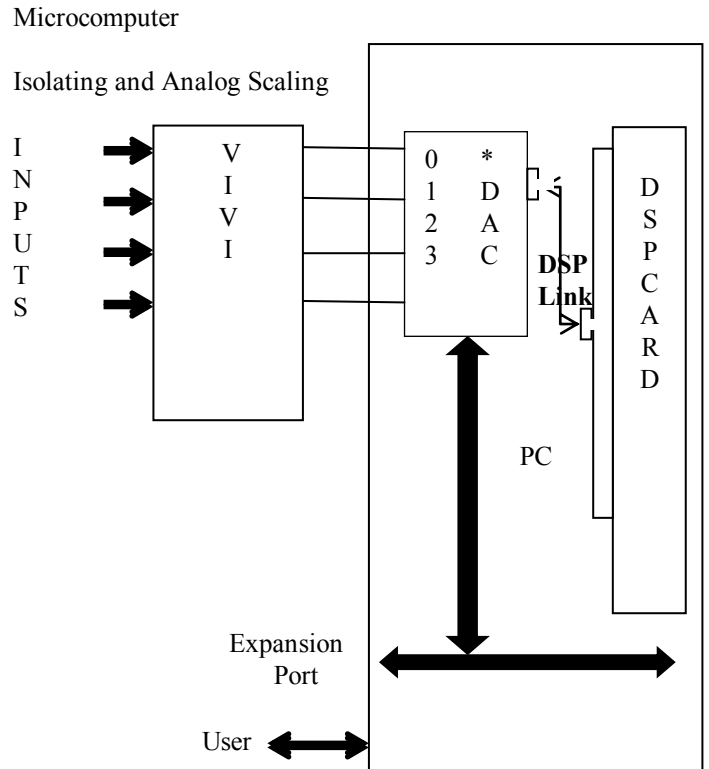


Fig. 1 Block diagram of DSP-based hardware used for implementing the proposed technique

The microcomputer block consists of a data acquisition card, a DSP card and MS-DOS-based host computer. The data acquisition card has anti-aliasing filters, four samples and hold amplifiers, a multiplexer and a 12-bit A/D converter and, therefore, can sample and digitize four signals. The DSP card is based on Texas Instruments TMS32030 floating point digital signal processor.

The software was divided into two parts; data acquisition software and frequency estimation software. The data acquisition software sampled and digitized the voltage signal at a rate of 720 Hz. The digitized values were presented to the frequency estimation software that implemented the proposed technique. The software was written in C language and, after compilation and assembly it was downloaded to the DSP card. Floating-point arithmetic was used in the implementation.

Benchmark tests were performed to determine the execution time of the software implementing the proposed frequency estimation technique. It was found that the software executed in about 1.2 ms when the number of iterations performed in one sampling interval was set at 2. This is well within the available inter sampling time of $(1/720)$ s, i.e., 1.3889 ms and, therefore, the software was set to perform 2 iterations in a sampling interval. The initial estimate of frequency was assumed to be 60 Hz.

IV. SIMULATION RESULT

Step-1 Find out the frequency of selected signal and to compute error for various sampling frequency.

Enter the value of power frequency = 50Hz

Enter the value of Vmax =700

Enter the value of sampling frequency =5000HZ

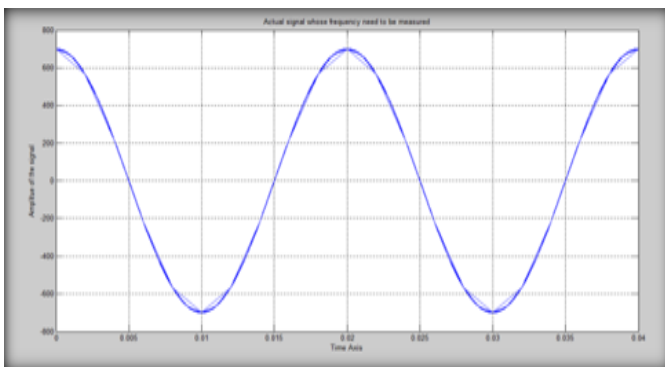
Enter the max harmonic no that you want in your signal =1

- When the value of power frequency taken as 50Hz and also consider the first harmonics in the

S .No.	Power Frequency	Sampling Frequency	Output Frequency	Error
1	50Hz	500	50.0000	0
2	50Hz	1000	50.0000	-0.1421
3	50Hz	1500	50.0000	0
4	50Hz	2000	50.0000	-0.1421
5	50Hz	2500	50.0000	0.5684
6	50Hz	3000	50.0000	-0.8527
7	50Hz	3500	50.0000	-0.1421
8	50Hz	4000	50.0000	0.2842
9	50Hz	4500	50.0000	-0.1421
10	50Hz	5000	50.0000	0.5684

frequency of selected signal.

Percentage Error = 1.0e-13 *
Elapsed time is 14.599329 seconds.



. Compute Error For Various Sampling Frequency Graph.

Step-2 Find out the frequency of selected signal and to compute errors for various number of harmonics.

Enter the value of power frequency=50Hz

Enter the value of Vmax=700

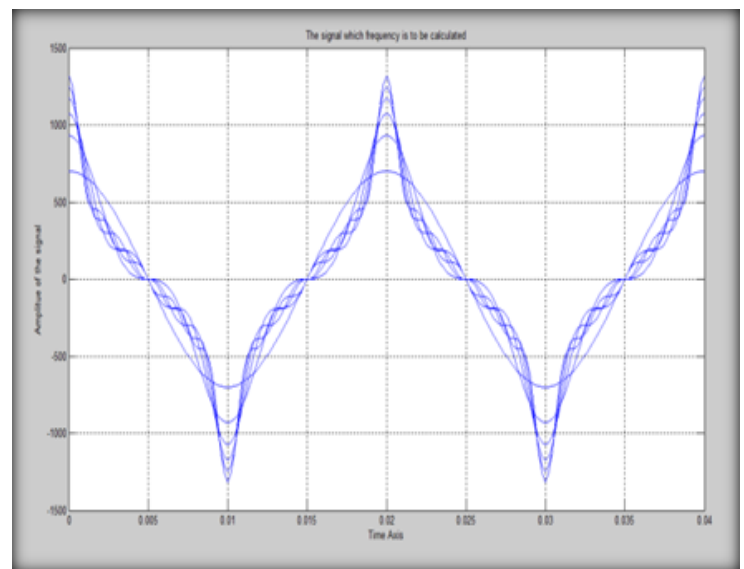
Enter the value of sampling frequency=5000HZ

- When the value of power frequency taken as 50Hz and also consider the sampling frequency (5000Hz)

S .No	Power Frequency	No of Harmonics	Output Frequency	Error
1	50Hz	1	50.0000	0.0000
2	50Hz	2	50.0000	0.0000
3	50Hz	3	49.4903	1.0194
4	50Hz	4	49.4903	1.0194
5	50Hz	5	49.0262	1.9476
6	50Hz	6	49.0262	1.9476
7	50Hz	7	48.5914	2.8172
8	50Hz	8	48.5914	2.8172
9	50Hz	9	48.1784	3.6431
10	50Hz	10	48.1784	3.6431
11	50Hz	11	47.7835	4.4330

in the frequency of selected signal.

Percentage Error = 0.0000
Elapsed time is 8.041241 seconds.



Compute Error For Various Number of Harmonics Graph.

Step-3 Find out the frequency of selected signal and to compute errors for various different power frequency.

Enter the value of sampling frequency = 5000Hz.

Enter the value of Vmax = 700Hz.

Enter the no of harmonics that you want in your signal = 1.

- When the value of sampling frequency (5000Hz) and

S .No.	Power Frequency	Output Frequency	Error
1	100Hz	100Hz	0.5684
2	90Hz	90Hz	0
3	80Hz	80Hz	0
4	70Hz	70Hz	-0.6090
5	60Hz	60Hz	-0.5921
6	50Hz	50Hz	0.5684

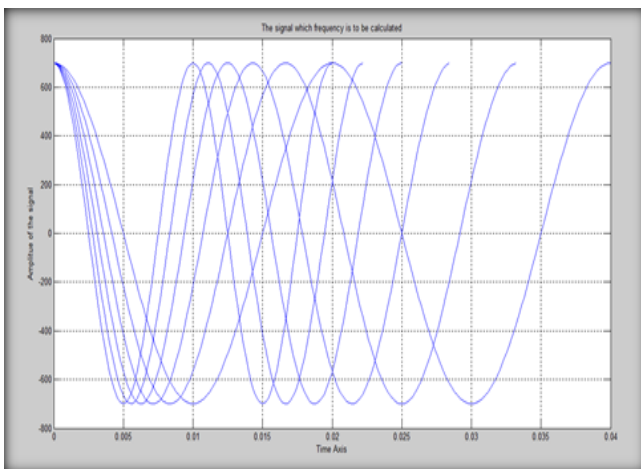
also consider the first harmonics in the frequency of selected signal.

$$\text{Percentage Error} = 1.0e-13 *$$

Elapsed time is 7.500060 seconds.

MATLAB Outputs At Different Power Frequency.

Compute Error For Various Different Power Frequency Graph.



V. CONCLUSION

A method for extending the useful measurement range of the digital signal processing technique for simultaneously

measuring peak values of a voltage or current and its frequency has been presented in this paper. This method is used to designing digital meters and relays that need to measure system parameter accurately over a large frequency range, The technique presented here is general enough to be applied for different relaying purpose such as frequency relay(under frequency, over frequency, over excitation protection).

REFERENCES

- [1] Relay and Telecommunication Div., Westinghouse Electric Corp., "Applied protective relaying," Carol Springs, FL, 1982.
- [2] A. G. Phadke, J. Thorp, and M. Adamiak, "A new measurement technique for tracking voltage phasors, local system frequency and rate of change of frequency," *IEEE Trans. Power Appar. Syst.*, vol. 102, no. 5, pp. 1025-1038, 1983. SIDHU: ACCURATE MEASUREMENT OF POWER SYSTEM FREQUENCY 81.
- [3] M. S. Sachdev and M. M. Giray, "A least square technique for determining power system frequency," *IEEE Trans. Power Appar. Syst.* vol. PAS-104, no. 2, pp. 437-443, 1985.
- [4] A. A. Girgis and T. L. D. Hwang, "Optimal estimation of voltage phasors and frequency deviation using linear and nonlinear Kalman filtering," *IEEE Trans. Power Appar. Syst.*, vol. PAS-103, no. 10, pp. 2943-2949, 1984.
- [4] A. A. Girgis and T. L. D. Hwang, "Optimal estimation of voltage Phasors and frequency deviation using linear and nonlinear Kalman filtering," *IEEE Trans. Power Appar. Syst.*, vol. PAS-103, no. 10, pp. 2943-2949, 1984.
- [5] H. Tao and I. F. Morrison, "The measurement of power system frequency using a microprocessor," *Elect. Power Syst. Res.*, vol. 11, pp.103-108, 1986.
- [6] S. A. Soliman, "An algorithm for frequency relaying based on least absolute value approximations," *Elect. Power Syst. Res.*, vol. 19, pp.73-84, 1990.
- [7] V. V. Terzija, M. B. Djuric, and B. D. Kovacevic, "Voltage phasor and local system frequency estimation using Newton-type algorithms," *IEEE Trans. Power Delivery*, vol. 9, no. 3, pp. 1368-1374, 1994.
- [8] T. S. Sidhu, M. S. Sachdev, and R. Das, "Modern relays: Research and teaching using PC's," *IEEE Comput. Applicat. Power*, vol. 10, pp.50-55, Apr. 1997.
- [9] A. Y. Zayezdny and I. Druckman, "Short time measurement of frequency and amplitude in the presence of noise," *IEEE Trans. Instrum. Meas.*, vol. 41, pp. 397-402, June 1992.
- [10] M. K. Mahmood, J. E. Allos, and M. A. Abdul-Karim, "Microprocessor implementation of a fast and simultaneous amplitude and frequency detector for sinusoidal signals," *IEEE Trans. Instrum. Meas.*, vol. IM-34, pp. 413-417, 1985.



Vivek Bargate, received B.E. (Electrical & Electronics & Engineering) in year 2008 and in pursuit for M.Tech. (Instrumentation & Control) from Bhilai Institute of Technology (BIT), Durg, Chhattisgarh, India. His interest is in Digital Signal Processing and control system design. Also he is having Life Membership of Indian Society of Technical Education, India (ISTE).



Sr. Associate Professor Mr. R. M. Potdar, received B.E. Electronics, M.Tech.(Hons) Instrumentation & Control. He is having a total teaching experiences of 15 years and industrial experiences of 5 years. His interests are in Image Processing, Neural Network & Fuzzy Logic System Design. His specialization subjects are Adaptive Control System, Optimal Control System, Control System Design, Satellite communication and Optical Communication. He has published the papers in 8 international journals and 4 national journals and also attended 2 international conference and 14 national conferences. Also he is having Life Membership of Indian Society of Technical Education, India (ISTE).