International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 3, Issue 10, October 2014

Low Latency CORDIC Architecture in FFT

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***Abstract*— CORDIC means coordinate rotation digital computer, a proposed scheme for the calculation of cosine and sine function of fixed angle. Low latency Bi-rotation CORDIC scheme is proposed here for the rotation of vector at fixed angle. Latency of computing the cosine and sine value of an angle is minimized by the influence of high speed adder design .This scheme applied for FFT processors in OFDM system for the calculation of twiddle factor.**

***Index Terms*—CORDIC, Elementary Angle Set, FFT, Scale factor, Sign Bit Register, Twiddle factor.**

I. INTRODUCTION

CORDIC, a scheme which is preferred for the rotation of vector at known and fixed angle. The CORDIC algorithm was first developed by Jack.E.Volder for the computation of trigonometric functions. CORDIC algorithm can also be applied for the multiplication, division and conversion operation .They found application in DSP, graphics and image processing. Out of many existed schemes improved high speed Bi-rotation CORDIC is preferred scheme which provide the rotation of vector at fixed angle in a limited number of micro rotation step by performing pair of micro rotation at the same time. Algebraic addition is the main operation for the CORDIC algorithm, the efficiency of the hardware implementation of the algorithm depends significantly on the type of adder/sub tractor used. Digital signal processing (DSP) is used in almost all the modern digital sound hearing application. The processing of the sound signals is carried out in the frequency domain. Fast Fourier Transform (FFT) converts the time domain signal to frequency domain and gives a complex number output representing each frequency component in the audible frequency (AF) spectrum.

The magnitude estimation block will estimate the magnitude of the complex numbers. This estimated magnitude is used as an input to apply various DSP algorithms for sound processing in the hearing aid. Hearing aid is a device that helps in making the normally inaudible sounds to be audible for hearing impaired people and thus enables them to maintain contact with the aura1 world. The study shows that around 10% of people in the developed countries suffer from hearing impairment. This magnitude estimation can be done by the trigonometric algorithm. The advantage of frequency domain leading to the need of FFT operation in OFDM system. The twiddle factor calculation, a major issue in FFT processor now resolved by preferring low latency Bi-rotation CORDIC design.

II. RELATED WORKS

The CORDIC computing technique was developed especially for use in real-time digital computer where the majority of the computation involved the discontinuous and programmed solution of the trigonometric relationships of navigation equations and a high solution rate for the trigonometric relationships of coordinate transformations. Conventional scheme [4], CORDIC scheme which require large number of iteration corresponding to the precision of output. Angle Recoding (AR) [2][3][5][10] is the one which reduce the iteration count to half of that of conventional scheme without altering the accuracy. The elementary angle set (EAS) based angle recoding scheme [6] where angle to rotate represent to an elementary angle set. It is the scheme providing better recoding efficiency. Parallel angle recoding [7] [8][10] achieves the same aim when all prior angles are known. High radix (radix-4) CORDIC [8] algorithm an existing scheme computes the results at less latency than radix-2 AR schemes. Cascaded pipelined schemes like cascade single rotation and cascade bi-rotation CORDIC, the micro rotation corresponding to each iteration is implemented stage by stage. Cascade bi-rotation is providing more throughput than single rotation. The barrel shifter, one of the hardware component for the shift operation to implement CORDIC equation whose complexity is effectively high .The complexity reduction get possible by the CORDIC pre shifted scheme. Scaling an important phenomenon to make the rotated vector with exact magnitude. The inclusion of scale factor and its multiplication with coordinates of vector leading to complex multiplication. Such complex operation leads to too much of latency. The scaling free CORDIC [13], proposed scheme which will bring the effect of scaling without multiplication. Here the single circuit is served for both scaling and micro rotation separately.

III. CORDIC OVERVIEW

The CORDIC which is used to rotate a vector in a known angle. Basically considering elementary rotation process, the given angle to rotate is achieved by performing micro rotation step. In each micro rotation step it rotates the vector to a micro rotation angle, and then it is compared with exact angle Φ. If the angles are not matched, CORDIC provide next micro rotation process to approach to exact angle. Considering two

ISSN: 2278 – 909X

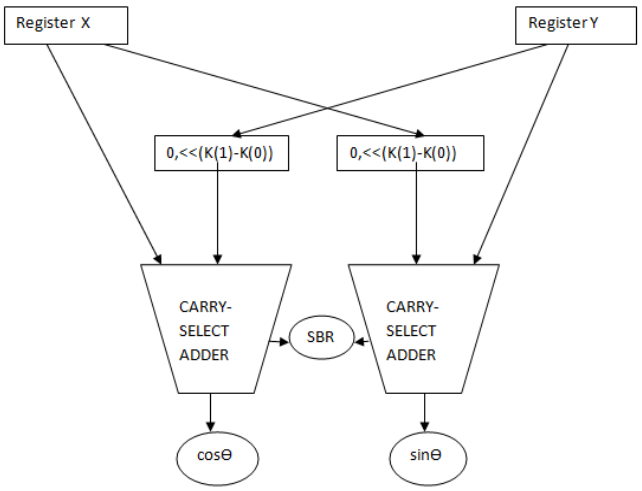

Fig1-Low Latency Bi-Rotation CORDIC

dimensions we are considering x coordinate and y coordinate of a vector. The CORDIC Algorithms can provide the Calculation of vector rotation and inverse tangent. The algorithm, credited to Volder is derived from the general Rotation transform as given below: Here X1and Y1 considered being coordinates of rotated vector at angle Φ. Then

$X1 = x \cos\Phi - y \sin\Phi$
$Y1 = y \cos\Phi + x \sin\Phi$
It rotates a vector in a Cartesian plane by the angle Φ. These can be arranged so that:

$X1 = \cos\Phi [x - y \tan\Phi]$
$Y1 = \cos\Phi [y + x \tan\Phi]$
The CORDIC Iteration equations implemented in hardware are:

$X_{i+1} = Xi - \sigma_i Y_i 2^{-i}$
$Y_{i+1} = X_i \sigma_i 2^{-i} + Y_i$
$Z_{i+1} = Z_i - \tan^{-1}(\sigma_i 2^{-i})$
Where $\sigma_i \epsilon \{-1, 0, 1\}$ which is the sign bit register content stored inside the ROM and it will tell the direction of rotated vector either clockwise or anticlockwise.
$\Theta = \Sigma \sigma_i \alpha_i$
Where $\alpha_i = \tan^{-1}(\sigma_i 2^{-i})$ is an elementary rotation angle covered during the iteration 'i'.
To implement the CORDIC equation, hard warily we need pair of registers to store coordinates, pair of barrel shifter to perform shift operation, pair of adder/sub tractor to perform addition and sub traction and sign bit registers to store the σ_i values.

A. Low latency bi-rotation scheme

Bi-rotation scheme [1], one of pipelined scheme can be implanted in both cascade and feedback mechanism. But cascade is more preferred than feedback mechanism as we are concentrating on low latency criteria. Comparing to single rotation CORDIC.
The scheme, bi-rotation offers more throughput because of implementing a pair of micro rotation at each stage instead of performing single rotation. Here there is no reduction of hardware component in each stage for the basic bi-rotation CORDIC comparing to single rotation. But a low latency bi-rotation CORDIC means that no of stages required to cover the exact angle is now reduced to half of that of cascade single rotation CORDIC. Comparing to existing basic bi-rotation CORDIC it is high speed bi-rotation CORDIC proposed here which will perform addition and sub traction in a faster Mode. Low Latency Bi-Rotation CORDIC as shown in Fig 1. k(i) represent no of shift performed by barrel shifter corresponding to i^{th} iteration. So k(0) shift at iteration=0 is performed by truncating k(0) LSBs of coordinate data to zeros. So it has to make shifter to perform zero shift at iteration =0.while on second iteration it has to perform k(1)-k(0) shift.

To achieve this aim, the adder design is changed here. Looking to the implementation side +/- indicates normal addition/sub traction which will performed by inbuilt adders. The proposed design influence the use of high speed adder like carry select adder for the implementation of CORDIC equations as shown in Fig1. Similar to basic CORDIC carry select adder has two inputs, one is direct input from a register and other is shifted version of another input.

IV. APPLICATION OF CORDIC IN FFT PROCESSORS

A modern signal processing application requires a high computational power for technical demands which we could be fulfilled only by ASIC. Though it meets all the technical demands ASCIC has disadvantage like inflexibility, high cost and economical for only mass products. So the system designers are striving to replace the hardware based solution with a software based solution. DSP, one of the most commonly used programmable devices has the lack of power requirement needed for the design. In order to provide the solution between these two extremes such as programmable signal processing and dedicated hardware a reconfigurable computing technique is developed. Here this paper replaces the MAC based FFT to a purely CORDIC based FFT [9][11]. The Coordinate Rotation Digital Computer (CORDIC) was introduced by Volder that provides an effective method for computing iteratively the rotation of the two dimensional vector using only shift and adds operation.
The CORDIC algorithm is used in many applications such as digital filtering, modulation, Fast Fourier Transform (FFT) [12], and Signal Value Decomposition (SVD) [14]. Here out of many CORDIC designs which can be applied to FFT processor, the proposed low latency bi-rotation CORDIC is one which compute twiddle factor at highest speed rate.
The CORDIC based architecture is a very appealing alternative to multiply and add hardware.
A 2 point FFT i.e. N=2 is shown in Fig 2.
$W_N^k = e^{-j 2\Pi k/N}$, is the Twiddle factor.
Here A and B are the complex input & is fed to the adder and sub tractor. The sub tractor output will be multiplied with twiddle factor W_N^k. For an 8point FFT butterfly structure it has 3 stages. The value of k is different in each stage.

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K=0, 1, 2, 3 for first stage of FFT
K=0 and 2 for second stage of FFT

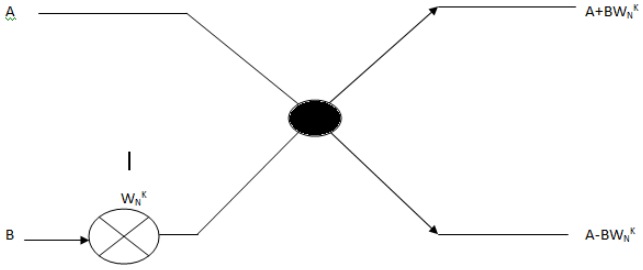

Fig 2 Two point FFT structure

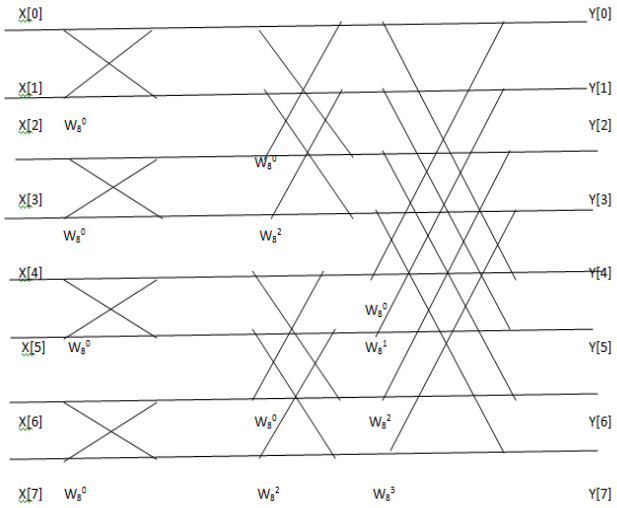

Fig 3 Butterfly Structure (8 Point FFT)

K=0 for third stage of FFT

The 'Radix 2' algorithms are useful if *N* is a regular power of 2 (*N*=2*p*). The FFT are the most advanced one because there are several numbers of FFT algorithms used.
There are two Radix 2 algorithms, called 'Decimation in Frequency' (DIF) and 'Decimation in Time' (DIT) algorithms. Both the algorithms depend on the recursive decomposition of an *N* point transform into 2 (*N*/2) point transforms. The decomposed process can be applied to any composite (non prime) *N*. The method is simple if *N* is divisible by 2 and if it is a power of 2, then the decomposition can be done recursively until the trivial '1 point' transform is reached.

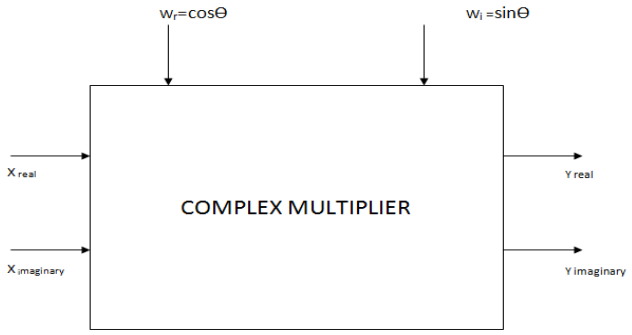

Fig 4 Complex multiplier of FFT

Consider X and Y as input and output which are complex in nature. Wr and Wi are results of CORDIC section, then the complex multiplication is as follows.

(X r+ j X i)*(Wr- j W i) =
((Xr * Wr) - (Xi * Wi)) + j ((Xr * Wi + Xi * Wr))

V. RESULT ANALYSIS

TABLE 1
Parameter List for CORDIC Schemes

parameters	Bi-rotation CORDIC	Low Latency Bi-rotation CORDIC
Latency	35ns	20ns
Number of ROM	1	0
Memory Usage	207464 kilobytes	214248 kilobytes

Latency, a major issue of CORDIC listed for both Bi-rotation CORDIC and low latency Bi-rotation CORDIC. Here in the case of simple bi-rotation CORDIC adder is nothing but similar to ripple carry adder. As far as improved bi-rotation CORDIC is concerned, it has carry select adder compute the addition in a faster manner. For the FFT processor application most probably an adder of 40bit operand when concerned Bi- rotation CORDIC calculate twiddle factor at 35 nanosecond (ns) where as improved bi-rotation CORDIC at 25 ns. Looking the complexity of the schemes, Bi-rotation CORDIC are less complex than improved Bi-rotation scheme.

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A. Simulation Result

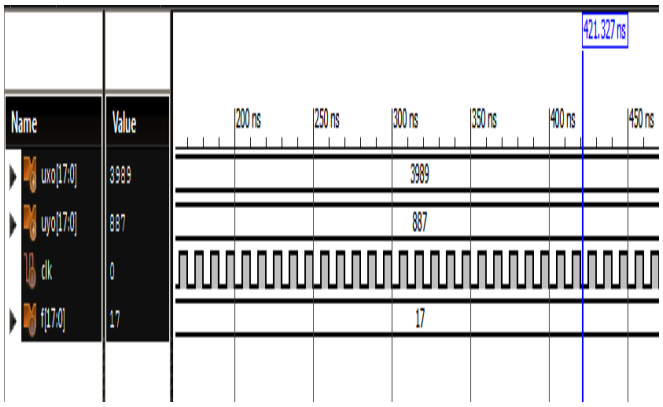

Fig 5 Simulation Result of Bi-Rotation Cascade CORDIC

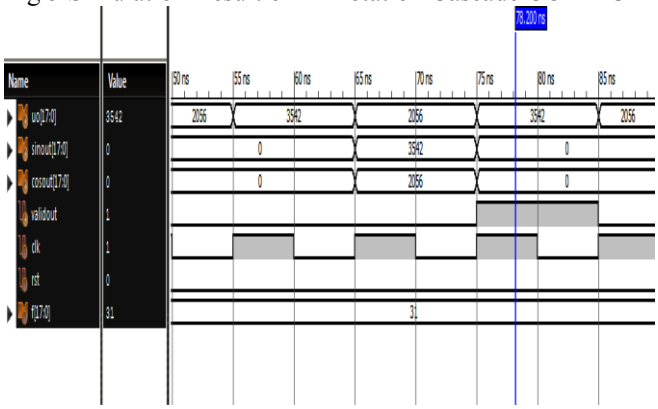

Fig 6 Simulation Result of Low Latency Bi-Rotation Cascade CORDIC

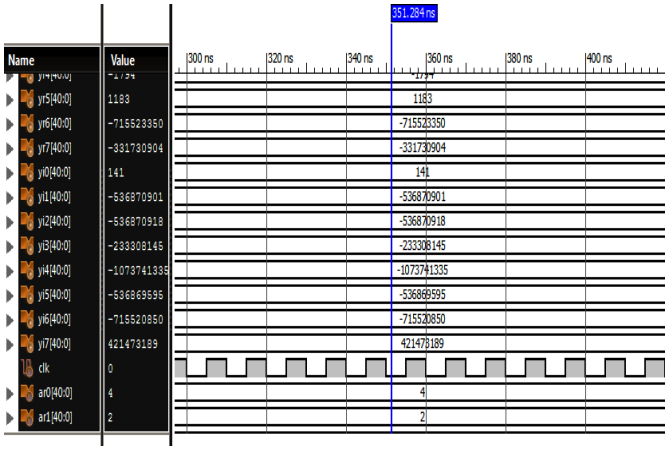

Fig 7 Simulation Result of CORDIC based FFT Processor

VI. EXPERIMENTAL SETUP

The proposed system is to be implemented in three parts. The first part is to accomplish the CORDIC architecture for the Bi -rotation schemes, the second part is devoted to develop the high speed VLSI architecture for CORDIC among the existing scheme, and the third part is the application of this high speed version in FFT. The software part in Verilog HDL language is verified using a-simulation behavior model in Xilinx. After the successful simulation and verification, these programs are loaded into Xilinx ISE Spartan 3E FPGA target device for synthesis.

VII. CONCLUSION

A high speed CORDIC scheme is proposed where high speed adders are preferred for addition /sub traction. For the FFT processors in OFDM system, such a CORDIC design is put forward for the twiddle factor calculation which provide entire output of FFT at less time.

ACKNOWLEDGMENT

I would like to acknowledge the support of the Department of Electronics and Communication Engineering, SNGCE for Technical facilities. I am also grateful to my beloved guide, Ms. Meera Thampy. (Assistant Prof., SNGCE), for her Valuable guidance, contributions and encouragement which make this work successful. Last but not the least; I humbly extend my gratitude to other faculty, my friends and family especially Mr. Rajiv and Ms Sujitha for their unending support.

Above all, I thank God Almighty for giving me strength, courage and blessings to complete this work.

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ISSN: 2278 – 909X

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ISSN: 2278 – 909X