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Implementation and performance evaluation of different multipliers

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***Abstract*— In digital signal processing applications, multiplication having the repetitive shift and add operation is the slowest in operation and dominates most of the execution time. There is a need of high speed multipliers. In order to increase the performance of multipliers, reduced number of half adders can decrease the delay and area also will be reduced. This thesis is the detailed study of different multipliers based on array multiplier, constant coefficient multiplication (kcm), vedic urdhva multiplier, wallace multiplier, proposed wallace tree multiplier and vedic nikhilam sutra multiplier. All these multipliers are coded in verilog hdl (hardware description language) and simulated in modelsimxeiii6.4b and synthesized in xilinx_ise9.1. The multipliers are compared based on luts (look up table) and path delays. Results show that improved wallace tree multiplier is the fastest multiplier with least delay.**

I. INTRODUCTION

Multiplication dominates the execution time of most digital signal processing algorithm. There is a need of high speed multiplier. Higher throughput arithmetic operations are important to produce high performance applications. Reducing the time delay and power consumption are essential requirements. Multiplier delay depends on the critical path delay and ultimately defines the performance of multiplier. Speed is the main factor in multipliers. In the proposed multiplier there is a improvement in the speed by reducing the number of half adders which also reduces delay and number of look up tables.

Different types of multipliers are discussed below:

I. Array multiplier

An array multiplier is a digital combinational circuit which is interesting design because that uses a large array of adders or an alternative that cycles a smaller array of adders used several times to compute the product. Logical effort is used to seek a design with minimum delay.

In this array multiplier all the partial product rows are formed and then uses carry save adder for adding the two binary numbers by using of full adders and half adders.

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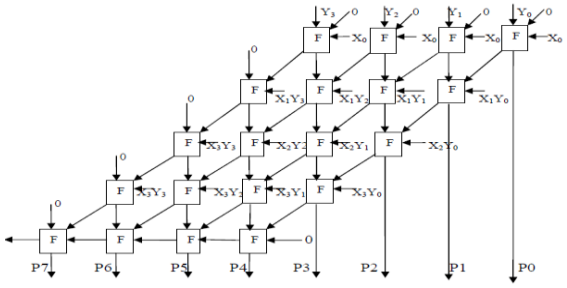


Structure of array multiplication

II. KCM

Constant coefficient multiplication is also known kcm. This kcm is rom based approach. In conventional kcm, one input is fixed but here both inputs for the multipliers are variables. In this method, a rom is used for storing of numbers. Constant coefficient multiplication is frequently referred to as multiplication by compile-time constants. These constant coefficients can be used explicitly or implicitly used in a program run on a general-purpose processor.

To find the multiplication of A and B, First need to find the difference of two numbers and then the output depends on the whether the result is even or odd.

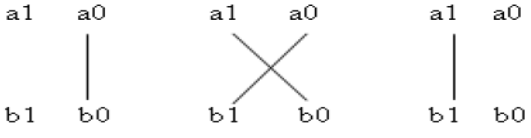
EVEN DIFFERENCE:
Result of the multiplication = [average] ^2 – [deviation] ^2
ODD DIFFERENCE:
Result of the multiplication = [average*(average+1] – [deviation*(deviation+1)]

Where
Average=[(A+B)/2]
Deviation= [Average-Smallest (a, b)]

III. VEDIC URDHAVA TIRYABHYAM MULTIPLIER

Vedic mathematics is a gift to this world by the ancient sages of India. The word Vedic is derived from word Veda which means that store-house of all knowledge.

Vedic urdhava multiplier is nothing but vertical and crosswise multiplier. This multiplication is applicable in all types of multiplications. In this multiplier the generation of partial products can be done with the concurrent addition. The partial product generation and the summation can be done by using the parallelism



Structure of urdhava multiplication

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IV.NIKHILAM SUTRA MULTIPLIER

Nikhilam sutra means "All from 9 and last from 10". It is also applicable to all cases of multiplication. It is more efficient in numbers involved are large. Larger the number, complexity of the multiplication will be reduced. This Nikhilam sutra which is used for large numbers and having the same nearest base. This Nikhilam sutra which is occupying less area and less delay compared to other multipliers.

87*97
Nearest base=100
87 (100-87)
97 (100-97)
Column1 Column2
87 13
97 3
84 39
Result = 84*100+39=8439

Structure of nikhilam multiplier

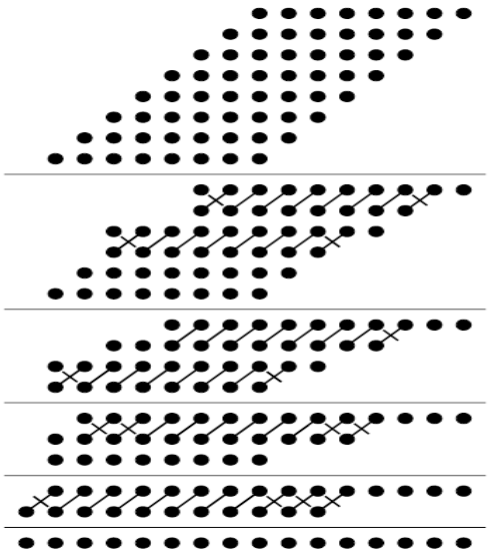
V.WALLACE TREE MULTIPLIER

Wallace tree multiplier is a parallel multiplier which is hardware efficient implementation of a digital circuit. In this Wallace tree multiplier partial products are reduced as soon as possible. Repeat the process until the largest stages are reduced to the height.
Wallace tree multiplier will be having three stages:

a) Generation of the partial products of multiplier is formed.
b) Reducing the partial products rows to the height of two rows.
c) Finally the reduction two rows is passed to a carry propagate adder to get the final result.

Next the partial products are formed by N rows these are grouped together in sets of three rows. Any additional rows that are not a member of a group of three rows then those rows are transferred to next layer without doing any modification.
With each group of three rows each. Then

a. Take any three wires with the same weights and input them into a full adder.
b. If there are two wires of the same weight left, input them into a half adder.
c. If there is just one wire left, connect it to the next layer



Structure of Wallace tree multiplier

In Wallace tree multiplier of 8-bit then four reduction stages are required with matrix height of 6, 4, 3, 2. This requires 64 AND gates, 38 FULL ADDERS, 15 HALF ADDER and 10 bit carry propagating adder are required to form the 16-bit product.

VI .PROPOSED WALLACE TREE MULTIPLIER

In proposed Wallace tree multiplier, usage of half adders is reduced as it does not reduce the partial product reduction. So by reducing the usage of half adder in Wallace tree multiplier the area will be reduced and then speed will be increased compared to that of conventional Wallace tree multiplier.
Proposed Wallace tree multiplier will be having three stages:

a) Generation of the partial products of multiplier is formed.
b) Reducing the partial products rows to the height of two rows.
c) Finally the reduction two rows is passed to a carry select adder to get the final result.

If the multiplier is having n-bit then partial products of the multiplier is formed by using N2 and gates. Next the partial products are formed by N rows these are grouped together in sets of three rows each by using the recursive algorithm. Any additional rows that are not a member of a group of three rows then those rows are transferred to next layer without doing any modification.
With each group of three rows each. Then

a) Use full adders for each 3-bit group in a column.
b) A group of 2-bit in a group is not process it is passed to next layer as passed in like single bit is passed to next layer.
c) The only time half adder is used is to ensure that the number of stages does not exceed that of a conventional Wallace.

When the multiplication which reduces the height of two then it is passing to a carry select adder to perform the final addition because its speed is more as compared to carry propagate adder. In Wallace tree multiplier of 8-bit then four reduction stages are required with matrix height of 6, 4, 3, and 2. This requires 64 AND gates, 40 FULL ADDERS, 3 HALF ADDER and 10 bit carry select adder are required to form the 16-bit product.

MULTIPLIER	DELAY(ns)	4 I/p LUTS
CONVENTIONAL WALLACE	18.647	131
PROPOSED WALLACE	17.972	122

SIMULATION RESULTS

The simulation results of different types of multipliers like Wallace tree multiplier and proposed Wallace tree multiplier and Nikhilam Vedic multiplier along with base paper multipliers.

Parameter	Luts	Delay
Array Multiplier	146	18.792
Kcm	79	22.864
Vedic Urdhava Multiplier	136	19.995
Wallace Tree Multiplier	135	18.314
Nikhilam Vedic Multiplier	140	28.481
Proposed Wallace Tree Multiplier	122	17.972

Simulation results of different multipliers

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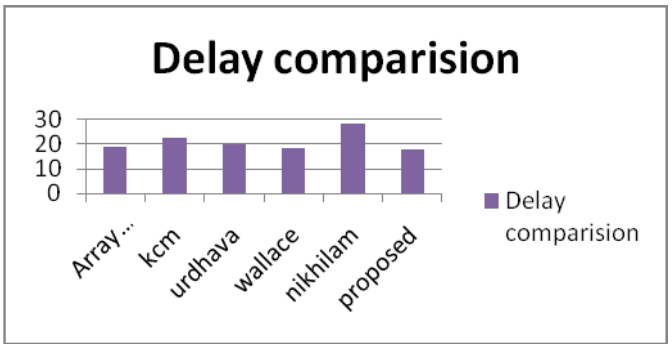
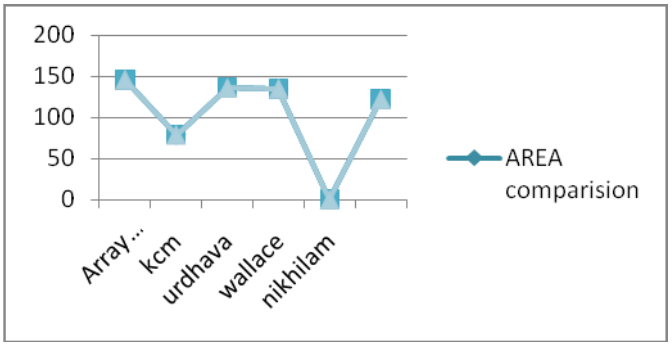
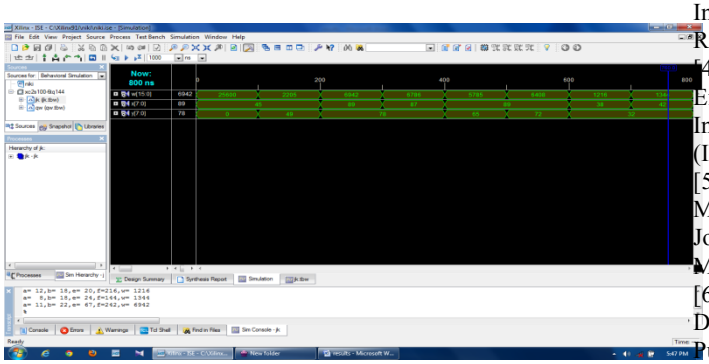


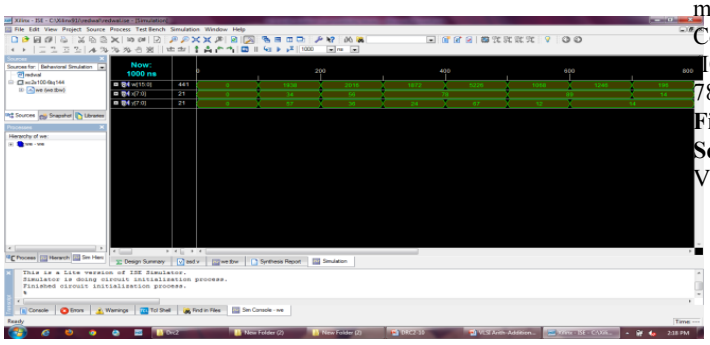
Delay comparison chart



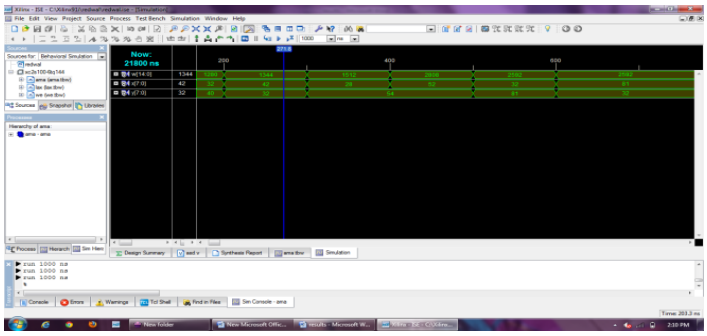
LUT comparison charts



Simulation results of nikhilam Vedic multiplier



Simulation result of Wallace tree multiplier



Simulation results of proposed Wallace tree multiplier

CONCLUSION:

The computational path delay for proposed 8x8 bit Wallace tree multiplier is found to be **17.972ns** as shown in Table 2 which is the least time delay of all the multipliers**.** Hence the motivation to reduce delay is finely fulfilled. Therefore, the proposed Wallace tree multiplier is much more efficient than Array, Constant Coefficient Multiplier (KCM), Urdhva Tiryakbhyam, Wallace tree multipliers, Nikhilam Vedic multiplier in terms of execution time (speed).

FUTURE SCOPE:

Modified carry select adder configurations can be attempted to increase speed for higher number of bit inputs than 8 or 16 bits. Adoptive methods or interactive multiple algorithmic models can result in performance up gradation.

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