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FPGA Realazation of Multi Channel Data Acquisition System with Nand Storage

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Abstract

Data Acquisition System (DAS) is widely used in different fields of Engineering. Mainly this paper describes design and development of multi channel FPGA based Data Acquisition System with NAND storage. This system acquires data with different frequencies (different sampling rates), the required pre-conditioning circuits already incorporated in the hardware. This is to implement ADC controller module on FPGA.ADC controller is on FPGA module, which receives data parallel and transfers this data to ADC through SPI protocol. It also generates required clock signals for SPI communications and ADC operation. At final, a RS232 based debug module is implemented on FPGA to debug application software and uploading data from NAND flash. Required and relevant hardware have been realized using Spartan-3 FPGA device.

Index terms –FPGA – Field Programmable Gate Array , ADC – Analog to Digital Converter .

I. INTRODUCTION

All engineering activities require collection of data, in development, production, quality control, management, process control etc.This has been using thermometer, voltmeters, scales, oscilloscopes and such variety of measuring devices and instruments to read the physical data.The emphasis is therefore on getting the machines to meet most of our data acquisition and control needs. Data acquisition and conversion systems are used to acquire analog signals from one or more sources and convert these signals into digital form for analysis or transmission by end devices such as digital computers, recorders, or communications networks. The analog signal inputs to data acquisition systems are most often generated from sensors and transducers which convert real-world parameters such as pressure, temperature, stress or strain, flow, etc., into equivalent electrical signals. The electrically equivalent signals are then converted by the data acquisition system and are then utilized by the end devices in digital form.

Data acquisition products serve as a focal point in a system, tying together a wide variety of products, such as sensors that indicate different parameters. This system acquires data with different frequencies (different sampling rates), the required pre-conditioning circuits already incorporated in the hardware.

II. DEVELOPMENT SPECIFICATIONS

Specification	Tool
Software	Xilinx13.2
Hardware	Spartan 3E
Language	Verilog HDL

III. DESIGN ARCHITECTURE

Figure.1 shows the block diagram of the data acquisition system FPGA as a main processing element. The system is designed to acquire the six channels data from pre-amplifier outputs, a dedicated ADC converter used for each individual channel[2].

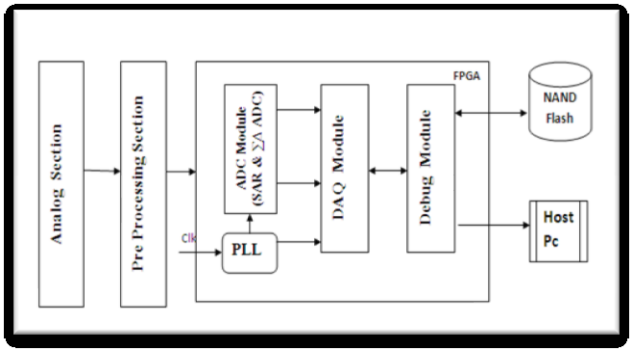

Fig.1Block diagram of multichannel DAS

The sensor outputs fed to pre-amplifier circuit for preconditioning and followed a low pass anti aliasing filters. A over sampling ADC (sigma-delta) using to reduce the anti-aliasing filter order. Due to FIR filter in ADC architecture multiplexing the ADC is not possible. An individual ADC placed for each channel. All ADC interfacing with FPGA, an ADC control module implemented for each individual ADC. This module

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generates all control and interfacing signals required for ADC and reads the sampled outputs[4]. A PLL used to generate different clocks for each module. This PLL takes FPGA input clock and generates clocks for ADC and SPI communication.

A. PLL Clocking

PLL is used to synthesize new frequencies which are a multiple of a reference frequency, with the same stability as the reference frequency[2]. PLL IP cores are used for generating clock signals.It takes the FPGA input clock as the reference frequency and generates required frequencies for each module.Table 2 represents the frequency ranges used for PLL Clocking. With reference to reset pin ,which is an active low signal, PLL locks the required range and gives the resultant frequency.Fig 2 shows the simulation result for PLL Clocking.

Table 1.PLL Frequency Ranges

Instantiation	Input frequency	output frequency
PLL1	10MHz	75MHz
PLL2	10MHz	80MHz
PLL3	8MHz	5.12MHz

B. SPI Communication

SPI is a synchronous serial data link that operates in full duplex[3].TLC2578 is a 8-channel, 12-bit SAR ADC Operated in Hardware Default Mode (SPI) Bipolar Offser Binary Output Code, Normal Long sampling (44 SCLKs), Internal OSC, single-ended input, one-shot conversion mode (mode=00)[6].Each operation cycle performs one sampling and one conversion for the selected channel. The TLC2578 (MUX) ADC requires a falling clock edge while the chip select pin is in the high state in order to release the output data.

C. ADC Interfacing

A 75MHz serial clock is used to initiate 16bit ADC in CMR state of SPI Communication. The ADS1606 and AD7785 is high-speed, high-precision, delta-sigma analog-to-digital converters (ADCs) with 16-bit and 24 bit resolution respectively[3]. The 16bit data is in binary two's complement format. When the input is positive out of range exceeding the positive full scale value of +1.467 Vref the output clips to 7FFFh and drdy goes low. Likewise, when the input is negative out-of-range by going below the negative full-scale value of –1.467VREF, the output clips to 8000h and the drdy goes low. The drdy remains low while the input signal is out-of-range[6]. The AD7765 uses an SPI-compatible serial interface.The data read from the AD7765 is clocked out using the serial clock. If the FSI line is low, then the first data bit on the serial data in (SDI) line is latched in on the next SCLK falling edge[6].To complete the SPI Communication a parallel DAC is interfaced with these ADCs. Fig 6 & 7 shows the simulation results for ADS1606 and AD7785. This DAC module converts these digitized samples into pure form (analog data). After this the results are displayed and stored in NAND flash[5].

D. NAND flash

NAND Flash uses electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. This provides a memory device with a low pin count. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations[5]. The addresses are latched by an address register and sent to a row decoder or a column decoder to select a row address or a column address, respectively.

IV. SIMULATION RESULTS

Xilinx released software to easily modify extra peripherals like UARTS, SPI controllers or other IP cores can be easily configured. It also offers the capability of generating an FPGA design. Xilinx Platform studio and a set of IP cores that are required for developing required systems[6]. The following figures shows the simulation results of individual modules.

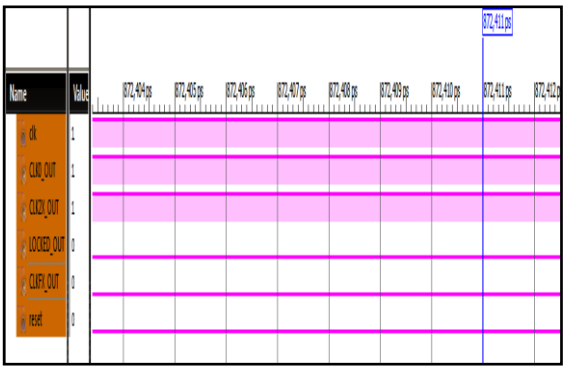

Fig 2. Simulation of PLL Clocking

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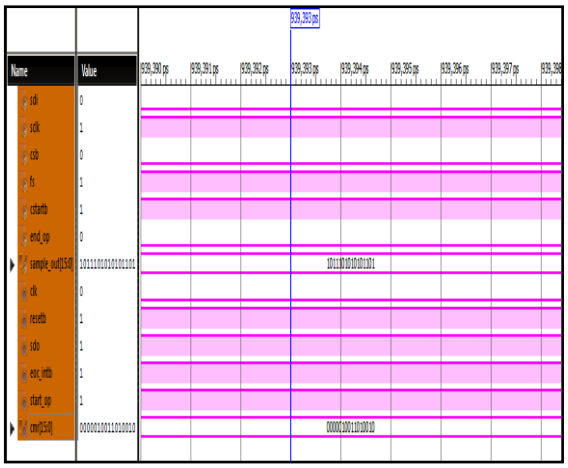

Fig 5. Simulation of TLC2578 ADC

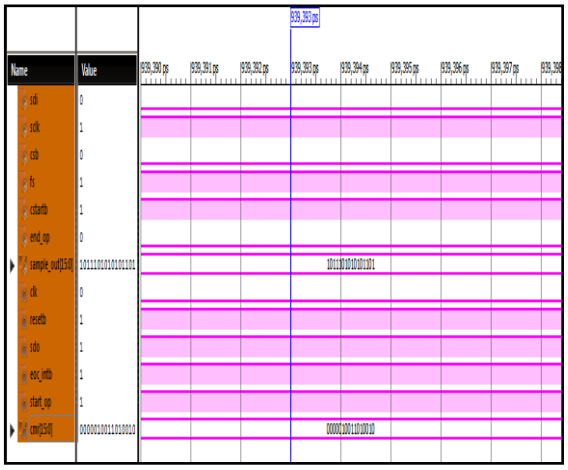

Fig 6 .Simulation of ADS1606

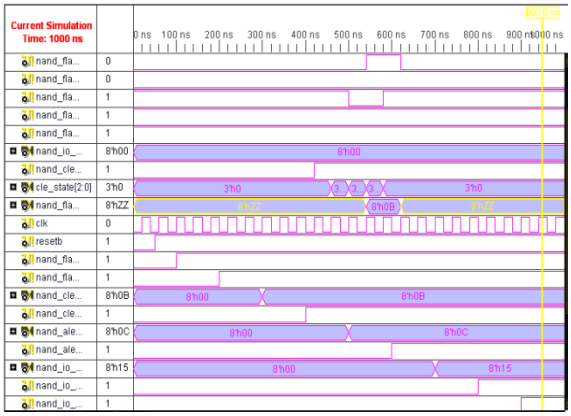

Fig 7 .Simulation of NAND

V. CONCLUSION

Multichannel data acquisition systems that are designed and constructed in-house have several advantages over turnkey commercial systems, including the potential for considerable cost savings, flexibility in acquiring data, and the ability to subsequently add additional components. The programmable input output lines made it to interface with many of the real-time applications with the only cost of voltage translators or level shifters. The programmable input output lines of FPGA can be used to interface more number of digital devices and the slots can also be expanded in order to increase further more number of digital devices attached. Where for the other type of processors offers limited connectivity.

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