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FPGA IMPLEMENTATION OF PARITY BIT BASED TCAM

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***Abstract*—This paper involves the design and implementation of a parity bit based TCAM on FPGA using VHDL.CAM is a special type of memory used in certain high speed search applications. TCAMs are the memories that searches the data on the basis of contents stored them. If a match is found it returns the address of the data, unlike RAM in which data is returned for a given address. TCAM compares input data against the stored data in parallel and outputs the address of matched data.**

This model actually represents the textual description of a hardware design or a piece of design which, when simulated mimics the design behavior.

Keywords-Content Addressable Memory(CAM);Ternary Content Addressable Memory(TCAM);RAM;Xilinx spartan FPGA,HDL;

I. INTRODUCTION

A CAM is a special type of storage memory[1] TCAMs are one level higher than CAM because they can search unknown bits also i.e. ternary states. The main role of ternary content addressable memory (TCAM) is to search input data against the pre-loaded data and output the comparison result which is then used to invoke a related entry from a conventional memory. A TCAM cell has a mask cell, data cell, and masking and comparison circuitry. Mask and data cells are typically implemented with SRAM. TCAM is an outgrowth of RAM, which became popular in the literature for its high speed search operation.

The major application of TCAM is in IPv6[2].Other applications are in network routers, cache memory, ATM switches,Translation look-asideBuffers(TLB) in microprocessors[3].

The parity bit based TCAM design consists of the original data segment and an extra one-bit segment, derived from the actual data bits. We only obtain the parity bit, i.e., odd or even number of "1"s.The obtained parity bit is placed directly to the corresponding word.

II. BASIC STRUCTURE OF CAM

Fig.1.Shows basic architecture of CAM. The input to the structure is through search lines and the input is a search word. The size of the input word can be varied depends on the FPGA`s size capacity. Here we are using 8-bit input search words. Each stored word has a match line and this match line indicates the absence or presence of the search word inside the stored data. An encoder is used at the output of the CAM architecture to choose the output if multiple matches are detected. The encoder selects the output with the priority level.

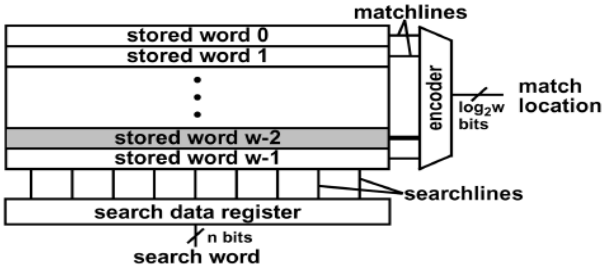

Figure1. Basic structure of CAM

III. HYBRID PARTITIONING OF TCAM

While designing a new architecture our prime aim is to create it efficiently and provide maximum performance. The primary step for improvising the performance of TCAM is the hybrid partitioning[5]. Hybrid partitioning logically dissects the TCAM table horizontally and vertically into m x n number of sub-tables. All TCAM sub-tables are then processed to be stored in their corresponding SRAM memory units.

A conceptual view of hybrid partitioning is shown in the fig.2.Vertical partitioning part of hybrid partitioning implies that a TCAM word of width "W" bits are divided into "n" sub-words, each of which is of width "w" bits. Horizontal partitioning part of hybrid partitioning divides each vertical partition using the original address range of conventional TCAM table. Hence, the dimension of each hybrid partition is "K w" where "K" represents a sub-set of original address pool and "w" is the number of bits in a sub-word. All TCAM tables have the same dimensions. Hybrid partitions/TCAM sub-tables spanning the same address range are considered to be in the same layer. For example,HP_{11},HP_{12},HP_{13},...HP_{1n} span the same address range and are in the same layer. It should be noted that number of layers are equal to number of horizontal partitions. As there are "m" horizontal partitions, thus there are "m" layers.

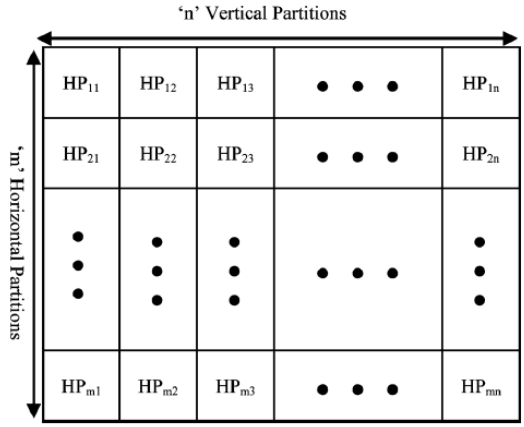

Figure 2. Hybrid partitioning

IV. Memory Architecture Of Hp-Sram Based Tcam

Architecture of HP SRAM-based TCAM is depicted in Fig. 3 where each layer corresponds to Fig. 4. The output of each layer is a Potential Matching Address (PMA). In case of multiple PMAs (multiple matches), Global Priority Encoder (GPE) selects the highest priority PMA as a Matching Address (MA). PMA of a lower layer has the highest priority. For example, if we have PMAs 1, 5, 9 corresponding to layers 1, 5, and 9 respectively, then GPE will select 1 as MA because it has the highest priority.

Architecture of a layer of the proposed TCAM is shown in Fig. 4. Main components in a layer of the target memory architecture include 'n' Bit Position Tables (BPTs), "n" Address Position Tables (APTs), "n" Address Position Table Address Generators (APTAGs), Local Priority Encoder (LPE), and ANDing operation. BPTs and APTs are constructed from SRAM. Each hybrid partition has its corresponding BPT, APTAG, APT, and ANDing operation.

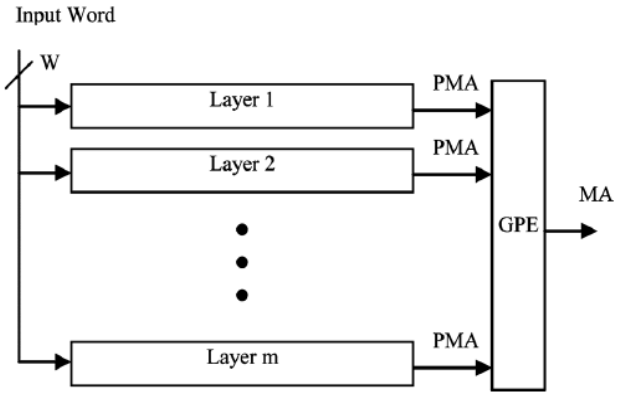

Figure 3. Memory Architecture of HP-SRAM based TCAM

V. Phases Of Hp Sram Based Tcam

HP SRAM-based TCAM has two phases: Data-and-Address Organizing and Storing (DAOS) phase, and Search phase.

A.DAOS phase

In this phase the hybrid partitioned TCAM is transformed into BPTs, APTs and APTAGs. The BPT and APT are mapped from the data and address positions of the TCAM memory.After mapping, LIs of their correspondinBPTs are set to their respective values.

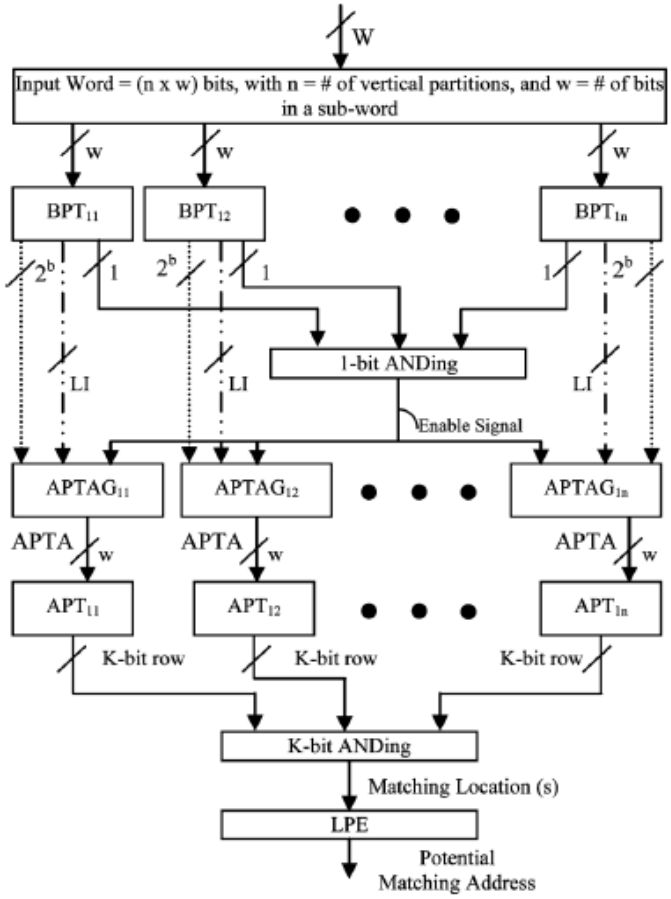

Figure 4.Architecture of a layer of HP SRAM based TCAM

Only those bit positions and address positions in BPTs and APTs, respectively, are high, which are mapped while remaining bit positions and address positions are set to low in BPTs and APTs, respectively. After mapping, LIs of their corresponding BPTs are set to their respective values.

A conventional TCAM table is shown in the table I.We have total of four hybrid partitions; with each one has dimensions of 4x4.Each ternary hybrid partition is then expanded into binary counterpart and processed to be stored in SRAM (BPT andAPT).After necessary processing HP1,HP2 HP3 and HP4 are mapped to their memory units (BPTs and APTs).APTs and BPTs for layer 2 (HP3 and HP4) are explicitly shown in Fig. 5. Layer 2 spans address range from 4 to 7, which are indicated in APTs of Fig. 5.

B. Search Phase

In this phase, an input word is applied and its MA, if exits, issent to output. The proposed TCAM accomplishes search operationin a layer as per steps depicted in the flow chart of Fig. 6.

In step 1, an input word is applied to a layer of the proposed TCAM. In step 2, the applied word is partitioned into "n" number of sub-words. These sub-words are then

applied to their corresponding BPTs in parallel. In step3 a sub-word is then divided into two portions: BPTA and BPI. Step3

Table I
TCAM Table And Its Hybrid Partitions

Address	Ternary Data								
	HP1				**HP2**				
0	0	0	0	0	1	0	1	0	Layer1
1	0	X	0	1	0	0	1	0	
2	1	0	0	1	1	0	0	X	
3	1	X	1	0	1	0	0	0	
	HP3				**HP4**				
4	X	0	0	1	1	0	1	0	
5	0	0	0	1	1	0	0	1	Layer2
6	1	0	0	0	1	0	0	0	
7	1	1	1	1	1	1	0	1	

APT3 **BPT3**

Address	Address positions				Address	Last index	Bit positions			
	4	5	6	7						
0	1	1	0	0	00	-1	0	1	0	0
1	0	0	1	0	01	0	0	0	0	0
2	1	0	0	0	10	0	1	1	0	0
3	0	0	0	1	11	2	0	0	0	1

APT3 **BPT3**

Address	Address positions				Address	Last index	Bit positions			
	4	5	6	7						
0	0	0	1	0	00	-1	0	0	0	0
1	0	1	0	0	01	-1	0	0	0	0
2	1	0	0	0	10	-1	1	1	1	0
3	0	0	0	1	11	2	0	1	0	0

Figure 5. APT And BPTs For Layer2

occurs for all sub-words in parallel. In step 4, bit position in BPT indicated by BPI in the row selected by BPTA is read out. If the read out bit is high (1), it shows that input sub-word is considered present otherwise not but at which address, still unknown. Step 4 is also performed in parallel for all BPTs. In step 5, the read out bits from all BPTs in step 4 are ANDed. Step 5 corresponds to 1-bit ANDing in Fig. 3. The result of this 1-bit ANDing operation specifies whether the searching effort is to be continued or to be stopped.

If the 1-bit ANDing results in a low signal, it means that mismatch has occurred and shows end of search phase in the layer, otherwise the proposed TCAM sustains search operation in the layer and enters step 6 where APTAG computes APTA by summing the number of one's in the selected row up to the bit position inclusive indicated by BPI and LI of the selected row of BPT. Step 6 is also carried out in parallel for the computation of all the APTAs. In step 7, APTAs, from step 6, read out rows from their corresponding APTs simultaneously. Step 8 shows ANDing operation.. The address positions that remain at high level after ANDing are considered possible matching locations. In the last step, step 9, LPE selects PMAamongmatching locations of step 8, otherwise a mismatch of the layer is signalled.

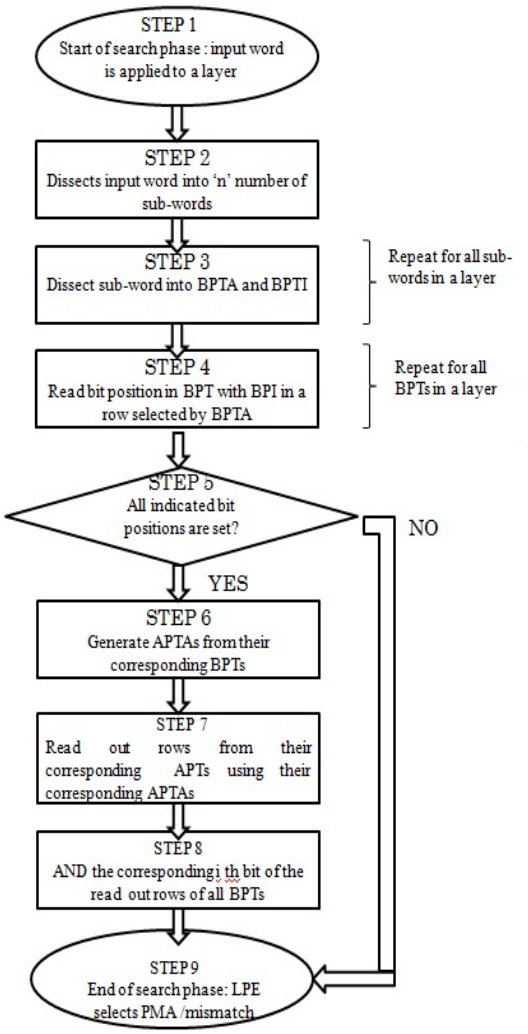

Figure 6.Flow chart of search phase

VI. PARITY BASED TCAM

The parity bit based CAM design isshown in Fig.7 consisting of the original data segment and an extraone-bit segment, derived from the actual data bits[5]. We only obtain theparity bit, i.e., odd or even number of "1"s. The obtained parity bit isplaced directly to the corresponding word and ML. Thus the new architecture has the same interface as the conventional CAM with one extra bit. During the search operation, there is only one single stage as in conventional CAM.

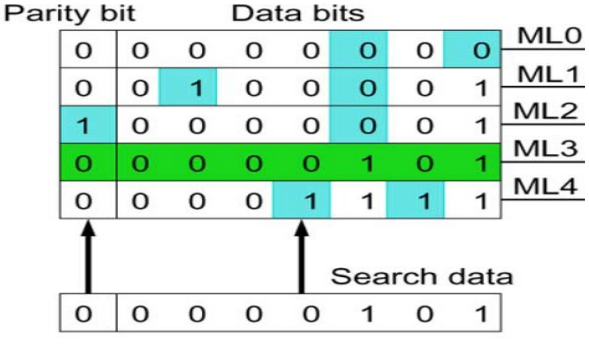

Figure 7.Parity bit based CAM

Hence, the use of this parity bits does not improve the power performance. However, this additional parity bit, in theory, reduces the sensing delay and boosts the driving strength.

In the case of a matched in the data segment (e.g., ML3), the parity bits of the search and the stored word is the same, thus the overall word returns a match. When 1 mismatch occurs in the data segment (e.g., ML2), numbers of "1"s in the stored and search word must be different by 1. As a result, the corresponding parity bits are different. Therefore now we have two mismatches (one from the parity bit and one from the data bits). If there are two mismatches in the data segment (e.g., ML0, ML1 or ML4), the parity bits are the same and overall we have two mismatches. With more mismatches, we can ignore these cases as they are not crucial cases. The sense amplifier now only have to identify between the 2-mismatch cases and the matched cases. Since the driving capability of the 2-mismatch word is twice as strong as search speed

VII. Analysis Of Parity Based Tcam With Conventional Tcam

A sample design of conventional TCAM and parity bit based TCAM have been implemented and verified on Xilinx Spartan 3E FPGA[6].The sample design has been synthesized using Xilinx ISE synthesizer and place & route tools. In this project an input word of 8 bits has been divided into two sub-words each of which is of 4 bits.Each sub-word has then been applied as an address to its corresponding memory module.Data accessed from a BPT has been processed using its corresponding APTAG to generate APTA for its corresponding APT.

The output waveform is shown in the fig.8.Table II contains the device utilization summary of the parity based TCAM.

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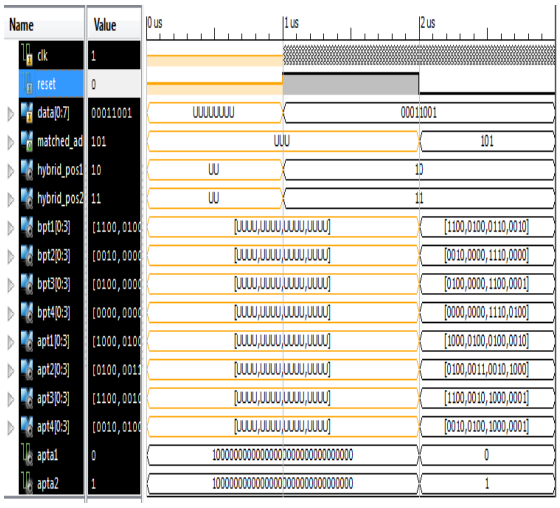

Figure 8.Waveform of Parity based TCAM

Table II
Device utilization summary

Device Utilization Summary			
Logic utilization	Used	Available	Utilization
Number of slices	45	2448	1%
Number of slice flip flops	11	4896	0%
Number of 4 input LUTs	77	4896	1%
Number of bonded IOBs	12	66	18%

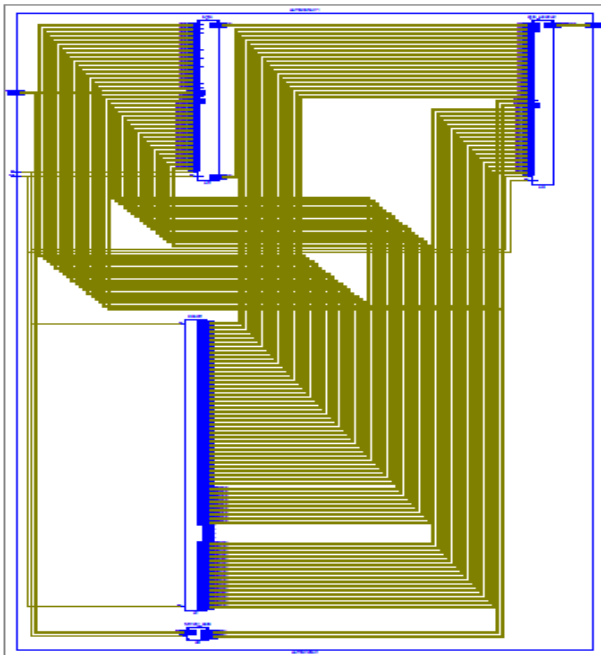

Figure 9. RTL view of TCAM

The inputs are data,clock and reset.The data input is the 8 bit input word given to the memory.Reset is a high to low signal.In the example the data input is 0001101 which is shown in the table I and the out put is matched data which gives the address of the input data word.In this example the output is 101 which is shown in the simulation result in fig 8.And the intermediate outputs are also shown in the waveform.

VIII. Conclusion

This paper represents the design and implementation of a parity bit based TCAM. TCAMs are gaining importance in highspeed lookup-intensive applications. However, the high-power consumption of TCAMs is limiting their popularity and versatility. The work done here gives a reusable Verification Environment for CAM/TCAM. This work also proposed a parity bit to improvise the searching speed. Thesearching operation was successfully performed using the additional circuitry that was added to the TCAM cell. The output obtained was satisfactory and was in accordance with the actual results obtained.

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