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DESIGN OF PARALLEL MULTIPLIERS USING HIGH SPEED ADDER

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ABSTRACT: **In recent years, power dissipation is one of the biggest challenges in VLSI design. The number of transistors are reduced in the circuit and ultra-low power design. In this project based on full adders are designed using EX-OR gates and different techniques are used for low power in full adders. The main aim of this paper is to reduce the power dissipation and area by reducing the number of transistors. In this project various types of full adders design are performed. Multipliers are the main sources of power dissipation in DSP blocks and Digital circuit systems. The design analysis of delay and power comparison of the low power using different types of full adder adders units and Parallel Multipliers. The parallel multipliers are Braun Multiplier and Vedic Multiplier. The designs are implemented delay and power results are obtained using Mentor Graphics EDA tool.**

KEYWORDS: **EX-OR gate, AND gate, Full adders, CMOS circuit, Ripple Carry Adder, Power Dissipation, Delay.**

I Introduction

Moore's law explains the requirement of the transistors for VLSI design it gives the empirical observation that transistor density and performance of integrated circuits, doubles every year, which was then revised to doubling every two years. The design of multiplier, full adders forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design goals are minimizing the number of transistor count, minimizing the power consumption and increasing the speed. Great effort has been concentrated on low-power microelectronics due to high-speed development of laptops, portable systems and cellular networks.

Adder is the core element of complex arithmetic circuits as it is used in the arithmetic logic unit (ALU), in the floating-point unit, and for address generation in case of cache or memory access. To reduce the power and area requirements of the computational complexities, the size of transistors are shrunk into the deep sub-micron region and predominantly handled by process engineering.

Many design architecture and techniques have been developed to reduce power dissipation complementary logic, Pseudo NMOS Dynamic CMOS, Clocked CMOS logic, CMOS Domino logic, Cascade voltage switch logic (CVSL), Modified Domino logic, Pass Transistor Logic (PTL), have been proposed. The power consumption of a CMOS circuit can be decomposed into two type's static and dynamic power dissipation.

The steady state power dissipation of a circuit is expressed by the following relation,

$$P_{static} = I_{stat} V_{dd} \quad \text{----- (1)}$$

The dynamic component of power dissipation is due to its transient switching behavior of the CMOS device,

$$P_{dynamic} = \alpha C V_{dd}^2 f \quad \text{-----(2)}$$

This paper is organized as following. Section II implementation of EX-OR gate. Section III introduces implementation of full adder. Design of full adder using Braun Multiplier and Vedic Multiplier section IV, Simulation and comparative analysis in table forms are shown in Section V, followed by the conclusion in Section VI.

II. DESIGN OF CMOS TRANSISTORS USING EX-OR GATE

The circuit performance improve in through transistor count minimization. EX-OR gates form the fundamental building block of full adders.

The basic EX-OR operation is, if the two inputs are same then the output is produced by an EX-OR gate is zero. If the inputs are changing the values, then the output is one. The following fig. (1-2) are 3T transistor, 2T transistor Schematic diagrams.

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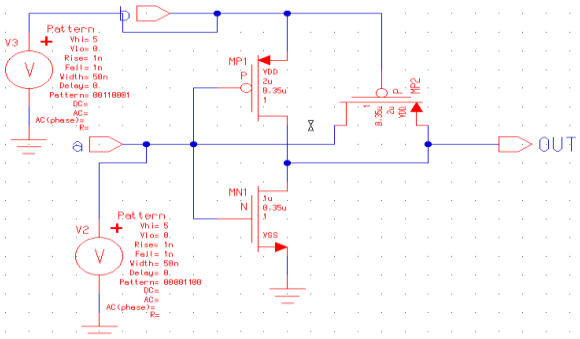

Fig. 1 Three Transistor EX-OR

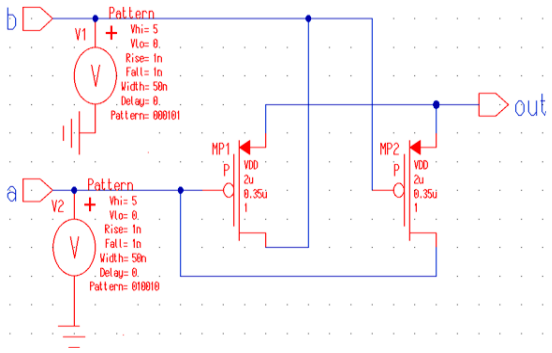

Fig. 2 Two Transistor EX-OR

The transistor count reduces, if the circuit Operating Speed is increased, Area and power consumption are very small.

III. DESIGN OF CMOS TRANSISTORS USING FULL ADDER

The basic design of CMOS full adder schematic structure, in which forms the basic building blocks of all digital VLSI circuits, occupying more area, speed is low, and high power dissipation. The performance of the EX-OR gates can significantly improve the performance of the adder. The early designs of EX-OR gates were based on either eight transistors is conventionally used in most designs.

The Full Adder output equation is given by,

$$SUM = A \oplus B \oplus C \text{ and}$$

$$CARRY = AB + BC + CA$$

The static CMOS Full adder is implemented by using 28 transistors. It can also minimize the number of transistors by using the CMOS Transmission gate and CMOS inverter logic. With this logic we reduce the number of transistors to 20. By using Pass transistor logic we can minimize the static power dissipation and number of transistors. Full adder is design with 14 transistors by using Pass transistor logic. Which leads the moderate power dissipation. The full adder design also implemented by using 10 transistors.

The new design of full adders which forms the basic building blocks of all digital VLSI circuits. The analysis of full adders using transistor counts reduced schematic fig. (3-4) are following,

Mainly the EX-OR circuits are used in designing of full adder. In previous design the full adder is designed by using eight transistors. Which can dissipates more power compare to this work. In this paper the design of full adder using two transistors EX-OR gates can be implemented. The Six transistor Full adder schematic structure shown in fig.4.

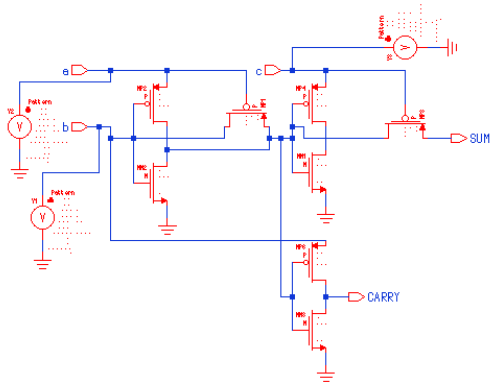

Fig.3 Eight CMOS Transistor Adder

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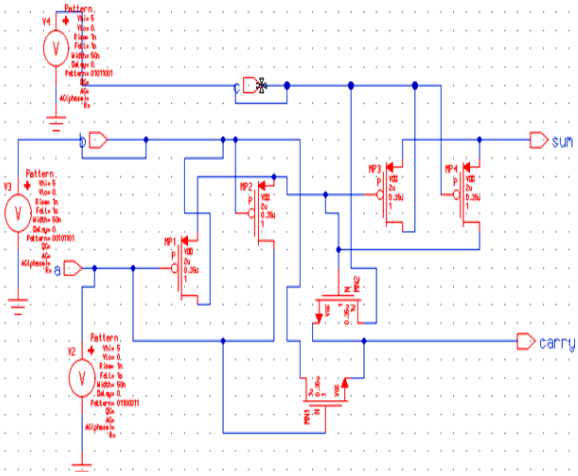

Fig.4 Six CMOS Transistor Adder

IV. DESIGN OF FULL ADDER USING MULTIPLIERS

High-speed multiplication is another critical function in a range of very large scale integration (VLSI) applications. Multiplications are expensive and slow operations.Multiplication is an important basic arithmetic operation and less common operation than addition, but it is still essential for microprocessors, digital signal processors and graphic engines. Multiplication is logically carried out by a sequence of addition, subtraction and shift operations. Therefore, high-speed multiplication can be achieved by having a high-speed multiplier. The multipliers are the structures where there will be many cascading stages of the full adder, so the performance of the full adders while cascading too many stages can be easily studied by analyzing the power, delay, power-delay product of the different multipliers made from different adders.

DESIGN OF FULL ADDER USING BRAUN MULTIPLIER

Braun multiplier is an uncomplicated parallel multiplier generally called as carry save array multiplier. The structure consists of array of AND gates and adders arranged in the iterative way and no need of logic registers. This can be called as non – addictive multipliers. In the internal structure, each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders.

The carry out will be shifted one bit to the left or right and then it will be added to the sum which is generated by the first adder and the newly generated partial product. The design of full adder using Braun Multiplier diagram shown in below fig. (5-6).

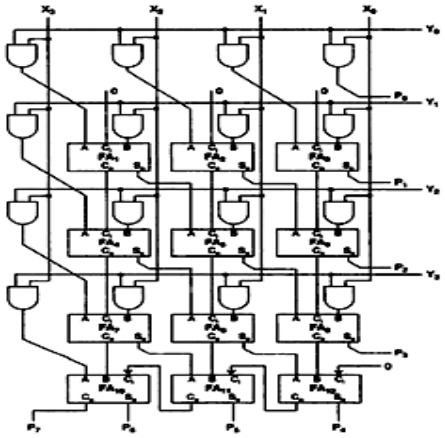

Fig. 5 Architecture of 4x4 Braun Multiplier

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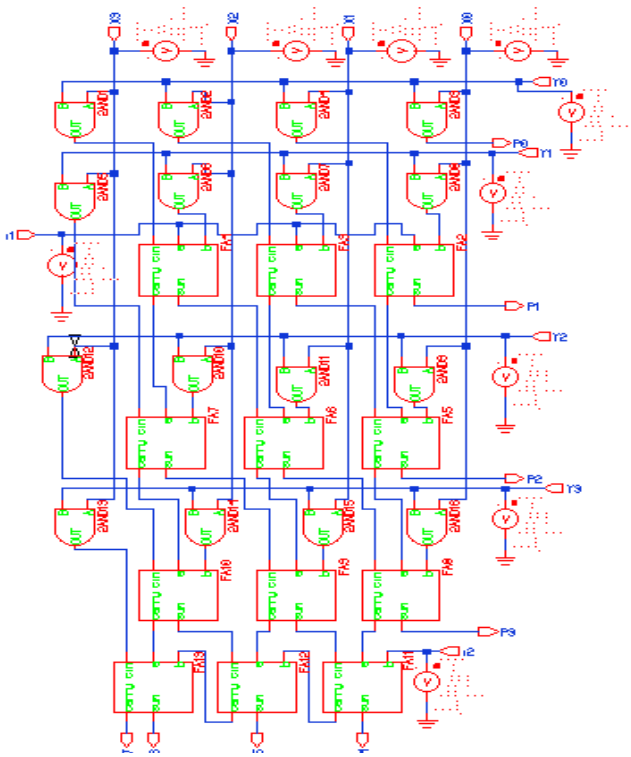

Fig. 6 Braun Multiplier circuit (4x4)

DESIGN OF FULL ADDER USING VEDIC MULTIPLIER

Vedic Multiplier is a Vertical Crosswise structure, it generates all partial products and their sum in one step. Since the partial products and their sum are calculated in Parallel. The Vedic Multiplier is one of the fastest multiplier. The Vedic Multiplier works under Algorithmic basis.

Algorithm

1. Divided the Multiplicand A and Multiplicand B into two equal parts, Each consisting of [N to (N/2) + 1] bits and [N/2 to 1] bits respectively, where first bit parts indicates the MSB and other represents LSB.
2. Represents the parts of A as Am and Al and parts of B as Bm and Bl. Now represents A and B as AmAl and BmBl respectively.
3. For example AXB we have general format as shown in below.
   Am Al
   BmBl
   These inputs are multiplied with Vertical and Crosswise basis, Am x Bm, Am x Bl, Al x Bl
   Al x Bm
4. The individual multiplication products can be obtained by the partitioning method and applying the basic building blocks.

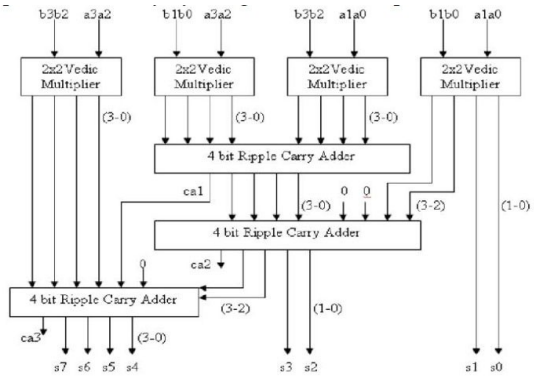

Fig. 7 Architecture of 4x4 Vedic Multiplier

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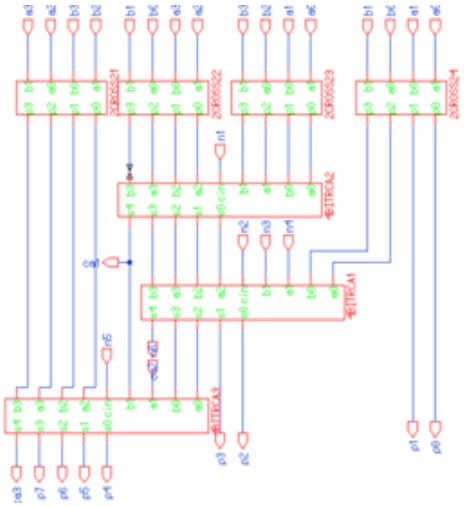

Fig.8 4x4 Vedic Multiplier

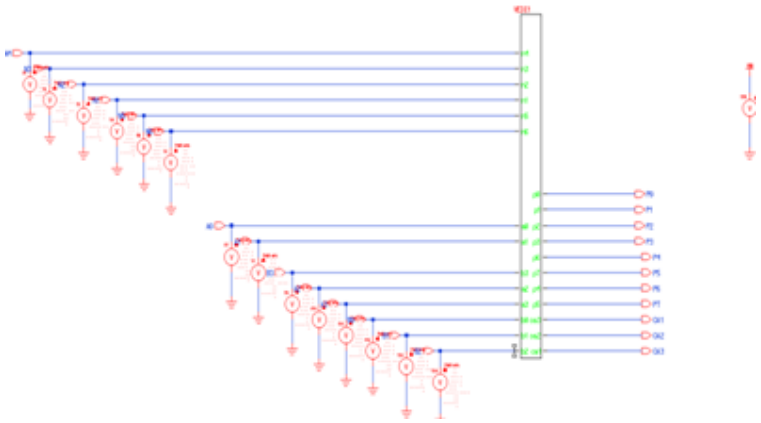

Fig. 9 Symbol of Vedic Multiplier

V.SIMULATION RESULTS AND COMPARATIVE ANALYSIS

In their CMOS EX-OR gate and full adder design shows the remarkable improvement in power-delay product. It also reduces the power consumption and reduces the silicon area. The Consumption of power and falling and rising times which are caused due to the difference in NMOS and PMOS transistors power consumption and speed. After the simulation, the layout of circuit is drawn. By the post simulation result along with a few corrections have achieved in sizes that the circuit has an accurate operation. Simulation results are performed by using digital schematic design tool of Mentor graphics tool. The CMOS logic EX-OR gate and CMOS logic full adder, the same output of an two multipliers like Braun Multiplier and Vedic Multiplier simulation results shown in fig. (10-12)

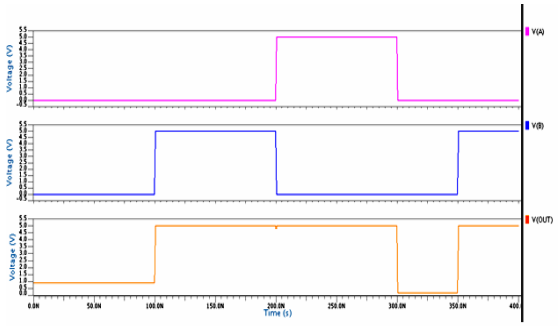

Fig. 10 Waveform of EX-OR Gate

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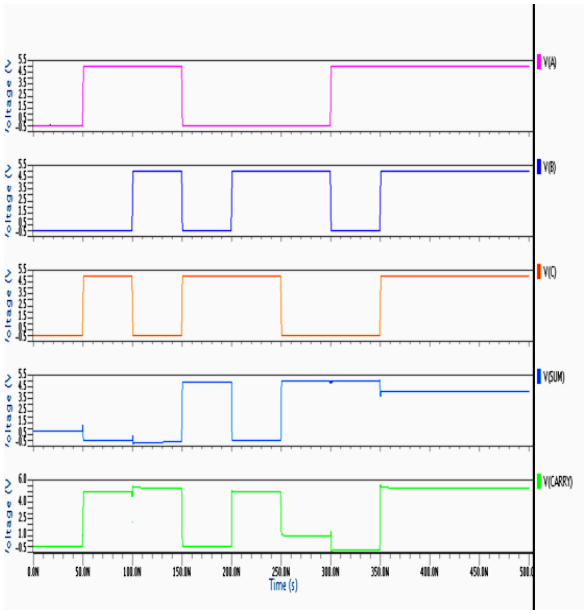
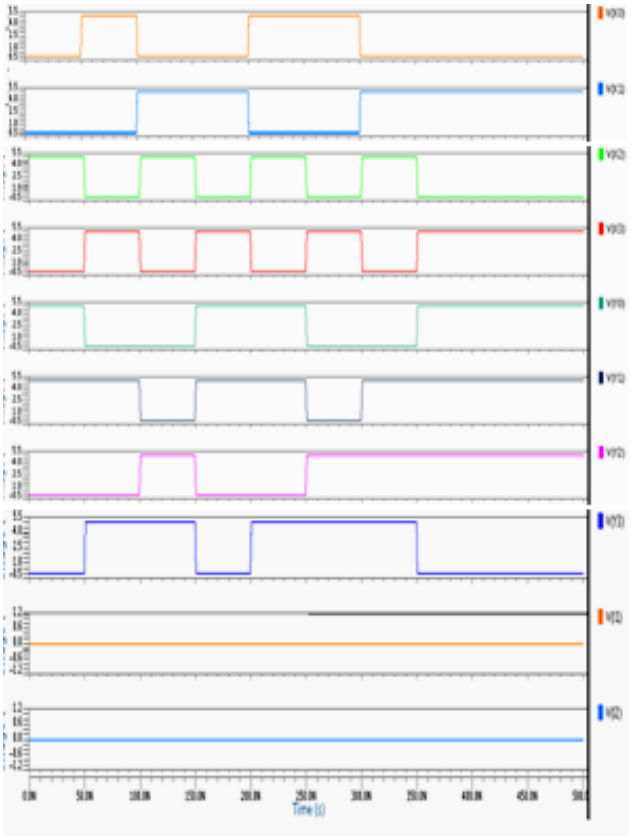


Fig. 11 Waveform of Full Adder

The output waveform of Braun Multiplier and Vedic Multiplier are given by, inputs as X3, X2, X1, X0 and Y3, Y2, Y1, Y0. Their outputs are given as P0, P1, P2, P3, P4, P5, P6, P7.



Inputs (X3-X0, Y3-Y0)

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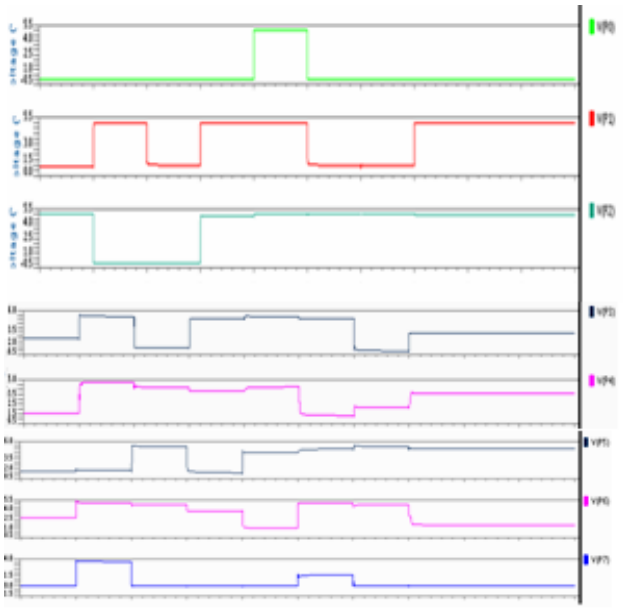

Outputs (P0-P7)
Fig. 12Waveform of Braun Multiplier

The comparison of the different EX-OR gates,, Full adders and 4x4 Braun and Vedic Multiplier are shown in tables (1-3) according to their transistor count, delay and power dissipation.

TABLE 1 Comparative Analysis of EX-OR

Structures	Number of Transistors	Delay (pS)	Power (pW)
Figure 1	3	95.72	90.506
Figure 2	2	40.67	89.315

TABLE 2 Comparative Analysis of Full Adder

Structure	Number of Transistors	Delay (nS)	Power (µW)
Figure 3	8	70.23	802.683
Figure 4	6	42.17	784.612

TABLE 3 Analysis of Braun Multiplier

Structure	Delay (nS)	Power (uW)
4x4 Braun Multiplier	50.00	972.1807
4x4 Vedic Multiplier	40.00	852.137

VI. CONCLUSION

In this paper different CMOS logic design families has been reviewed and evaluated based on the performance metrics like area, power, delay and transistor count. But the previous techniques have the disadvantages of transistor count, delay and power dissipation. The 3T XOR occupied more area and power dissipated when compared to 2T XOR, same as for 8T full adders are occupied more area, power dissipation and delay when compared to 6T full adder. The Braun Multiplier is used to multiply with up to 24x24, increasing the number of bits its difficult. In this Multiplier is used in unsigned numbers only. The future research activities may include integration of the proposed full Adders, in both signed and unsigned numbers multiplier systems.

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