International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 3, Issue 11, November 2014

Low Power and Reduce Area Dual Edge Pulse Triggered Flip-Flop Based on Signal Feed-Through Scheme

Ch.Sreedhar[1], K Mariya Priyadarshini[2]

***Abstract*: Flip-flops are the basic storage elements used extensively in all kinds of controlling units of IC's. In particular, digital design now a day's often adopt intensive pipelining techniques and employ many FF-rich modules. It is estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is high. As edge triggered is characterized by positive set up time causing large D-to-Q delays. In this paper an Explicit Dual Edge pulse Triggered FF (DETFF) with reduced area and power is proposed. When compared with the existing techniques the novel circuit proposed in this paper is suitable for low power, low area and high speed applications**.

***Key words*: Flip-flop (FF), Dual Edge pulse-triggering, signal feed through, Tanner EDA.**

I. INTRODUCTION

The increasing significance of portable system need to limit power consumption and reduce heat dissipation, in very large scale integration (VLSI) chips. This has led to rapid developments in low-power design during the recent years. The digital designs adopt synchronous circuit techniques and employ many flip-flops rich modules such as register file, shift register and first-in first-out. Flip-flops contribute a significant portion of chip area and power consumption to the overall system design.

The hard -edged flip-flops are characterized by positive setup time causing large D to Q delays. To reduce this disadvantage the pulse triggered flip-flops has been proposed. It reduces the two stages into one stage and it is characterized by soft edge property. For high speed operations of the conventional master-slave flip-flop a popular alternative is pulse triggered flip-flop. A pulse triggered flip-flop consists of pulse generator for generating strobe signals and a latch for data storage. The logic complexity and number of stages inside these pulse triggered flip-flop are reduced small D to delay.

Pulse triggered flip-flop are classified into two types implicit pulse triggered flip-flop and explicit pulse triggered flip-flop. In implicit pulse triggered flip-flop the pulse generated inside the flip-flop. For example: data close-to-output, Hybrid latch flip-flop (HLFF), semi dynamic flip-flop (SFF).

Manuscript received Nov, 2014.

***Ch.Sreedhar**, PG Scholar, ECE Department, SRK institute of Technology, affiliated to Jawaharlal Nehru Technological University Kakinada, Andhra Pradesh, India.*

***K Mariya Priyadarshini,** Assistant Professor, ECE Department, SRK institute of Technology, affiliated to Jawaharlal Nehru Technological University Kakinada, Andhra Pradesh, India.*

In Explicit pulse triggered flip-flop (E p-ff), the pulse is generated externally. These flip-flops can have the pulse generator is shared by neighboring flip-flops. Some of the techniques like explicit pulse data close- to- output (EP DCO), static conditional flip-flop (S-CDFF) are discussed in this paper. This sharing can help in distributing the power overhead of the pulse generator across many Explicit pulse triggered flip-flop. A system using explicit pulse triggered flip-flop will be more energy efficient than a system using implicit pulse triggered flip-flop.

Double-Edge Triggering (DET) has been implemented in the explicit pulse triggered flip-flops, but it is difficult to deploy in implicit pulse triggered flip-flop. (DET), data latching or sampling is issued at both raising and falling edges. DET saves energy both in clock distribution network and also in flip flops. Even if we use half the frequency, we can maintain the same throughput of original system. Simulations are done using Tanner EDA tool and results are shown for implicit, explicit and dual edge triggering flip-flops.

II. PREVIOUS TECHNIQUES

A. Implicit Pulse Triggered Flip-Flops

1) Implicit data close to output

Implicit data close to output contains an AND logic-based pulse generator and a semi dynamic structured latch design. It has small delay and simple topology. It occupies small area and also it uses single phase clocking. The inverter I5 and I6 are used to latch data and inverter I7 and I8 are used to hold the internal node. Two problems exist in this design. During the rising edge, NMOS transistors N2 and N3 are turned. This leads to larger switching power. The other is, node X control two larger MOS transistor N2 and N3 are turned on. This leads to larger capacitance load which causes speed and performance degradation.

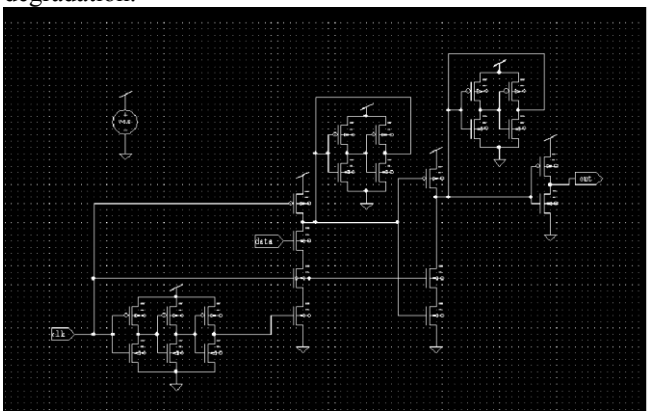

Fig.1 Implicit data close to output circuit diagram

2) Hybrid Latch Flip-Flop

In hybrid latch flip-flop, the unnecessary internal transition increase which increases the total power consumption of flip-flop. If the input is high a glitch is generated. The transistors in a stack degrade the performance of logic. Due to this problem the HLFF is not suitable for low power is required. To overcome this problem a semi-dynamic flip- latch flip-flop due to low number of transistor in stack flop had proposed. The semi-dynamic flip-flop is faster than hybrid but the total number of transistors is greater than the HLFF. To avoid unnecessary transitions, we proposed modified hybrid latch flip-flop.

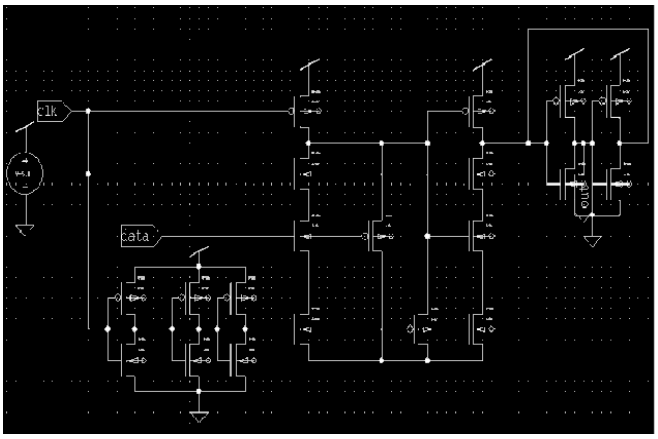

Fig.2 Hybrid Latch Flip-Flop circuit diagram

3) MHFF (Modified Hybrid Latch Flip-Flop)

Static latch structure is employed. Precharging of the node reduces the delay, but the power consumption is increased. Node X is not precharged periodically by the clock signal. When Q is low, the node is maintained high with the help of a weak pull-up transistor P1 which is controlled by the FF output signal Q. By using this design unnecessary discharging problem at node X is eliminated. It has the longer Data-to-Q, during the "0" to "1" transitions occur. This occurs due to node X is not pre-discharged. The area Consumption is high because we need larger transistors to enhance the discharging capability. When both data and output Q equal 1 there is extra power consumption because of the floating nodes.

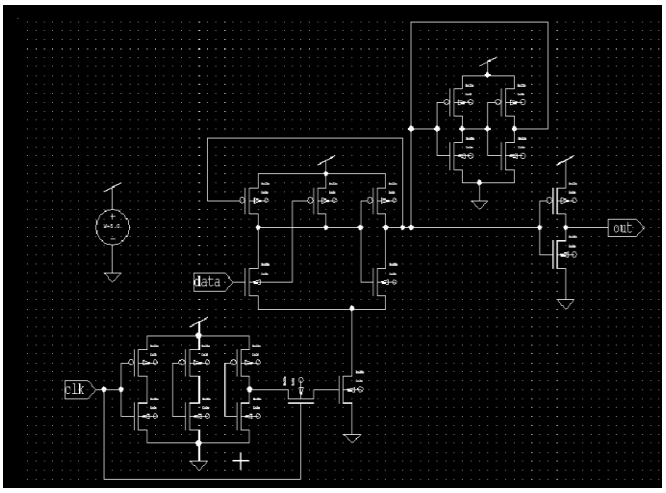

Fig.3 MHFF (Modified Hybrid Latch Flip-Flop) circuit diagram

4) SCCER (Single Ended Conditional Capture Energy Recovery Flip-Flop)

It uses a conditional discharged technique in which the discharge path is controlled by eliminating the switching activity when input the input stays in stable HIGH. The NMOS transistor N1 and N2 connected in series to eliminate the discharge path. An extra NMOS transistor N3 is used to eliminate the unwanted switching activity. The back to back inverters which are used instead of pull up and pull down resistors is replaced by a weak pull up transistor P1 and inverter I2 to reduce the load capacitance of node.

The Q_fdbk is used to control N3. So if D=1 there is no discharge. The discharge path is a long when input data is "1".

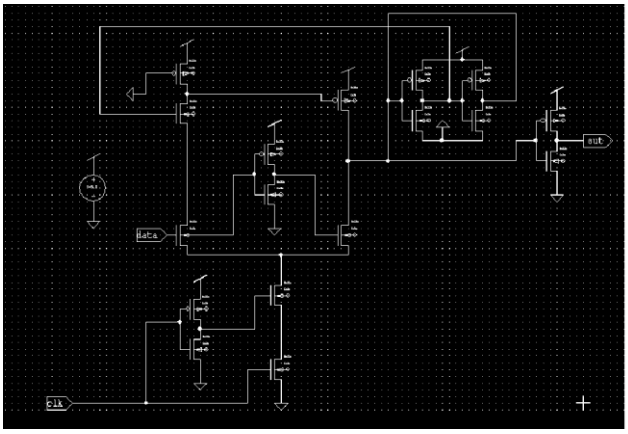

Fig.4 SCCER (Single Ended Conditional Capture Energy Recovery Flip-Flop) circuit diagram

B. Explicit Pulse Triggering Flip-Flop:

1) Explicit pulse data-close-to-output

It is considered as one of the fastest flip-flop due to semi-dynamic latch structure. It contains a NAND-logic-based pulse generator and true-single-phase-clock (TSPC). It is well suited for very high performance applications. In this flip-flop, the inverter I3and I4 are used to latch data and inverters I1 and I2 are used to hold the internal node X. this design has a drawback, when internal node X is discharge on every rising edge of the clock even the static input is "1". This leads to large switching power dissipation.

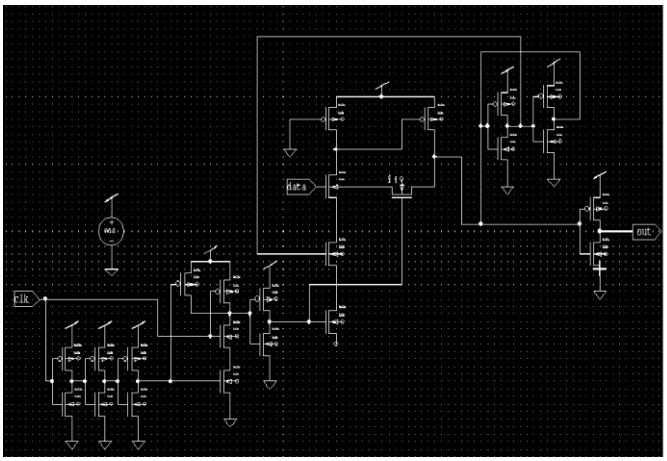

Fig.5 Explicit pulse data-close-to-output circuit diagram

2) Conditional discharged flip-flop:

The drawbacks in ep-DCO can be overcome in the conditional discharge techniques. An extra nMOS transistor

N3 controlled by the output signal Q_fdbk. Due to this no discharge occurs if the input data remains "1". It has a longer D-to-Q delay.

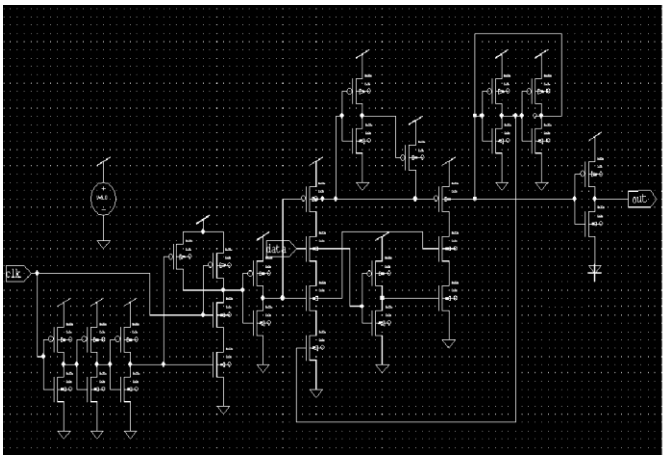

Fig.6 Conditional discharged flip-flop circuit diagram

3) Static Conditional discharged flip-flop**:**

In this design using static latch structure. Node X is periodically precharges. It exhibits the longer D-to-Q delay than the CDFF design. The CDFF and SCDFF, both designs face a worst case delay caused by a discharging path consisting of three stacked transistors N1-N3. To overcome delay for speed performance, a powerful pull down circuitry is need which cause extra layout area and power consumption.

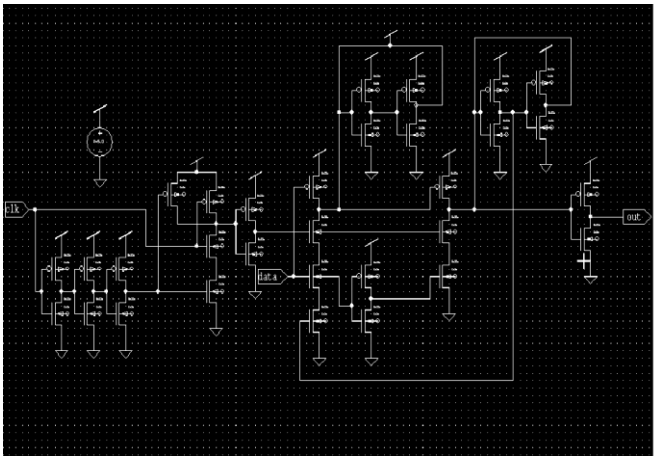

Fig.7 Static Conditional discharged flip-flop circuit diagram

4) Modified hybrid latch flip-flop:

To overcome the longer delay in SCDFF, modified hybrid latch flip-flop has proposed. It also uses the static latch structure. The keeper logic at node X is removed. The output signal Q is controlled by the weak pull up transistor P1 to maintain the level if node X when Q equal to "0". It has two draw backs, first, node 'X' is per charged a prolonged "0" to "1" delay is expected due to level-degraded clock pulse is applied to the discharging of transistor N3. Second, node X becomes floating and it may drift causes extra dc power.

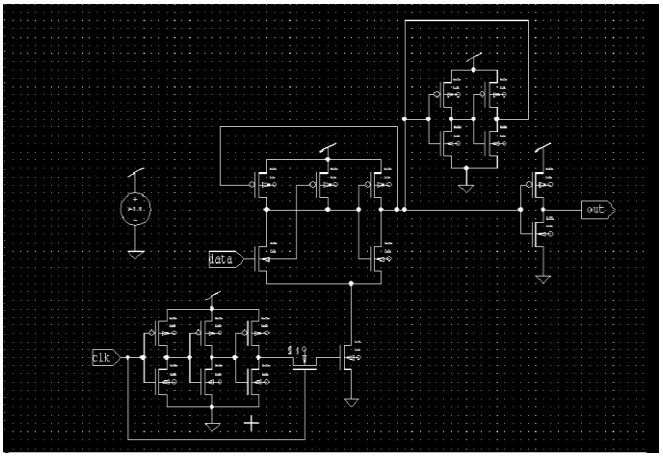

Fig.8 Modified hybrid latch flip-flop circuit diagram

5) Newly Modified Hybrid Latch Flip-Flop**:**

All pervious technique adopts worst case timing occurring at "0" to "1" data transitions. The proposed technique overcomes this delay by signal feed through technique. The proposed design is a static latch structure and a conditional discharge scheme to avoid the superfluous switching at an internal node. Proposed design has a several advantages. First, a weak pull transistor P1 is connected to ground with gate in the first stage of TSPC latch. This leads to pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. It also reduces the load capacitance of node X. Second, the pulse clock controlled the pass transistor N_X. So that input data can drive directly into the node Q. i.e., signal feed-through scheme. The pull-up transistor P2 at the second stage inverter of TSPC latch has a extra passage facilities auxiliary signal driving from the input source to node Q. the node can quickly pulled up to shorten the data transition delay. Third, the pull-down network of second stage inverter is completely removed. Here we employed pass transistor N_X provides a discharging path. The pass transistor N_X acts as two folded network. i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during 1 to 0 data transitions. The proposed technique saves the circuit design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The extra component in the proposed technique is an nMOS pass transistor to support signal feed through. The pass transistor improves the 0 to 1 delay and thus reduces the disparity between the rise time and fall time delays.

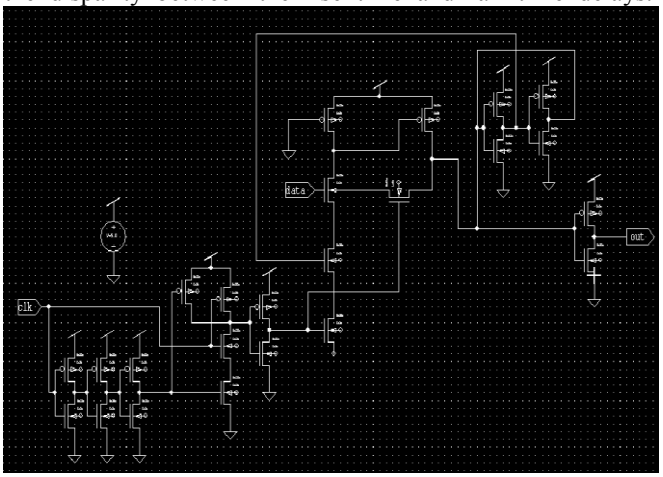

Fig.9 Newly Modified hybrid latch flip-flop circuit diagram

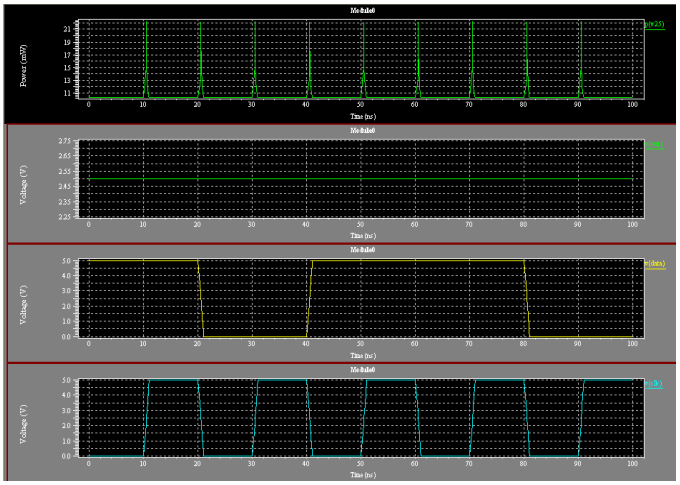

Fig.10 Newly Modified hybrid latch flip-flop wave form.

III. PROPOSED TECHNIQUE

DOUBLE EDGE TRIGGERED FLIP-FLOP:

Double edge triggered flip-flops reduced the clock frequency by half while keeping the data rate same. The DETFF design aim is saving energy both on the distribution network and flip-flops. In DETFF data latching or sampling is issued at both the rising and falling edges this leads to allow clock routing network to consume less power. In DETFF, the two operations being executed in one cycle with half the frequency. The clock switching activity is reduce by half this leads to power saving in the clock routing network

The DETFF can be implemented in two ways. First, insert additional circuitry to generate internal pulse signals on each clock edge. Second, duplicate the pathway to enable the flip-flop to sample data on every clock edge.

A. Double Edge Triggered Flip-Flop

The DET flip-flop is a basically a master slave flip-flop structure. It has two data paths. The upper data path consists of a single edge positive triggering flip-flop implementing using transmission gate. The lower data path consists of single edge negative triggering flip-flop implementing using transmission gate. Both the data paths have feedback loop connected, when flop is stopped the logic level at output is retained.

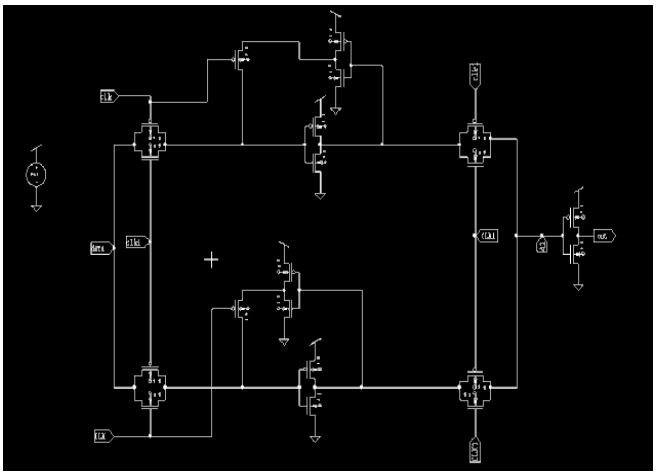

Fig.11 Double Edge Triggered Flip-Flop circuit diagram

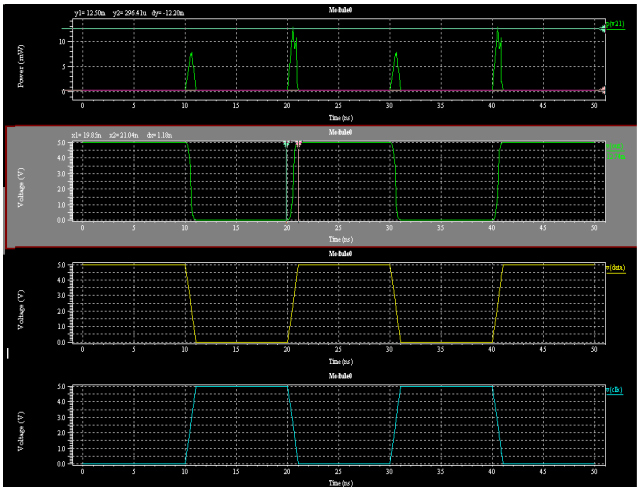

Fig.12 Double Edge Triggered Flip-Flop wave form

B. MODIFIED DOUBLE EDGE TRIGGE- -RED FLIP-FLOP

In modified double edge triggered flip-flop the feedback path has been changed when compared to DET Flip-flop. The upper data path is triggered on raising edge and lower data path is triggered at on falling edge. In this flip-flop an inverter and a PMOS transistor are used to hold the logic level when TG is placed. If data value is high the inverter switches the signal to low this leads to PMOS transistor pulls the data up to high. If data is low the inverter switches the signal to high which will isolate the data from VDD and keep the value to low. The MDET flip-flop acts as a static functionality for high output because PMOS transistor connected to VDD is used in the feedback network. The low output is not provided the static functionality of this flip-flop. Thus the circuit behaves as a dynamic circuit.

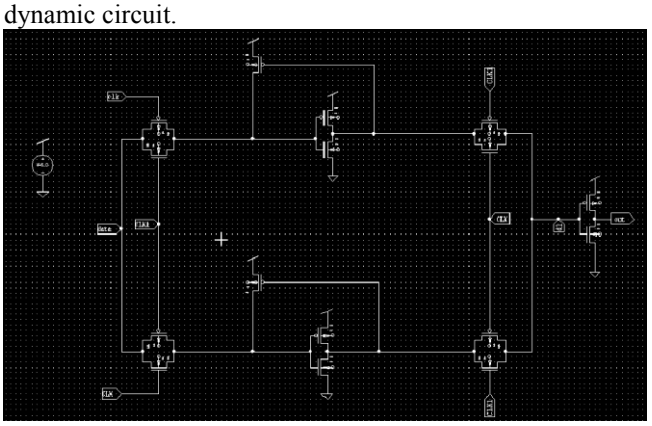

Fig.13 Modified Double Edge Triggered Flip-Flop circuit diagram

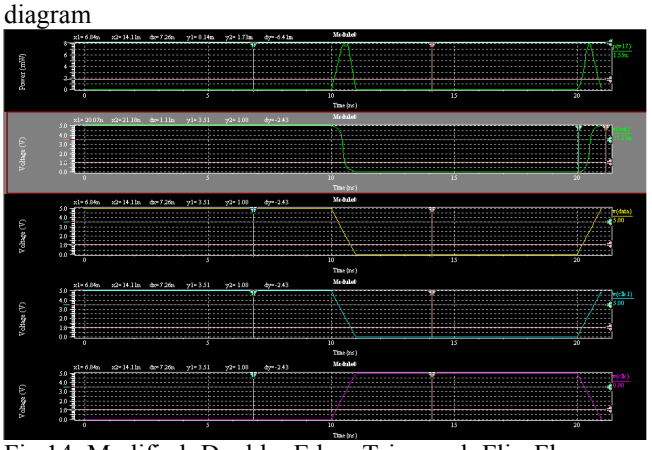

Fig.14 Modified Double Edge Triggered Flip-Flop wave form

C. Newly Modified Double Edge Triggered Flip-Flop

This flip-flop is faster than previous flip-flops due to number of clock transistor are reduced and replacing transmission gate by using n type pass transistor. This flip-flop is a master slave flip-flop structure and it consists of two data paths. The n type pass transistor is followed by an inverter which results in strong high.

The newly MDET flip-flop is free from threshold voltage loss problem of pass transistor. By using NMOS transistor in transmission gate .By replacing the p-type pass transistor by n-type transistor we can reduce the area due to NMOS is less than PMOS transistor. It is compensated the mobility constraint of NMOS and PMOS. Thus newly modified double edge triggered flip-flop is more efficient in area, power and speed when compared to previous flip-flop.

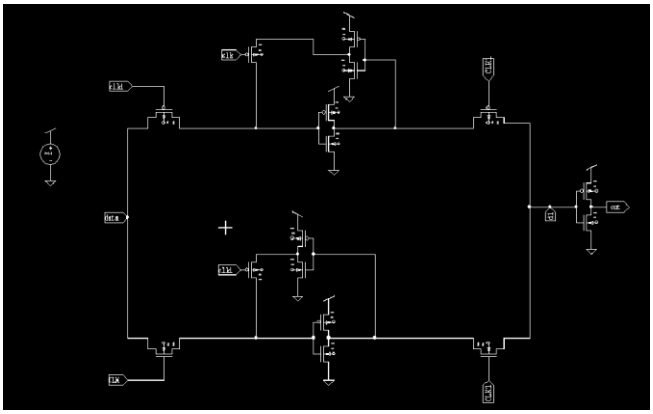

Fig.15 Newly Modified Double Edge Triggered Flip-Flop wave form

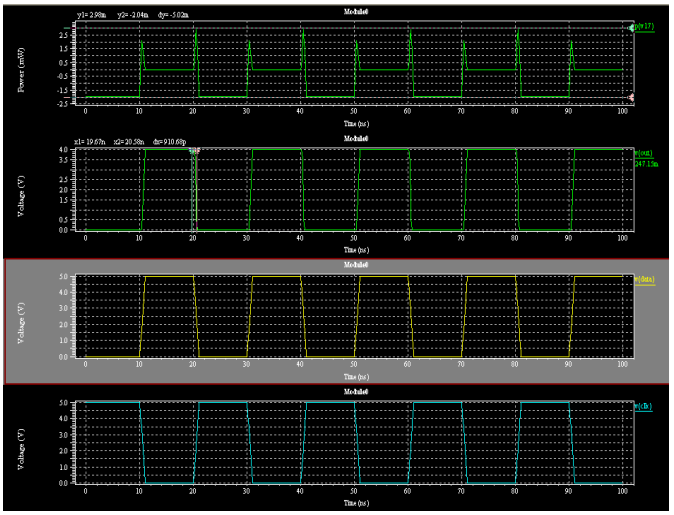

Fig.16 Newly Modified Double Edge Triggered Flip-Flop wave form

IV. SIMULATION RESULTS

The performance of pulse triggered flip-flops is design through simulations. All simulations are carried out using TSPICE simulation tool.. A conventional CMOS NAND-logic-based pulse generator design with a three stage inverter is used in explicit pulse triggering flip-flop but it will not used in EXMHLFF because it has own pulse generation circuitry. The pulse width design is crucial of data capture as well as the power consumption. The DETFF is proposed for storing the data in both rising edge and falling edge of clock signal. The performance for different designs is compared of implicit type P-FF, explicit type P-FF and double edge triggering flip-flop.

Table.1 Area, Power and Delay comparison of Implicit Pulse Triggered Flip-Flops

Technique	No Of Transistors	Delay (sec)	Dynamic Power (watts)	Logic Output '0' Static Power (watts)	Logic Output '0' Static Power (watts)
IMDCO	23	910.68p	10.79m	10.29m	8.66m
HLFF	20	546.41p	8.76m	7.02n	8.63m
MHLFF	19		16.87m	8.72m	11.10m
SCCER	17	964.69p	2.18m	13.76m	10.33m

Table.2 Area, Power and Delay Comparison of Explicit Pulse Triggered Flip-Flop

Technique	No Of Transistors	Delay(sec)	Dynamic Power(watts)	Logic Output '0' Static Power (watts)	Logic Output '0' Static Power (watts)
EXDCO	28	728.55	8.78m	2.06n	7.34n
EXCDFF	30	728.55	2.48u	4.00u	1.38n
EXSCDFF	31	546.41	10.16m	606.17u	8.71m
EXMHLFF	19	554.18	8.78m	2.06n	7.34n

Table.3 Leakage Power Calculation of Explicit Pulse Triggered Flip-Flop

Flip-flop designs	EX-DCO (Power in watts)	CDFF (Power in watts)	SCDFF (Power in watts)	MHLFF (Power in watts)	NMHLFF (Power in watts)
(CLK, Data)= (0 , 0)	6.03n	3.98u	15.82u	8.67m	10.29m
(CLK, Data)= (0 , 1)	5.08n	2.64m	10.30m	6.76m	10.29m
(CLK, Data)= (1 , 0)	4.73n	16.474u	186.45u	10.29m	10.29m
(CLK, Data)= (1, 1)	4.74n	-1.39n	10.31m	11.06m	10.29m

Table.4 Area, Power and Delay Comparison of Dual Edge Triggered Flip-Flop

Technique	No Of Transistors	Delay	Dynamic Power
Double Edge Triggered Flip-flop	20	2.11ns	12.20mw
Modified Double Edge Triggered Flip-flop	16	1.82ns	8.14mw
Newly Modified Double Edge Triggered Flip-flop	14	2.35ns	5.02mw

Table.5 Leakage Power Calculation of Leakage Power of DET

Flip-flop Designs	Double Edge Triggered Flip-flop (Power in watts)	Modified Double Edge Triggered Flip-flop (Power in watts)	Newly Modified Double Edge Triggered Flip-flop (Power in watts)
(CLK, Data)= (0 , 0)	5m	5.5micro	6.9m
(CLK, Data)= (0 , 1)	322.21u	1.55n	14.45m
(CLK, Data)= (1 , 0)	1.34n	5.5	11.56n
(CLK, Data)= (1 , 1)	3.05m	1.55n	11.6n

V. CONCLUSION

The proposed double edge triggered flip-flop is having less number of clocked transistors than existing flip-flop designs. Due to reduction in no of transistor in a circuit, the overall delay will also reduce. Thus reducing the overall switching delay power, and area consumption. The DET-FF can perform two operations being executed in one cycle, if we use half the frequency. By reducing the frequency into half, the clock switching activity is reduced by half. It will leads to power saving in the clock routing network. Therefore the proposed design well suits for low power and high performance application.

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Author Profile

Ch.Sreedhar received his Bachelor of Technology degree in Electronics and Communication Engineering from Jawaharlal Nehru Technological University Kakinada, Andhra Pradesh, India in 2012. He is pursuing Master of Technology degree from the department of Electronics and Communication Engineering, at of SRK Institute of Technology Enikepadu Vijayawada, Andhra Pradesh, India. His areas of interest include analog IC design, digital communication and Low Power VLSI design**.**

K.Mariya Priyadarshini received her Bachelor of Technology degree in Electronics and Communication Engineering from Vaagdevi College of Engineering, Warangal affiliated to Jawaharlal Nehru Technological University Hyderabad, Andhra Pradesh, India. She is awarded Master of Technology degree in VLSI Design from Karunya University, Coimbatore Tamilnadu, India. At present she is working as an Asst.Professor in SRK Institute of Technology Enikepadu Vijayawada, Andhra Pradesh, India Her areas of interest include Analog IC design, Low Power VLSI design, ASIC design, CPLD'S and FPGA'S**.**

