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Comparative Analysis and Optimization of Active Power and Delay of CMOS &DTMOS 1Bit and 8-Bit Full Adders

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Abstract- To optimize the power use of goods and services of a digital design such as that of an integrated circuit, while keeping up the functionality, we believe the power optimization is the employment of electronic design automation tools. The performance analysis and comparing between several parameters that are power delay, powerful, delay product of different 1-bit and 8-bit CMOS full adders that are conventional CMOS with different full adders has been presented here. The increasing speed and complexity of today's designs, implies a significant increase in the power consumption of very-large-scale-integration (VLSI) chips. In this paper proposed full adder is a novel 1-bit full adder cell which uses only eight transistors also three multiplexers and one inverter are applied to minimize the transistor count and bring down power consumption. The low power and low transistor count make the novel 8T full adder cell a candidate for power efficient application. The plans have been borne away by the HSpice tool at 180nm and 45nmtechnologies. DTMOS is where the body is linked up to gate. These techniques offer high current device comparable to CMOS circuits operated at lower voltages (i.e. sub threshold). The leakage current produced by DTMOS circuits during OFF state is comparable with leakage currents of CMOS circuits.
***Keywords*: CMOS, power delay, Full-Adder, DTMOS, Power minimization**

I. INTRODUCTION

The craze for portable electronics in daily life is forcing designers to target for operation at high speed, low power energy and higher reliability. Compared to existing techniques 28T, 16T, 14T, 10T transistors full adder, the proposed design adder shows a significant improvement in silicon area and power, time lag and power delay product. In the present days there is an ever-increasing number of portable applications requiring lower-power and higher throughput than ever before for example, notebook and laptop computers, representing the fastest growing segment of the computer industry, are demanding the same computation capabilities as found in desktop machines. The explosive increase in laptops and portable systems and in cellular networks has intensified the research efforts in low power microelectronics. To increase the focal ratio of the circuits all the circuits are implemented using DTMOS at 45nm technology. The sub threshold circuit experience large delays and thus they cannot be used in high frequency applications. There are several issues related to the full adders. Some of them are power consumption, performance, area, noise immunity and regularity and good driving ability.

Several works have been done in order to decrease transistor count and consequently decrease power consumption and area. A full adder has three inputs and two outputs block in which the outputs are the addition of three inputs. Basic fundamental units used in various circuits such as parity checkers, compressors and comparators are full adders [5]. This technique uses high threshold voltage sleep transistor which cut-off a circuit block when the block is not switching [3]. In some designs, reducing transistor count has been resulted in threshold loss problem that causes non-full swing outputs [4], low speed and low noise immunity especially when they are used in cascaded fashion. Some of them has threshold loss problem that cause non-full swing outputs, the sent low speed and low noise immunity. However, usually they have less power consumption in comparison to full adders with full swing outputs. Not full swing full adders are useful in building up larger circuits as multiple bit input adders and multipliers. In Integrated Circuits mainly two types of full adders (Static & dynamic) are used. Static full adders commonly are more reliable, simpler and lower power than dynamic ones.

II. RELATED WORK

In the existing method implementation part, The performance analysis and comparison between various parameters that are power, delay, power delay product and rise time ,fall time of different 1-bit and 8-bit CMOS full adders that are 28T,16T,14T,10T are presented here. Many efforts have recently done to implement high-speed and low-power 1-bit full adder cells with smaller area [9,3]. In this paper, we propose a systematic approach to design 10-transistor full adders.

CONVENTIONAL 28T CMOS FULL ADDER:

The 1-bit conventional CMOS full adder cell is shown in Fig1. The 1-bit full adder cell has 28 transistors.The CMOS design style is not area efficient for complex gates with large fan-ins. Thus, care must be taken when a static logic style is selected to realize a logic function. The pseudo NMOS technique is straightforward. The pass transistor logic style is known to be a popular method for implementing some specific circuits

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such as multiplexers and XOR-based circuits, like adders.

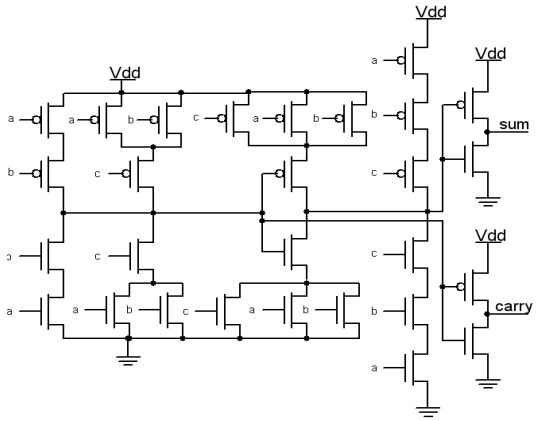

Fig.1. Conventional CMOS Full Adder

REVIEW OF FULL-ADDER DESIGN

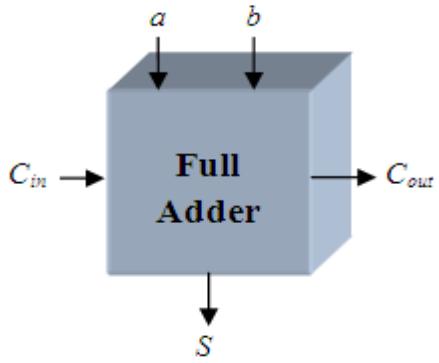

Fig.2: Block diagram representation of one-bit full adder.

A 1-bit full adder adds three one bit numbers, frequently written as A, B and C. A and B are the operands and C is a bit carried in from the next less important stage. Full adder is typically a part in a cascade of adders' binary numbers [9].

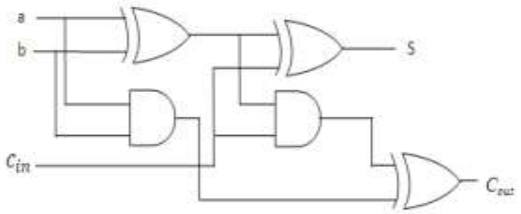

Fig. 3: Schematic of a Full Adder.

The circuit generates a two-bit output sum typically represented by the signals Carry and Sum. Sum could be made the three bit XOR of A, B, and C and Carry could be made the three-bit common function of A, B, and C.

The expression of Sum and Carry outputs of 1-bit full adder based on binary inputs A, B, C are represented as:

$$Sum = A \oplus B \oplus C \ldots\ldots\ldots\ldots\ldots (1)$$

$$Carry = AB + BC + CA \ldots\ldots\ldots\ldots (2)$$

16T FULL A DDER

The novel adder cell (NEW) has 16 transistor presented here, However, the XOR-XNOR module has been modified to reduce delay and power consumption. lower power and delay has been obtained at the expense of 2 additional transistors.

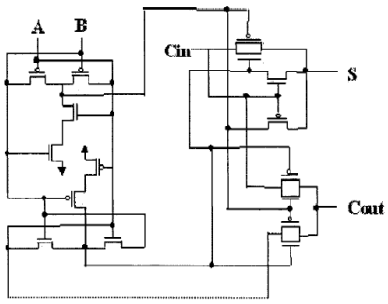

Fig. 4. 16T full adder

14T Full Adder:

The 14T adder with 14 transistors consumes considerably less power in the order of microwatts and has higher speed. The 14T adder reduces threshold loss problem compared to the previous different types of transistor adders.

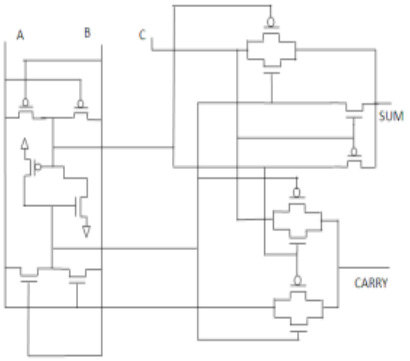

Fig.5: Schematic of 14T Full Adder 45nm technology

10T Full Adder

In this study we investigated the power and delay performance characteristics of adder using 10-transistor adder circuits. The basic benefit of 10 transistors full adders.

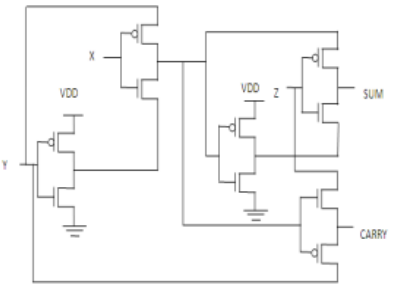

Fig.6: Schematic of 10T Full Adder 45nm technology

III. POWER CONSIDERATIONS

The aim to design the system for low power is not a straight forward task, as it is involved in all the IC-design stages.

There are several sources of power consumption in CMOS circuits:

1) Switching Power: Due to output switching during output transitions.

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2) Short Circuit Power: Due to the current between VDD and GND during a transistor switching.

3) Static Power: Caused by leakage current and static current.

IV. RIPPLE CARRY ADDER

A ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascaded, with the carry output from each full adder connected to the carry input of the next full adder in the chain. Fig shows the interconnection of eight full adder (FA) circuits to provide a 8-bit ripple carry adder. Notice from Fig 1 that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits a0 and b0 in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits s0-s7. In the ripple carry adder, the output is known after the carry generated by the previous stage is produced.

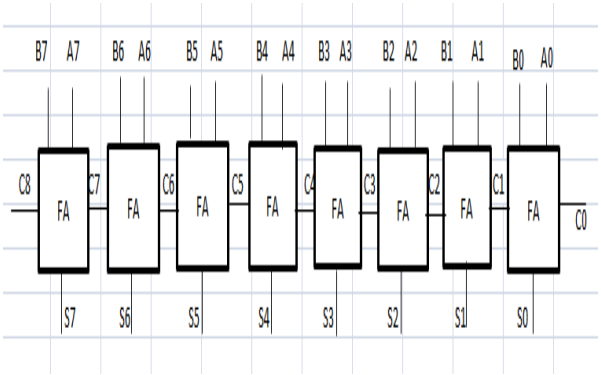

Fig.7 . 8-bit ripple carry adder

1. Designing Ripple Carry Adder

A standard 8-bit ripple-carry adder built as a cascade from eight 1-bit full-adders. C0 for carry-in, inputs are A0..A7 and B0..B7.To demonstrate the typical behavior of the ripple-carry adder, very large gate-delays are used for the gates inside the 1-bit adders - resulting in an addition time of about 0.6 seconds per adder. Note that each stage of the adder has to wait until the previous stage has calculated and propagates its carry output signal. Therefore, the total delay of a ripple-carry adder is proportional to the number of bits. Faster adders are often required for bit widths of 16 or greater. Each full-adder built by using a new CMOS technology which consumes less power. The PDP exhibited by the full-adder would affect the system's overall performance.

V. OVERVIEW OF 1-BIT 8T FULL ADDER

The full adder function can be described as follows; the addition of two 1-bit inputs A and B with forestage carry C_{in} calculates the two 1-bit outputs sum and C_{out} , where

sum = A ⊕ B ⊕ Cin……(1)

Cout= Cin (A ⊕ B) +AB .....….(2)

In this design ,the Boolean function as

Sum = (A⊕C_{in}) ·(C_{out})' + (A⊕Cin)' ·B……..(4)

Cout = (A⊕Cin) · B + (A⊕Cin)' ·A……..(5)

From Eqs. (3) and (4), the 8T design is proposed(Fig. 7).

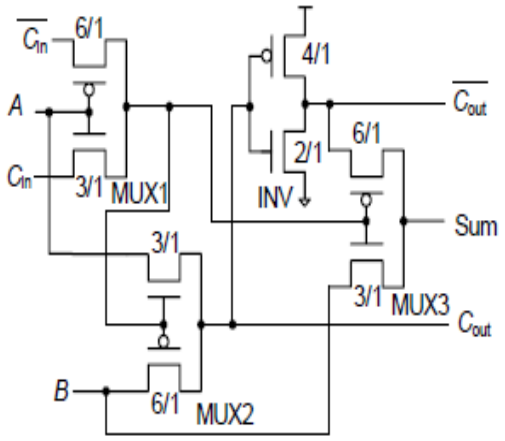

Fig.8. The proposed 8-transistor full adder(8T)

The entire design process can be divided into several steps as follows:

1. in *(A⊕C)'* (or *A⊕C*in) is needed as a control signal in multiplexers MUX2 and MUX3 to generate *C*out and Sum. In this study, in *(A⊕C)'* is implemented by MUX1 (Fig. 7).

2. The multiplexer circuit MUX2 is adopted in our proposed design to generate *C*out followed by an inverter INV. The inverter has three advantages for the circuit: firstly, it speeds up the carry propagation as a buffer along the carry chain. Secondly, it provides

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complementary signals needed for the generation of Sum. Thirdly, the inverter can improve the output voltage swing as a level restoring circuit (Lin *et al*., 2007).

3. The Sum is generated by the multiplexer MUX3 passing either *B* or out C_{out}' according to the value of in $(A \oplus C)'$.

The proposed full adder circuit, which uses three multiplexers and an inverter, requires eight transistors. Choosing appropriate width to length rates of transistors, *W*/*L*, improves the threshold drop of the circuit (Chowdhury *et al.*, 2008).

VI. SIMULATION RESULTS

The simulated results using HSPICE in 180nm technology and 45nm technology. The supply voltages are 0.7v (45nm) and 1.8v (180nm) .

1-bit full adder when V_{DD}=0.7V at 45nm .

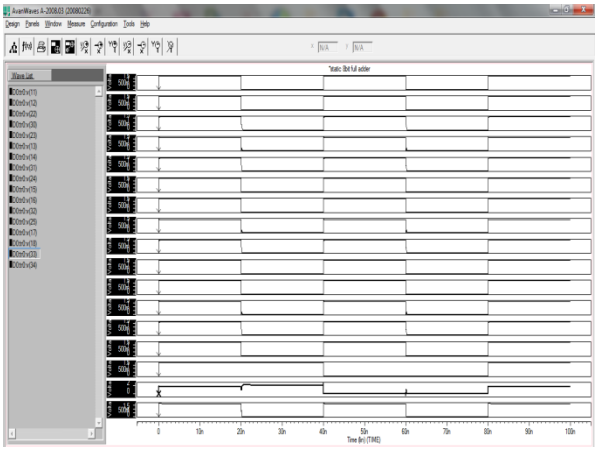

Fig.9. Simulation Waveform of 8T

The data analysis of the input and output such as A, B, C, sum and carry in 1-bit full adder and a standard 8-bit ripple-carry adder built as a cascade from eight 1-bit full-adders. C0 for carry-in, S0-S7 for sum, inputs are A0..A7 and B0..B7. The proposed 8T full adder of simulated results are shown here.

Parameter/ Full Adder	Voltage (V_{DD})	Average power (W)	Propagation delay(S)	Power delay product(J)
28T	1.8V	14.84E-05	12.04E-11	17.86 E-15
16T	1.8V	4.409E-05	0.342E-11	0.507 E-15
14T	1.8V	3.794E-05	1.871E-11	0.709 E-15
10T	1.8V	3.745E-05	1.173E-11	0.439 E-15
8T	1.8V	3.205E-05	0.895E-11	0.286 E-15

Table .1. Simulation Results Of 1-Bit Full Adder At 45nm Technology

VII. COMPARISION OF CMOS AND DTMOS FULL ADDERS

MOSFET devices are generally operated above threshold voltages but the devices can also exhibit control characteristics, even below the threshold voltages.

This region of operation of these devices may be called sub threshold operation. Basically principle of sub threshold logic is operating MOSFET in sub threshold region and using the leakage current in that region for switching action, there by significantly decreasing the power consumption.

The sub threshold circuit experience large delays and hence they cannot be used in high frequency applications. DTMOS ,where body is connected to gate. This technique provide high current device compare to CMOS circuits operated at lower voltages(i.e sub threshold). The leakage current produced by DTMOS circuits during OFF state is comparable with leakage currents of CMOS circuits.

Structure Of CMOS and DTMOS Configuration:

Typical schematic structures of CMOS and DTMOS are given in Figure 11.1(a), 11.1(b). In conventional NMOS circuit, Fig. 11.2(a), the substrate is normally connected to ground or lowest potential in the circuit and in PMOS circuits, the substrate is connected to supply voltage(VDD=0.3V) or the highest potential in the circuit. In DTMOS, Fig

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11.2 (b), the substrate is always kept at gate potential. Also, the voltage of each transistor substrate is dynamically adjusted depending on the gate voltage, causing the threshold voltage of the device to adjust dynamically . DTMOS devices are efficient because they function as dual threshold logic gates. When a DTMOS transistor is ON, its threshold is lowered increasing the current and decreasing propagation delay. Likewise when the transistor is OFF, the threshold is raised, reducing leakage current and minimizing power and energy dissipation. DTMOS is an excellent scheme to provide less delay with increased speed compared to traditional body biasing in the sub-threshold region.

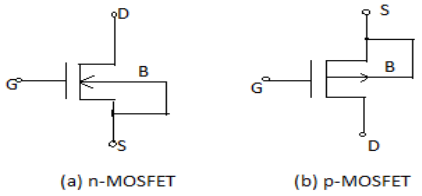

Fig 9- CMOS Structure

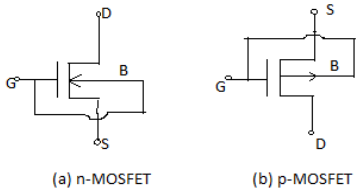

Fig 10- DTMOS Structure

VII. SIMULATION RESULTS

The simulated results using HSPICE in 45nm technology. The supply voltage is 0.3v (45nm) . The data analysis of the input and output such as A, B, C, sum and carry in 1-bit full adder and a standard 8-bit ripple-carry adder built as a cascade from eight 1-bit full-adders. C0 for carry-in, S0-S7 for sum, inputs are A0..A7 and B0..B7. The proposed 8T full adder of simulated results are shown here.

CONCLISIONS

The performance of digital VLSI applications depends largely on the characteristics of the full adder circuits employed in such systems. The novel full adder design proposed is composed of only eight transistors forming three multiplexers and one inverter to produce complementary carry signals (*C*out and out *C*) and summation signal (Sum). Comparing the proposed design with other existing adders in respect of power consumption, delay, and power delay product, the new design embodies a good many advantages. Power ,delay and power delay product(PDP) has also been improved. The comparison sshows that the implementation of the full adder would be better at 45nm technology as compared to 180nm technology. DTMOS has less delay and power delay product and more power compare to CMOS. DTMOS is an excellent scheme to provide less delay with increased speed compared to traditional body biasing in the sub-threshold region.sIn future work, the proposed design will be embedded into multiplier to demonstrate the performance in realistic applications.

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