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LUT OPTIMIZATION USING COMBINED APC-OMS TECHNIQUE

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Abstract: *Now a day's in signal processing multiplication is the most important arithmetic operation that uses look-up-table (LUT) as a memory for computations in arithmetic logic unit(ALU). LUT based computing is suitable for most of the digital-signal-processing (DSP) algorithms, which involves multiplication with a fixed set of coefficients.*

*The design of multiplier requires huge number of logic gates in DSP, thus it occupies more area, delay and consumes large amount power. This paper aims to develop APC (**Anti-symmetric product coding**) and OMS (**Odd Multiple Storage**) techniques for reducing the size of the LUT and power consumption of the multiplier. The APC and OMS module contains 4-line to 3- line address encoder, 3 to 8 line address decoder, control circuit, memory and barrel shifter modules. The performance of the designed LUT based multiplier With APC and OMS technique are verified in N-tap filter. The design can be simulated & synthesized by using Modelsim6.0.*

Keywords– ALU, APC, LUT, OMS.

I. INTRODUCTION

System-on-chip (SoC) is one of the leading theme in VLSI (very large scale integrated) technology. The thickness and complexity in VLSI circuit increases, the design costs for the emerging VLSI chip are also increased. Application specific domains are low power memories for mobile devices and consumer products [1]. For multimedia presentations, high-speed memories have much significance. The wide temperature memories finds application in self-propelled applications. In the design of biomedical instruments, high reliability memories were used which have high consistence [4].Traditional concept of memory as a standalone subsystem is getting changed and it is embedded within the logic components. Processor has been moved to memory or memory has been moved to processor, the relocations result in higher bandwidth, lower power consumption and less access-delay [9]. **memory-based computing** a class of dedicated systems, where the computational functions are performed by LUTs, instead of actual calculations close to human-like computing simple to design, and more regular compared with the multiply-accumulate structures have potential for high-throughput and reduced latency implementation involves less dynamic power consumption due to minimization of switching activities like inner-product computation using the distributed arithmetic. Direct implementation of constant multiplications [10], well-suited for digital filtering and orthogonal transformations for DSP implementation of fixed and adaptive FIR filters and transforms. The fig.1 shows a conventional LUT-based multiplier, here *A* is a fixed factor and *X* is considered as an input

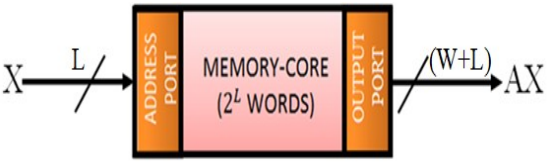

Fig 1: *Conventional LUT based multiplier.*

word to be multiplied with *A. let X* to be a positive binary number of word length *L*, there can be 2*L* possible values of input and consequently, there can be 2*L* possible values of product $C = A \cdot X$. Therefore, for memory-based multiplication an LUT of 2*L* words consisting of product values which are computed at first. Corresponding to all possible values of input is usually used. The product word $(A \cdot Xi)$ is stored at the location *Xi* for $0 \le Xi \le 2L - 1$, such that if an *L*-bit binary value of *Xi* is used as the address for the LUT, then the corresponding product value $(A \cdot Xi)$ is available as its output.

II. LOOKUP TABLE BASED MULTIPLIER

Multipliers method involves use of RAMs, ROMs or Look-Up Tables (LUTs) to store pre-computed values of coefficient operations. For fast accessing of values from the memory, LUT's are used for saving the computation complexity. In digital logic, an n-bit LUT can be implemented with a multiplexer whose select lines are the inputs of LUT and inputs are constant factors. In this project we are

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going to design multiplier based on Look up table by memory based computing. A LUT is a memory with one bit output that should have a truth table for each input combination generates a certain logic output. The input combination is referred to as an address.

Digital signal processing can be defined as the processing of digital information with minimum noise. The computation in digital systems increases with decreasing area. Therefore, new approaches are to be considered to optimize the size of memory along with power consumption. Multiplication, nothing but the repeated addition plays a vital role in signal processing. Memory based computations are more regular than the multiply and accumulate structures and offer many advantages.

This paper explains to optimizing lookup table in order to obtain Anti-Symmetric product coding scheme (APC) and Odd-Multiple Storage scheme (OMS). The proposed LUT design involves the combination of both the APC and the OMS schemes.

2.1 Anti-symmetric product coding scheme (APC)

APC technique is used to process the multiplication based on LUT. In this method, a 5-bit word($x_0 x_1 x_2 x_3 x_4$) is stored in a memory array shown in table 1. Conventional LUT based multiplier required 32 combinations of memory locations. The 2's compliment technique was adopted in APC will be reduces the size of the LUT by 50% i.e. for 5-bit input takes 16 memory locations shown in table 1. From the table the

Product word = 16A + x4 bit ×(APC word)

… (1)

In equation (1) when x4 = 1

Then the product word equals to 16A+APC word, otherwise 16A-APC word. The product value for X = (10000) corresponds to APC value "0000," which could be derived by resetting the LUT output, instead of storing that in the LUT.

Table I
Storage of values in APC

Input , X	Prodct values	Input ,X	Prodct values	Address $x_3'x_2'x_1'x_0'$	APC Words
00001	A	11111	31A	1111	15A
00010	2A	11110	30A	1110	14A
00011	3A	11101	29A	1101	13A
00100	4A	11100	28A	1100	12A
00101	5A	11011	27A	1011	11A
00110	6A	11010	26A	1010	10A
00111	7A	11001	25A	1001	9A
01000	8A	11000	24A	1000	8A
01001	9A	10111	23A	0111	7A
01010	10A	10110	22A	0110	6A
01011	11A	10101	21A	0101	5A
01100	12A	10100	20A	0100	4A
01101	13A	10011	19A	0011	3A
01110	14A	10010	18A	0010	2A
01111	15A	10001	17A	0001	1A
10000	16A	10000	16A	0000	0A

The APC module with 2's complement is shown in Fig 2.

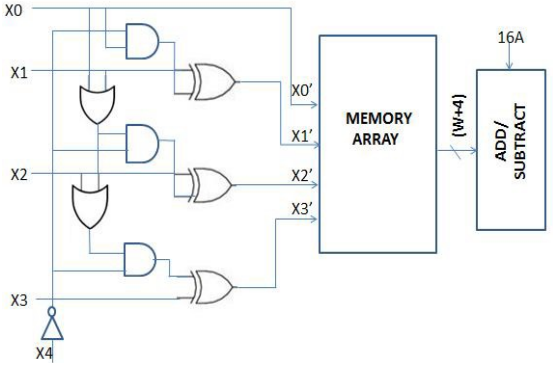

Fig 2: *LUT based multiplier using the APC technique for 5-bit input*

2.2 Odd Multiple Storage (OMS)

The OMS module consists of 4-to-3 address encoder, control circuit, memory array, NOR cell and barrel shifter are shown in figure 3. In this method, only odd multiple of the constant are to be stored in the LUT. Even multiples could be derived from the stored words.

The addressed APC values are re-addressed in OMS by using 4-to-3 Address Encoder is shown in table 2. A memory element (or) Memory array can be designed using a 3-to-8 decoder. Memory-unit of (2^*L*)/2 words of (*W*+*L*)-bit width is used to store the odd multiples of constant *A*. a barrel-shifter for

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producing a maximum of (L-1) left-shifts is used to derive all the even multiples of A. the L-bit input word is mapped to (L-1)-bit address of the LUT by an encoder [12]. The control-bits for barrel-shifter are derived by a control circuit to perform the necessary shifts of the LUT output. RESET signal is generated by the same control circuit to reset the LUT output when the X=0.

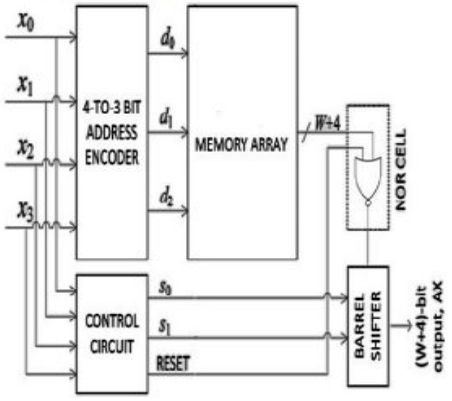

Fig 3: *block diagram of Odd multiple storage*

Table II
OMS based reduction scheme for LUT multiplier

APC word	Product word	APC word	Product word	OMS word	Product word
0000	0	1000	8A	0001	A
0001	A	1001	9A	0011	3A
0010	2A	1010	10A	0101	5A
0011	3A	1011	11A	0111	7A
0100	4A	1100	12A	1001	9A
0101	5A	1101	13A	1011	11A
0110	6A	1110	14A	1101	13A
0111	7A	1111	15A	1111	15A

In this approach 50% of the APC words are stored in LUT, so that by combining APC and OMS techniques ¾ product words of a multiplier are eliminated. Then the final size of the LUT is the ¼ of the actual size.

III. PROPOSED METHOD

The performance of the combined APC –OMS technique are evaluated in N-tap Filter. The structure of the N-tap Filter shown in fig 4. It requires N-1 delay elements and N number of multiplications. Here we assume N=4 so that for 4-tap Filter design takes 3 memory elements and 4 multiplications shown in fig 5. In this Filter block M replaced by APC-OMS based multiplier

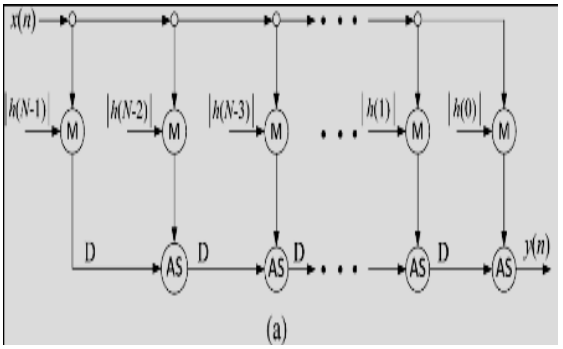

Fig 4: *Basic N-tap filter*

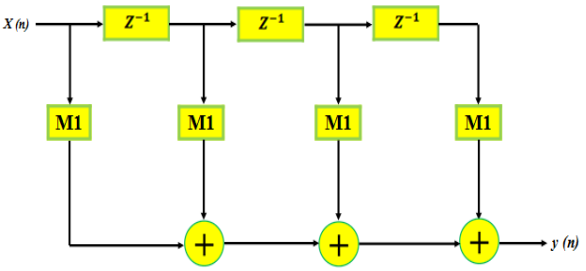

Fig 5: *4-tap filter*

IV. RESULTS AND ANALYSIS

The project modules are developed in Verilog HDL, and its simulation and synthesis result achieved through ModelSim-Altera 6.3g_p1 and ISE Design Suite 14.7. It is used to analyse the logic elements used for conventional LUT-based multiplier and APC-OMS based LUT multiplier. The fig 6(a) shows the simulation wave forms of an APC-OMS multiplier. We are forcing x input (01000) and acquires (00001000). The RTL schematic of multiplier shown in fig 6(b).

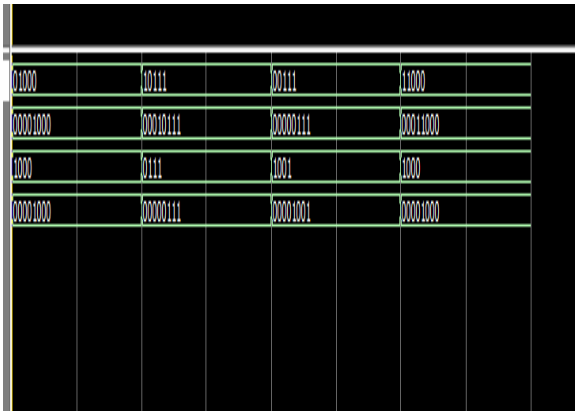

Fig 6(a): *APC&OMS output wave forms*

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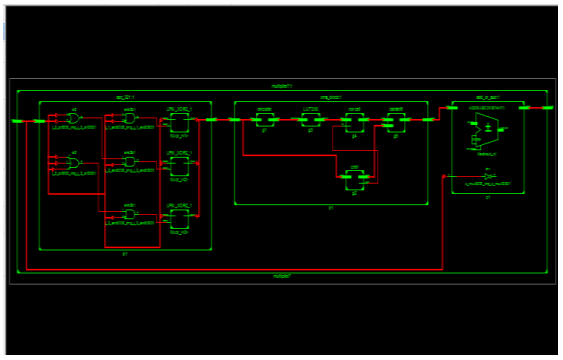

Fig 2: *RTL schematic of APC&OMS*

The fig 7(a) shows simulation wave form of a 4-tap Filter. We are forcing x input (00001) we get (00000100) for (0010) we get (00001000) similarly, N-input N-tap Filter generates 4*N value.

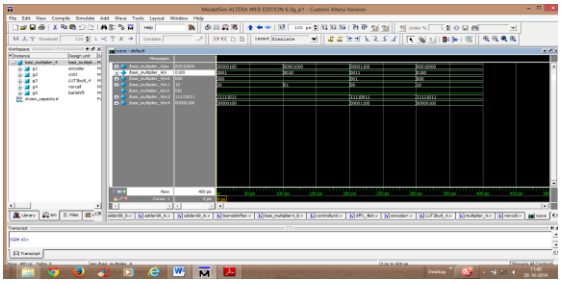

Fig 7(a): *4-tap filter simulation wave forms*

The RTL schematic of multiplier shown in fig 7(b).

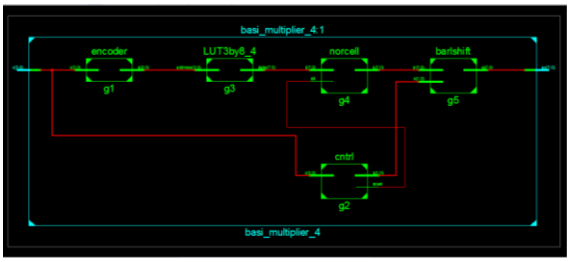

Fig 7(b): *4-tap filter RTL diagram*

The timing analysis of 4-tap Filter are summarised in table 3.

Table III
Timing analysis of 4-tap Filter

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Timing Detail:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 4 / 4
-------------------------------------------------------------------------
Delay:               4.632ns (Levels of Logic = 2)
  Source:            x<3> (PAD)
  Destination:       ax<5> (PAD)

  Data Path: x<3> to ax<5>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.106   0.357  x_3_IBUF (x_3_IBUF)
     OBUF:I->O                 3.169          ax_5_OBUF (ax<5>)
    ----------------------------------------
    Total                      4.632ns (4.275ns logic, 0.357ns route)
                                       (92.3% logic, 7.7% route)

=========================================================================
```

V. CONCLUSION

Memory-technology is growing quite fast and efficient memories for different applications are emerging over the years. LUT could be designed for efficient evaluation of non-linear functions, like sinusoidal and hyperbolic functions, logarithms and multiple precision arithmetic. The performance of the system can be improved when the Memory elements are embedded directly into the structure of the microprocessor or integrated in the functional elements of dedicated processors.

In this paper LUT based conventional multiplier was design by using APC-OMS methods. With these technology ¾ of the look up table size is reduced. Performance of the multiplier was tested in 4-tap Filter. This type designs are well suited for memory based applications like DSP computations and Microprocessors.

VIII. REFERENCES

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