

Fault-Tolerant Multiple Task Migration in Mesh NoC's over virtual Point-to-Point connections

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Abstract

Multiple task migration is a process in network on chips are able to transfer the data from one cluster to another cluster, while transfer the data from one cluster to another cluster message latency, migration latency, Network latency and power consumption are problem encountered. New techniques are introduced like hybrid scheme, virtual point to point Connections (VIPs) has been introduced that dedicates low power and low latency heavy communication flow created by multiple task migration mechanism. The proposed system scheme reduces total message latency, total migration latency, total network latency, power saving is achieved compared to the previously proposed task migration strategy for mesh multicomputer. Analyzing the results show that the proposed scheme reduces message latency by 16% and migration latency by 15%, while 13% power savings can be achieved. And also, a fault-tolerant NoC architecture designed in VHDL and synthesized using Xilinx ISE is presented which not only is able to recover from single permanent router failure, but also improves the average response time of the system.

Keywords:- MPSoCs, NoCs, Task migration, Virtual point-to multipoint connection, Power, Performance, Fault-Tolerant Design.

I. INTRODUCTION

In earlier days point to point links, star based approach and shared buses which increases large number of IP cores on the same chip makes the design of communication architectures involves major problems in SoCs. In this earlier approach increases vast area and

also poor scalability are the major drawbacks while connecting point to point communication links in SoCs, Applicability of shared buses and star based communication to future many core SoCs are also under question due to unpredictability of latency and enhancement of power. [3]. To reduce the area and increases the efficiency of packet switched network on chips are preciously performed and computes in present generations of multiprocessor systems on chips. Experimental results of various on-chip interconnection design shows in [4] where the authors compare various on-chip interconnections and NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs. Networks-on-Chip (NoCs) have emerged as the best alternative to provide high performance in communication for futures Systems-on-Chip (SoCs) with dozens of cores integrated on a single silicon die.

Network on chip is an emerging paradigm for communications with in large VLSI systems implemented on single silicon chip. In NOC systems, modules such as processor cores, memories and specialized IP blocks exchange data using a network as a "public transportation" sub-systems for the information traffic. A NOC establishes from multiple point to point data links interconnected by switches, such that messages can releases from any source module to destination module over several links, by making routing decisions at switches. Generally heterogeneous MPSOC'S [5] are under progress in applications of multimedia and networking such sorts of operation mechanism created by the dynamic work load.

In fact heterogeneous MPSOC'S design faces major challenges like communication and computation latency for achieving better reliability and while introduce a deadlock free routing algorithm in NOC's architecture which minimized communication energy, simultaneously communication system should assists to satisfy the specific design constrains via bandwidth reservation. In a single silicon die consists of number of resources that have to communicate makes the use of interconnection systems based on shared buses are not convenient, a simple technique is used to resolve the problem of on-chip communication is to use a Network on chip communication. This is t he best way to resolves that problem of on chip interconnections.

Task migration in mesh NOC's manipulate free from the congestion and load balancing as major objective. On-chip communication supports hundreds of cores in single silicon wafer. Source routing has one major drawback of over head for storing the path information in header of every packet. If the size of the network increases the performance will reduces [6]. Junction based routing can resolves such kind of problems and it has two important issues related to junction based routing, such as numbers and position of the junctions and path computation for efficient dead lock free routing, while increasing the path length reduces the number of junctions.

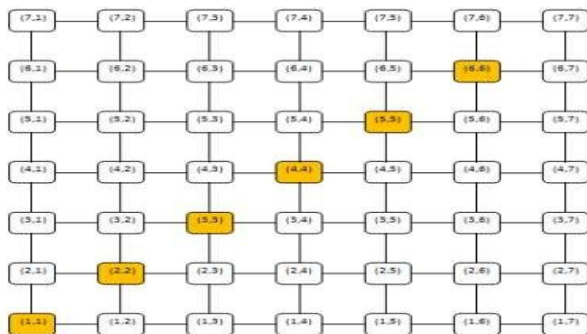


Fig 1. Negative-First Routing Algorithm

The illustration of different routing algorithms about path computations for Mesh topology NOC with junctions fig. 1 shows that junction configurations for North-Last Routing Algorithm. Applying North-last routing algorithm, minimum number of junctions is 9. we define junction ratio as follows:

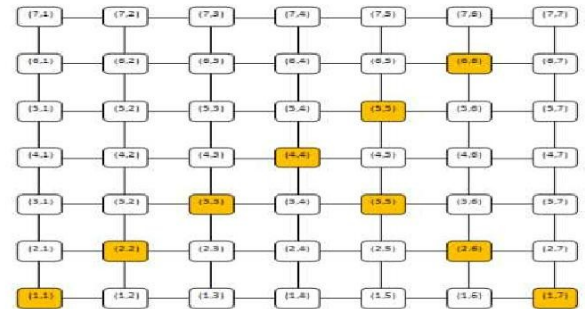


Fig 2. 7x7 Task migration network using North-Last routing algorithm with hop count Limit of 7

$$NJ/NN = \text{Number of junctions/number of Nodes} = 9/49 = 0.18.$$

Figure 2 shows the only possible configuration for this case, the number of available paths are generally reduced when using JBR.

Figure 3 shows Junction Configurations for Other Kinds of Routing Algorithms such as West-First, XY and Negative-first routing algorithms are applied.

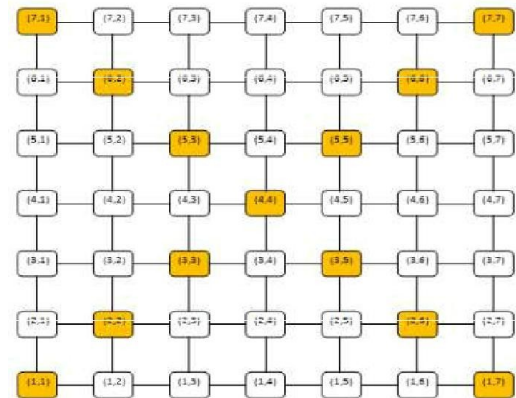


Fig 3. XY Routing Algorithms

For instance, applying XY routing algorithm, number of required junctions is 12. Figure-2, 3, shows the only possible configurations for these routing algorithms used.

II. RELATED WORK

In earlier days various techniques has been introduced in mesh multi computers such as task migration and multiple task migration [7]. In this research paper, three types of migration was introduced, such as first migration called as Diagonal scheme major objective is to explore all disjoint paths in one phase to migrate task based on XY routing, second migration called Gather-routing-scattering algorithm express about to optimize the number of task migration paths finite number of nodes in the source sub mesh and send them to the corresponding cores in the destination sub mesh which will then scatter the tasks to their final destinations. The above two migration schemes are combined called hybrid scheme.

The first platform resource is to require fast and efficiency on NOC'S and second thing on NOC's resources reallocation taken place in case of mapping failure and changes by the user requirement. In this approach may concerns only performance while neglecting power consumption. The word task migration was recently addressed, the main theme concentrate on the mechanism of starting mechanism on the source core and resuming the task on the destination core.

In paper [4], multi processor systems on chips which showing the interest in migration technique and also arises both in research and product development. The main thing of this paper deals about process migration only and don't consider performance and power consumption over heads of migrations. We are mainly concentrating to minimize the power consumption and improve overall network performance while overhead caused by migrating tasks when they are transferring from source core to destination core.

Many algorithms in this area have been proposed which follow their own optimization aims. The main problem with the fault-tolerant routings is that if a router fails, considering

mesh architecture, recovery cannot be accomplished only by rerouting. In addition, hardware redundancy is inevitable in order to repair the lost connection to the network of the core directly connected to the failed router.

A fault-tolerant mesh-based NoC architecture with the ability of recovering from single permanent failure is presented in [13]. This method adds a redundant link between each core and one of its neighboring routers, resulting in significant improvement in reliability while has little impact on performance. In this architecture, only one spare router should be selected among all possible alternative ones. It also shows that mapping algorithm has a great impact on mentioned parameters. Following this concept, in this paper, a hardware and performance aware design for the fault tolerant NoC architecture is presented which takes in to account the specific application mapped onto mesh topology.

III. PREREQUISITES OF APPLICATION SPECIFIC NOC DESIGN

A. Problem Formulation

In general 2D Mesh multi computer consists of local memory, processor and router and some input and output function. The architecture of the 2D meshes multicomputer system which provides wormhole routing in all-port communication. In general system level design of 2D mesh multicomputer depends up on graph-based design architecture. In Mesh NOC's interconnects can be represented as some parameters like size, router, bandwidth and buffer.

**Size consists of (X and Y)
dimension parameters Router
consists of (source, destination)
Bandwidth (BW)
Buffer (B)**

The main objective is to reduce the overhead of migration to the normal communication of other IP cores.

In a network on chip while doing migration from one core to another; it incorporates migration time and power consumption, simultaneously increases the ultimate network. In a network on chip while doing migration from one core to another; it incorporates migration time and power consumption, simultaneously increases the ultimate network

B. Routing Algorithm

The routing algorithm determines the path that each packet follows between a source-destination pair. Routing algorithms noticeably affect the cost and performance of NoC parameters i.e. area, power consumption and average message latency. Due to determined sources and destinations in application-specific NoC, minimum-distance routing algorithms are mostly considered in this area which is computed off-line and admissible paths stored into the routing tables.

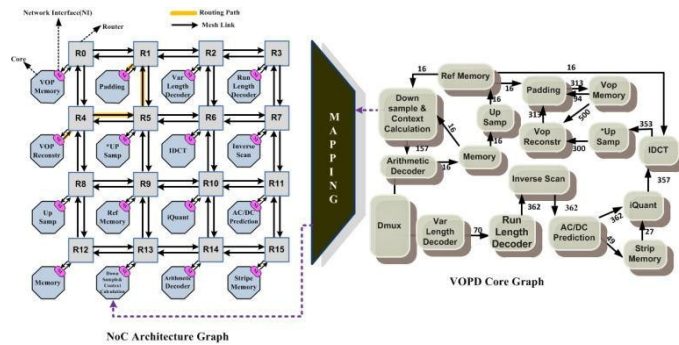


Fig.4: Mapping problem concepts

In general, every routing algorithm should include deadlock freedom feature [6]. So channel dependency graphs (CDG) is used to avoid any possible deadlocks. The CDG is a directed graph with the network channels as the vertices and the direct dependencies between the two channels as the edges. Using this method guarantees that routing algorithm is still deadlock-free. A fault tolerant mesh based NoC architecture with the ability of recovering from single permanent failure. This method adds a redundant link between each core and one of its neighboring routers, resulting in significant improvement in reliability.

IV. THE PROPOSED APPROACH

The proposed low-power and low-latency task migration strategy is based on hybrid scheme algorithm [8] and uses VIPs for the paths involved in task migration to reduce the average migration latency (AML) and hence the total mean network latency and power consumption.

In this approach we are mainly concentrating on power consumption, network latency, message latency and migration latency. The process of multiple task migration is used to transfer the data from one core to another core, so it utilizes some mechanism that is hybrid scheme. In the hybrid scheme the first process is used to collect each sub task in each sub core and each row or column; hence it is congestion free. Using this technique number multiple task migration flows are reduced.

Gathering step obtaining derivation of time calculated as

$$T_{gather} = \max([\log_e p], [\log_e q]) * t_s + \max([\log_2 p^{m^2}], [\log_2 q^{m^2}]) * t_x.$$

t_s = startup latency

t_x = link between the neighboring nodes

m = number of flits.

Diagonal step obtaining derivation of time calculated as

$$T_{diagonal} = \max([W/p], [H/q]) * (t_s + \max(m p, m q) * t_x)$$

Finally scattering scheme obtaining derivation of time calculated as

$T_{scatter} = T_{gather}$ here it obtains the time taken by the scatter is square of that time taken by the gathering process.

Total transmission time (hybrid time) is combined of all above parameters such gathering time, diagonal time and scatter time.

$$T_{hybrid} = T_{gather} + T_{diagonal} + T_{scatter}$$

In the mesh-based architecture which is the simplest and most dominant topology for today's regular network on chips, each core is connected to a single router as depicted in Fig.4.

As shown in Fig. 5, each router consists of five identical input/output ports and each port is a bidirectional link with a circular FIFO on its input side. In order to recover the inaccessibility of the core, a fault-tolerant architecture which each core is connected to two routers i.e. main and spare have been proposed shown in Fig. 6.

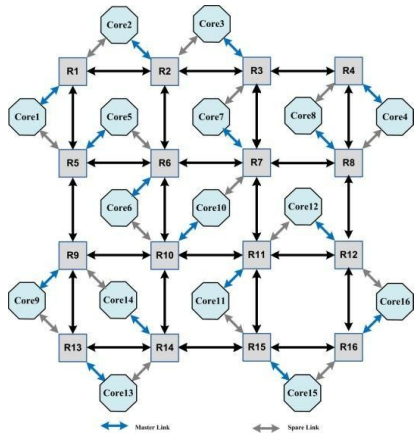


Fig.5: The proposed architecture in [9]

Adding one port to all non-edge routers in this architecture leads to a great waste of hardware. However, in this paper the provided path diversities between adjacent routers are used to improve performance of the system and a new component called Link Interface (LI) instead of router port is developed to reduce hardware overhead. According to the mentioned architecture shown in Fig.6, after mapping an application onto mesh topology, an efficient spare router selection should be considered to find the best spare router for any core.

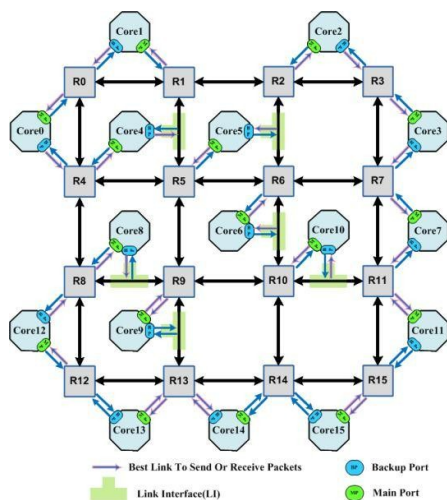


Fig.6: The proposed fault-tolerant architecture in this paper

In this architecture, if both main and spare routers are working properly, the best (minimum-distance) paths to send and receive packets are derived from path diversities and if main (spare) is faulty, spare (main) will be responsible to transfer packets through rerouting paths.

V. EXPERIMENTAL RESULTS

In this section, we evaluate the proposed Multiple task migration schemes using *Gathering-Routing-Scattering* algorithm [6]. All considered multiple task migration strategies and the proposed technique are implemented on an NoC architecture simulated by Xmutator [2]. Simulation experiments are performed for a 128-bit wide system. Moreover, the process feature size and working frequency of the NoC is set to 65nm and 280 MHz.

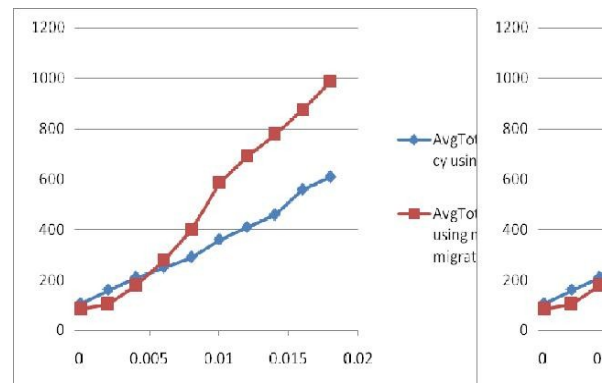


Fig. 5 Average message latency

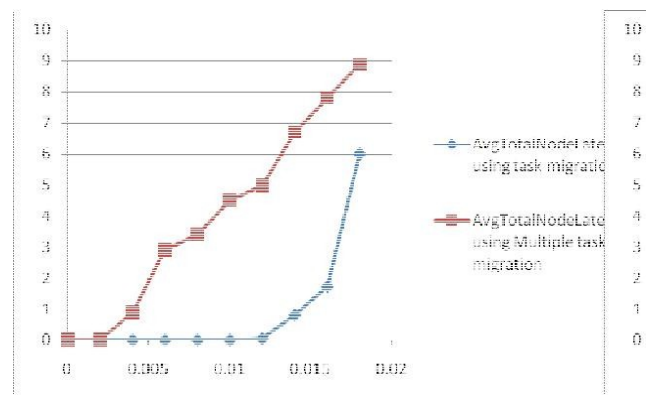


Fig. 7 Average total node latency

In order to compare the average response time and hardware cost of the reliable architecture and traditional mesh, they have been designed in VHDL and synthesized using Xilinx ISE. It should be pointed that it actually is a great achievement to develop a fault-tolerant NoC design which also has better performance. To explain in details, when all routers are correctly operating, new architecture improves the average response time by 41% comparing to mesh and it also improves the response time by 10%. Conclusively, we observe that the proposed approach allows to decrease the response time of system by 27% and tolerate permanent failure of each single router (Fig. 9).

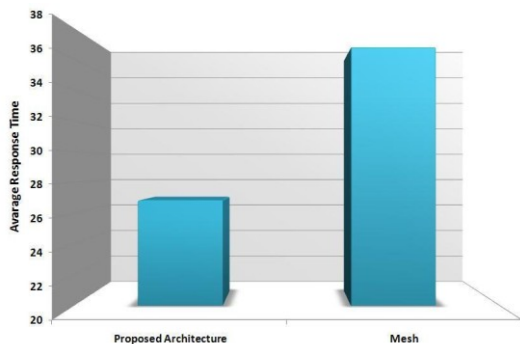


Fig.9: Comparing proposed architecture with mesh in terms of average response time (all situations are considered)

VI. CONCLUSION

In this paper, we proposed multiple task migration schemes in mesh-based NoCs based on low-latency, low-power virtual point-to-point (VIPs) connections and a new fault-tolerant application-specific NoC was proposed which is able to tolerate one router failure and guarantees the 100% packet delivery. Experimental results revealed that the proposed scheme could improve over earlier technology. Link Interface as a solution for reducing hardware redundancy was suggested and synthesized results demonstrated that each new router port is almost equal to three Link Interfaces in terms of hardware overhead. In future we can expect some more enhancement using virtual point-to-multi point connection in

the presence of super scalar methodology which will provides low latency and low power heavy communication flow created by multiple task migration mechanism.

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