

# VHDL IMPLEMENTATION OF $\frac{\pi}{4}$ QPSK MODULATOR & DEMODULATOR

Karri Tejaswi<sup>1</sup>, Prof.Tadichetti Ram Babu<sup>2</sup>, Asst.prof.Subrahmanyam Sayila  
M.Tech, RamaChandra College of Engineering,Vatluru(v),Eluru,India

*Professor, Department of E.C.E* , RamaChandra College of Engineering,Vatluru(v),Eluru,India  
Asst.prof,Department of E.C.E,ACE Engineering college,Ankushapur(v),Ghatkesar(M) Hyderabad,India

## ABSTRACT

With digital techniques, extremely low error rates producing high signal reliability are possible in communication systems. Digital circuits are also more reliable and can be reproduced at a lower cost than analog circuits. The digital technique based communication systems are highly reconfigurable and programmable. This is an essential and desirable property in latest mobile technologies. $\pi/4$  QPSK is widely used modulation scheme in satellite radio applications. Maximum phase transition of  $\pi/4$  QPSK is limited to  $\pm 135^\circ$  as compared to  $180^\circ$  for QPSK and  $90^\circ$  for OQPSK. Hence, the  $\pi/4$  QPSK preserves the constant envelope property better than the band limited QPSK but is more susceptible to envelope variations than OQPSK. However,  $\pi/4$  QPSK has the advantage over OQPSK in that, it can be differentially detected. A stream of identical 1's or 0's will always produce a phase change.

In this paper the digital implementation of  $\pi/4$  QPSK modulator and demodulator is attempted. Complete modulator and demodulator units are modeled using VHDL, and functionally verified using Modelsim simulation tools. The code is synthesized fully onto Xilinx. The Modulator consists of various communication modules like phase calculator, I-Q mapper, frequency synthesizer, clock generators, and COS-LUT. The demodulator consists of modules COS-LUT, Negative SIN-LUT, digital multiplier, integrate & dump circuit and base band

differential detector. These digital modules are implemented as different modules and used as components in top level entities.

## INTRODUCTION

Modulation is the process of facilitating the transfer of information over a medium .the process of converting information so that it can be successfully sent through a medium is called modulation there are three different types of digital modulation techniques those are amplitude shift keying (ASK) frequency shift keying (FSK) phase shift keying (PSK) all of these techniques vary a parameter of a sinusoid to represent the information which we wish to send. In ASK, the amplitude of the carrier is changed in response to information and all else is kept fixed. Bit 1 is transmitted by a carrier of one particular amplitude to transmit 0, we change the amplitude keeping the frequency constant. In FSK, we change the frequency in response to information. One particular frequency for a 1 and another frequency for a 0. In PSK, we change the phase of the sinusoidal carrier to indicate information

Phase shift represents the change in the state of the information. ASK techniques are more susceptible to the effects of non-linear devices which compress and distort signal amplitude. To avoid such distortion, the system must be operated in the wire based

signaling. Basically in QPSK, it appends two bits together and form a *symbol*. The symbol can have any one of the four possible values corresponding to the two-bit sequences 00,01,10,11. So, this gives four distinct signals for transmission. At receiver each signal represents one symbol and correspondingly two bits. The modulation scheme is characterized by the fact that the information carried by the transmitted wave is contained in the phase. In QPSK, the phase of the carrier takes on one of four equally spaced values, such as  $\pi/4$ ,  $3\pi/4$ ,  $5\pi/4$  and  $7\pi/4$ . And hence one of the four possible waveforms is transmitted during each signaling interval. OQPSK signaling is similar to QPSK signaling except for time alignment of the even and odd bit streams.

In QPSK signaling the bit transitions of the even and the odd bit streams occur at the same time instance, but in OQPSK signaling, the even and odd bit streams,  $m_i(t)$  and  $m_q(t)$ , are offset in their relative alignment by one bit period (half symbol period).when QPSK signals are pulse shaped, they loose the constant envelope property. Phase shift of  $\pi$  radians can cause the signal envelope to pass through the origin.

## 1. DIFFERENT MODULATION TECHNIQUES

### A.Binary Phase Shift Keying

Binary Phase shift keying is a digital modulation scheme that conveys data by changing, or modulating, the phase of a reference carrier signal. Any digital modulation scheme uses a finite number of distinct signals to represent digital data. PSK [5] uses a finite number of phases, each assigned a unique pattern of binary bits. Usually, each phase encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase .

Binary PSK requires 3 db less of signal to noise ratio than QPSK to achieve the same BER. This outcome will hold true only if we consider BER in terms of SNR per carrier. In terms of signal to noise ratio per bit the BER is same for both QPSK and BPSK [4]

### B. Quadrature phase shift keying

(QPSK) is a form of phase shift keying in which two bits are modulated at once, selecting one of four possible carrier phase shifts (0, 90, 180, or 270 degrees). QPSK allows the signal to carry twice as much information as ordinary PSK using the same bandwidth. QPSK is used for satellite transmission of mpeg2 video, cable modems, videoconferencing, cellular phone systems, and other forms of digital communication over an RF carrier [3].

Quadrature phase-shift keying (QPSK) is a complex modulation format that has been the subject of several recent coherent detection real-time transmission experiments. The major challenge of coherent QPSK transmission is the combination of general noise reduction combined with phase noise tracking, especially when standard distributed feedback (dfb) lasers are employed [1].

### C.Offset QPSK (OQPSK)

OQPSK is a modified form of QPSK where the bit waveforms on i and q channels are offset or shifted in phase from each other by one-half of a bit time. DPSK is an alternative form of digital modulation where the binary input information is contained in the difference between two successive signaling elements rather than the absolute phase with DPSK, it is not necessary to recover the a phase-coherent carrier. Instead, a received signaling element is delayed by one signaling-element time slot and then compared with the next received signaling element [ref 14].

### III. EXISTING METHOD

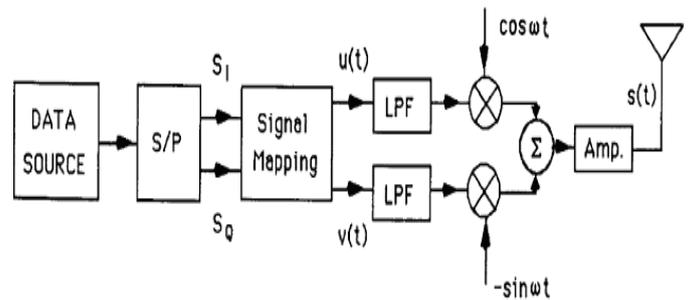
#### A. ANALOG IMPLEMENTATION OF $\pi/4$ QPSK

One of the great advantages of the proposed modulation scheme is that design and development can start now, there is no need of technology transfer from a single source or the need to prove a modulation scheme. A complete description of  $\pi/4$  DQPSK is given. The detail here is sufficient to enable the design and development of systems. It is clearly a modulation scheme that is bandwidth efficient and enables good performance at low cost, hence its selection for the Japanese digital cordless telephone standard.

Ideally with a wireless product, there is freedom for the manufacturer to balance cost versus performance,  $\pi/4$  DQPSK has this ability, one can select to develop the 'ideal' system or a lower cost system with very reasonable performance.

The higher data rate inputs have been focused on the use of non linear amplifiers. However this places serious constraints on the data rate achieved or degrades the performance of the radio link. Technically the only route to achieve higher data rates without significant loss of performance is to follow the route of non constant amplitude envelope modulation. One advantage of  $\pi/4$  DQPSK is that 'reasonably linear' transmit amplifiers can be used that have acceptable efficiency, not as poor as those assumed to date.

This paper proposes 1.5Mb/sec, not because this is the limit, but because of system implementation issues. This note is a general discussion as to why this modulation scheme should be selected, additional technical information will be presented in Vancouver.



- The input bit stream is partitioned by serial to parallel converter into two parallel data streams of  $m_{I,k}$  and  $m_{Q,k}$ , each with a symbol rate equal to half that of the incoming bit rate.
- The  $K^{\text{th}}$  in-phase and quadrature pulses,  $I_k$  and  $Q_k$  are produced at the output of the signal mapping circuit over time  $KT \leq t \leq (K+1)T$ , and are determined by their previous values,  $I_{k-1}$  and  $Q_{k-1}$ , as well as  $\theta_k$ , which itself is a function of  $\phi_k$ , which is a function of the current input symbols  $m_{I,k}$  and  $m_{Q,k}$ .  $I_k$  and  $Q_k$  represent rectangular pulses over one symbol duration having amplitudes given by:
  - $I_k = \cos\theta_k$
  - $Q_k = \sin\theta_k$
  - $\theta_k = \theta_{k-1} + \phi_k$
  -

Information Bits, $m_{I,k}, m_{Q,k}$	Phase Shift $\phi_k$
11	$\pi/4$
01	$3\pi/4$
00	$-\pi/4$
10	$-3\pi/4$

The in phase and quadrature bit streams  $I_k$  and  $Q_k$  are then separately multiplied by two carriers, which are in quadrature with one another to produce  $\pi/4$  QPSK waveforms given by :

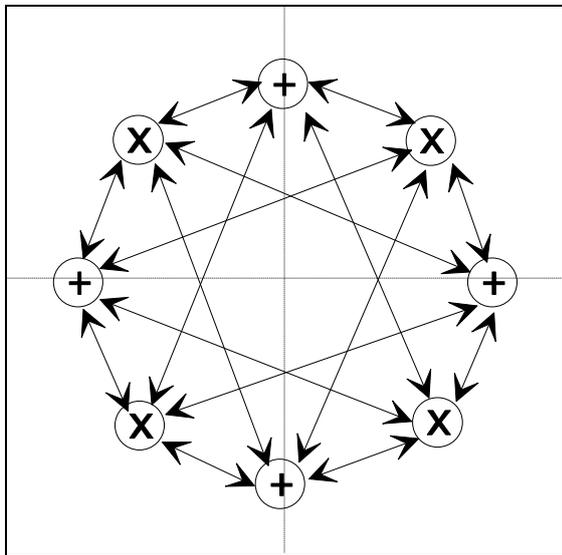
$$\pi/4 \text{ QPSK } (t) = I(t) \text{ Cos}w_c t - Q(t) \text{ Sin}w_c t$$


Figure 2.2 Constellation of  $\pi/4$  QPSK signal.

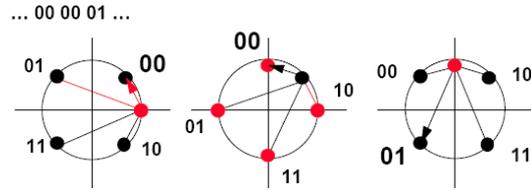


Figure 2.2 Phase transition from current symbol to next symbol in  $\pi/4$  QPSK.

## 2. Block diagram of demodulator

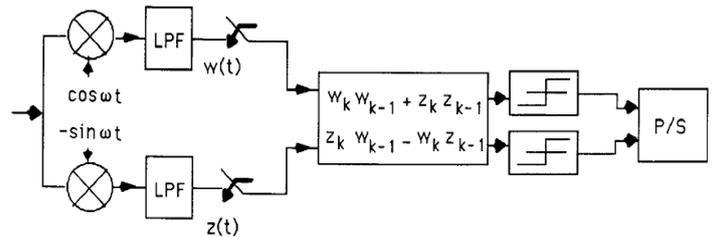
Incoming  $\pi/4$  QPSK signal is quadrature demodulated using two oscillator signals that have the same frequency as the un-modulated carrier at the transmitter, but not necessarily the same phase.

If  $\phi_k = \tan^{-1} (Q_k/I_k)$  is the phase of the carrier due to the Kth data bit, the output  $w_k$  and the  $Z_k$  from the two low pass filters can be expressed as:

$$w_k = \text{Cos}(\phi_k-r)$$

$$Z_k = \text{Sin}(\phi_k-r)$$

Where  $r$  is the phase shift due to noise, propagation and interference. The phase  $r$  is



assumed to change much slower than  $\phi_k$ , so it is essentially a constant.

The two sequences  $w_k$  and  $Z_k$  are passed through a differential decoder which operates on the following rule:

$$X_k = w_k w_{k-1} + Z_k Z_{k-1}$$

$$Y_k = Z_k w_{k-1} - w_k Z_{k-1}$$

$$X_k = \text{Cos}(\phi_k-r) \text{ Cos}(\phi_{(k-1)-r}) + \text{Sin}(\phi_k-r) \text{ Sin}(\phi_{(k-1)-r})$$

$$= \text{Cos}(\phi_k - \phi_{(k-1)})$$

$$Y_k = \text{Sin}(\phi_k - r) \text{Cos}(\phi_{(k-1)} - r) + \text{Cos}(\phi_k - r) \text{Sin}(\phi_{(k-1)} - r)$$

$$= \text{Sin}(\phi_k - \phi_{(k-1)})$$

The output of the differential encoder is applied to the decision circuit which uses gray code to determine:

$$S_I = 1, \quad \text{if } X_k > 0$$

$$S_I = 0, \quad \text{if } X_k < 0$$

$$S_Q = 1, \quad \text{if } Y_k > 0$$

$$S_Q = 0, \quad \text{if } Y_k < 0$$

Where  $S_I$  and  $S_Q$  are the detected bits in the in-phase and quadrature arms.

#### Advantages and Disadvantages of Analog $\pi/4$ QPSK:

- There need not be phase synchronization between the modulator and demodulator carrier signals. But the carrier frequency of demodulator must be same as the transmitter carrier frequency, and it should not drift.
- Differential detection is often employed due to ease of hardware implementation.
- Differential detection offers a lower error floor, since it does not rely on phase synchronization.

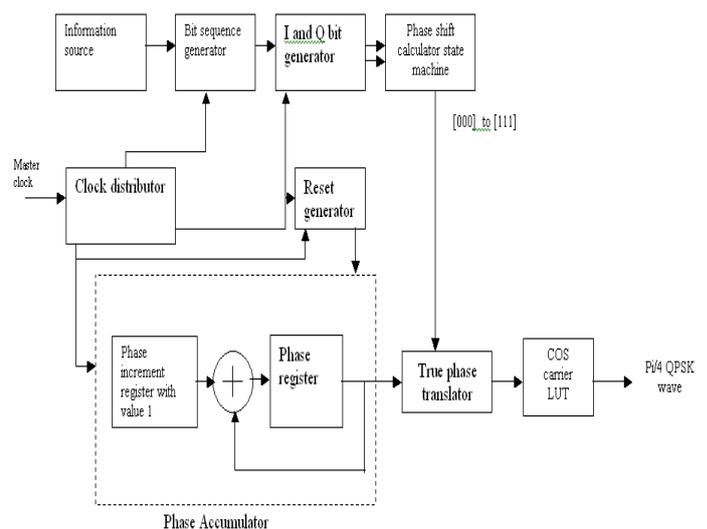
## IV. PROPOSED METHOD

### A. DIGITAL MODULATOR

The  $\pi/4$  QPSK modulation scheme is a modulation scheme that has combined a conventional QPSK modulation scheme with an offset QPSK (OQPSK) scheme, and it is mainly used in North America mobile communication system is-54 and Japan digital cellular system JDC.

Since the conventional  $\pi/4$  QPSK modulation scheme was realized with analog Quadrature modulators, distortion and drift were incurred in signal phase, direct-current offset and gain, thus deteriorating the performance of the whole system. In modern communication systems, usage of digital techniques has reported, higher performance. The full digital implementation of  $\pi/4$  QPSK, can achieve better performance over corresponding analog implementation.

Modulator consists of different blocks such as bit sequence generator, I and Q bit Generator, phase shift calculator, clock distributor reset generator, phase accumulator ...etc

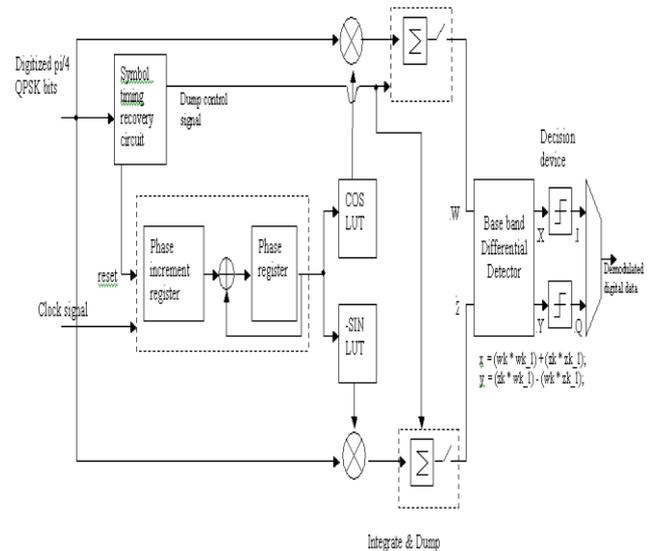


## B. DIGITAL PI/4 QPSK DEMODULATOR

The block diagram of digital pi/4 QPSK demodulator (according to base band differential detector principle), which will be implemented in this project, is given below

Demodulation is the act of extracting the original information-bearing signal from a modulated carrier wave. A demodulator is an electronic circuit (or computer program in a software defined radio) that is used to recover the information content from the modulated carrier wave. Following figure represents the demodulator diagram. it consists of different blocks such as symbol timing recovery circuit, phase accumulator, baseband differential detector ..etcThe demodulator, which is designed specifically for the symbol-set used by the modulator, determines the phase of the received signal and maps it back to the symbol it represents, thus recovering the original data. This requires the receiver to be able to compare the phase of the received signal to a reference signal. Alternatively, instead of using the bit patterns to set the phase of the wave, it can instead be used to change it by a specified amount. The demodulator then determines the changes in the phase of the received signal rather than the phase itself. Since this scheme depends on the difference between successive phases, it is termed differential phase-shift keying (DPSK). DPSK can be significantly simpler to implement than ordinary PSK since there is no need for the demodulator to have a copy of the reference

signal to determine the exact phase of the received signal (it is a non-coherent scheme).



## V. SIMULATION RESULTS

### A. TOP LEVEL ENVIRONMENT & SIMULATION RESULTS

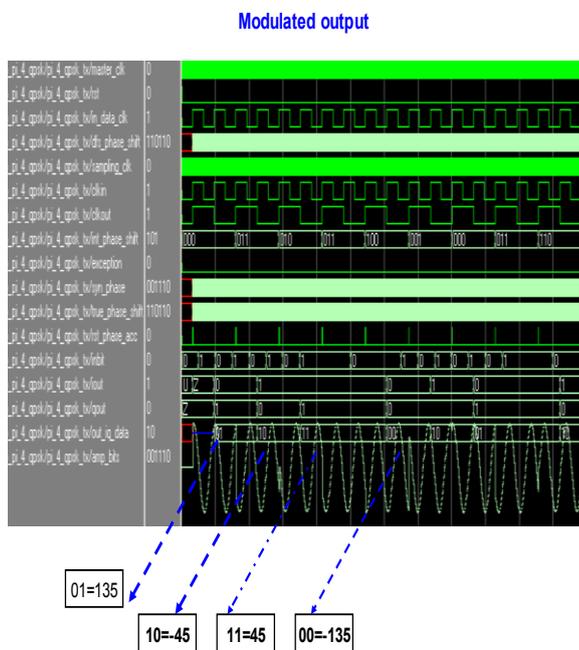
This chapter explains the top level overview of the environment and simulation results. The following is the sequence of operations followed to verify the design

- VHDL code is written for every module in digital modulator and demodulator, Simulation of these modules is done in Modelsim.
- Test benches are written to give a required input to each block and check the outputs for their correctness.
- The simulation of each module is shown for both modulator and

demodulator and also for top module of Modulator and Demodulator :

• **Modulated output of Pi/4 QPSK**

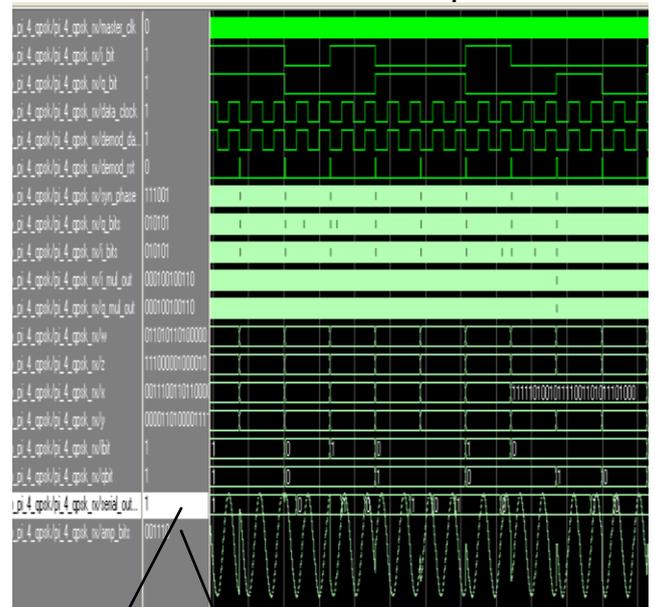
This shows that the output of the Modulator for the given input values it generates output for the respective symbol combinations and also it shows that output in analog signal for the checking of the output which is to be shifted based on the input bit combinations



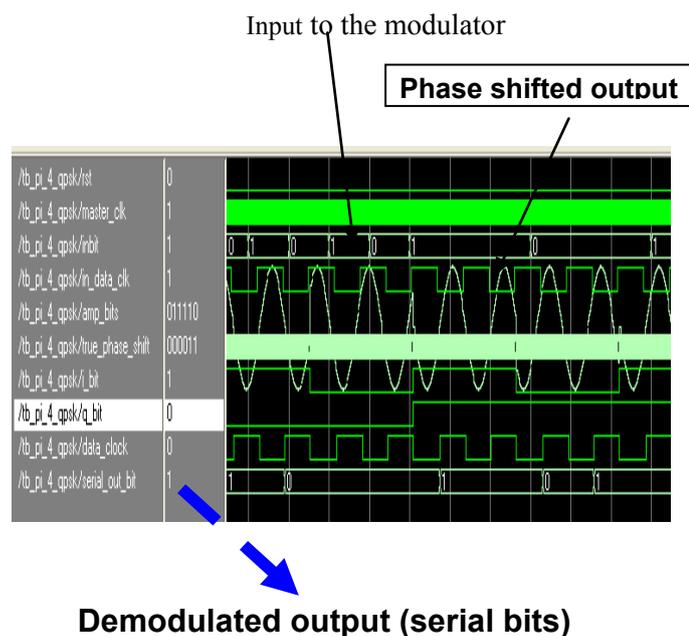
**Demodulated output of Pi/4 QPSK**

This shows that the output of the Demodulator, the output of the modulator is given to the demodulator as input to reconstruct the input. Here for the clarity I am showing the input in analog only (but originally it is also a digital signal only).

The demodulated output is equal to the input of the modulator.



• **Top Module (Modulated and Demodulated) output**



- This is the output of the top module, here total 6 bit delay was introduced. After this delay we can see that modulator input bits and demodulator output bits are same.

### CONCLUSION

The proposed project QPSK modulator and demodulator units are designed in digital. In  $\pi/4$  QPSK modulator, signalling points of the modulator, are selected from two QPSK constellations which are shifted by  $\pi/4$  with respect to each other. Switching between two constellations, every successive bit ensures that there is at least a phase shift which is an integer multiple of  $\pi/4$  radians between successive symbols. This ensures that there is a phase transition for every symbol. In this project  $\pi/4$  QPSK modulator, IQ bit is converted into 3 bit equivalent using phase shift calculator which gives total 8 phases and the modulated output is stored in a ROM based LUT. Maximum phase transition is limited to 135degrees to 45 degrees as compared to 180 degrees for QPSK and 90 degrees to OQPSK. In the Demodulator block Base band differential detection technique is used because ease of hardware implementation and it offers low bit error rate and it has a very good phase synchronization. It Can be detected non-coherently, thus greatly simplifies the receiver.  $\pi/4$  QPSK complete modulator and demodulator units were modeled using VHDL. Functionally verified using Modelsim simulation tools. The code is synthesized fully onto Xilinx FPGAs, and the output is also verified in analog form which is very much easy to verify the phase shifts than in digital form (0's and 1's).

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