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Design and Implementation of Reversible Vedic Multiplier for High Speed Low Power Operations

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Abstract— Number style is usually a difficult task; what number ever novel styles square measure planned, the user desires demands far more optimized ones. religious text arithmetic is world notable for its algorithms that yield faster results, be it for mental calculations or hardware style. Power dissipation is drastically reduced by the utilization of Reversible logic. The reversible Urdhva Tiryakbhayam religious text number is one such number that is effective each in terms of speed and power. during this paper we have a tendency to aim to reinforce the performance of the previous style. the overall Reversible Logic Implementation price (TRLIC) is employed as AN aid to guage the planned style. This number may be with efficiency adopted in planning quick Fourier Transforms (FFTs) Filters and different applications of DSP like imaging, computer code outlined radios, wireless communications.

Index Term— Quantum Computing, Reversible Logic Gate, Urdhva Tiryakbhayam, Optimized Design, TRLIC.

I. INTRODUCTION

Vedic arithmetic is one in all the foremost ancient methodologies employed by the Aryans so as to perform mathematical calculations [2]. This consists of algorithms which will boil down massive arithmetic operations to straightforward mind calculations. The on top of aforementioned advantage stems from terribly fact|the actual fact} that religious text arithmetic approach is completely completely different and regarded very near the means a personality's mind works. The efforts place by Jagadguru Hindu Sri Bharati Krishna Tirtha maharajah to introduce religious text arithmetic to the commoners still as contour religious text Algorithms into sixteen classes [1] or Sutras must be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication rule that is standard for its potency in reducing the calculations concerned.

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With the advancement within the VLSI technology, there's AN ever increasing quench for moveable and embedded Digital Signal process (DSP) systems. DSP is ubiquitous in virtually each engineering discipline. quicker additions and multiplications square measure the order of the day. Multiplication is that the most simple and regularly used operations in an exceedingly electronic equipment. Multiplication is AN operation of scaling one range by another. Multiplication operations additionally type the premise for different advanced operations like convolution, separate Fourier remodel, quick Fourier Transforms, etc. With ever increasing want for quicker clock frequency it becomes imperative to possess quicker arithmetic unit. Therefore, DSP engineers square measure perpetually looking for new algorithms and hardware to implement them. religious text arithmetic may be capably used here to perform multiplication.

Another vital space that any DSP engineer should concentrate is that the power dissipation, the primary one being speed. there's continually a exchange between the ability dissipated and speed of operation. The reversible computation is one such field that assures zero power dissipation. therefore throughout the planning of any reversible circuit the delay is that the solely criteria that should be taken care of. In [12] a reversible Urdhva Tiryakbhayam number had been planned. This paper is AN extension of the previous work that tries to optimize the circuit planned in [12]. The paper is organized as follows: The section II provides the fundamentals of reversible logic together with the literature review. Section III explains the Urdhva Tiryakbhayam rule. The section IV describes the modifications of the previous style so as to evolve the optimized style. Section V compares the planned style with the opposite non religious text numbers still because the previous religious text number style and attracts a conclusion claiming the flexibility of Reversible Urdhva Tiryakbhayam multiplier.

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II. REVERSIBLE LOGIC

A. Literature Survey and Significance of reversible logic

Conventional combinative logic circuits square measure noted to dissipate heat for each little bit of data that's lost. this is often additionally evident from the second law of physics that states that any process results in loss of energy. Landauer showed that any gate that's irreversible, essentially dissipates energy, and every irreversible bit generates k*T ln2 joules of warmth wherever k is Boltzmann's constant (1.38 x 10-23 joules/Kelvin) and T is temperature in Kelvin. Lowering the brink voltage and management of the ability provide square measure wide applied practices to decrease the energy consumption in any operation . but these technologies of lowering the energy consumption can hit a barrier of kT . so as to alleviate this, techniques like reducing the temperature of pc and constructing a thermodynamically reversible pc may be used .

Frank analyzed that the second choice was a stronger alternative. once the temperature of the system reduces to temperature, the energy reduces 2 orders of magnitude however exploitation reversible computing there may be any additional reduction that matches with the theoretical worth. The cardinal feature of reversible computing is that electrical phenomenon on the cell consisting of semiconductor units isn't allowable to discharge throughout transistor switch . this could be reused through reversible computing and thus decrease energy dissipation. Bennett in 1973 showed that AN irreversible pc will continually be created reversible. Reversible logic circuits

naturally pay attention of heating since in an exceedingly reversible logic each input vector may be unambiguously recovered from its output vectors and thus no data is lost.

B. REVERSIBLE LOGIC GATES

A Reversible computer circuit is AN n-input n-output logic operate within which there's a matched correspondence between the inputs and also the outputs. This not solely helps to see the outputs from the inputs however additionally the inputs may be unambiguously recovered from the outputs. thanks to this bijective mapping the output vectors square measure just permutations of the input vectors.

Some of the fundamental reversible logic gates within the literature those square measure helpful in planning the Reversible Urdhva Tiryakbhayam number square measure the Richard Feynman Gate—the solely 2x2 gate, that's used for fan-out functions still as for complementing. it's a quantum price of 1. Peres Gate— a 3x3 gate that's accustomed manufacture AND operation still as EX-OR operation. it's a quantum price of 4. New Fault Tolerant gate (NFT) – is additionally a 3x3 gate with a quantum price 5. HNG gate that could be a 4x4 gate which will be effectively used as a full adder and provides minimum quantum price implementation. it's a quantum price of six. BVPPG could be a 5x5 gate with a quantum price of 10. All the mentioned gates square measure shown within the figure one.

C. optimisation parameters for reversible logic circuits

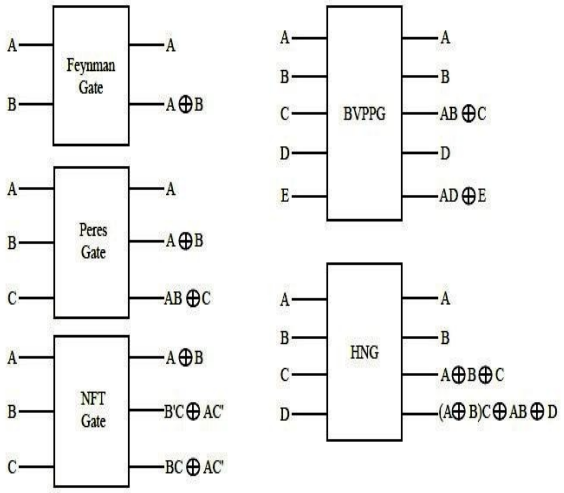

Figure 1: Reversible Logic Gates

The vital parameters [14] that play a significant role within the style of AN optimized reversible logic circuit square measure as listed:

Constants (CI): This refers to the quantity of inputs that square measure to be maintained constant at either zero or one so as to synthesize the given logical operate.

Garbage (GO): This refers to the quantity of outputs that aren't utilized in the synthesis of a given operate. These square measure terribly essential, while not that changeability can't be achieved.

Gate count (NG): the quantity of reversible gates accustomed understand the operate.

Flexibility: This refers to the catholicity of a reversible computer circuit in realizing additional functions.

Quantum price (QC): This refers to the value of the circuit in terms of the value of a primitive gate. it's calculated knowing the quantity of primitive reversible logic gates (1x1 or 2x2) needed to appreciate the circuit

Gate levels: This refers to the quantity of levels within the circuit that square measure needed to appreciate the given logic functions.

Total Reversible Logic Implementation price (TRLIC) : Let, in an exceedingly reversible logic circuit there square measure nanogram reversible logic gates, CI constant inputs, GO number of garbage outputs, and have a quantum price QC. Then the TRLIC is given as

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$$TRLIC = \sum(NG + CI + GO + QC) \ldots 1$$

III. URDHVA TIRYAKBHAYAM MULTIPLICATION ALGORITHM

Urdhva Tiryakbhayam (UT) could be a number supported religious text mathematical algorithms deviced by ancient Indian religious text mathematicians. Urdhva Tiryakbhayam Sanskrit literature may be applied to any or all cases of multiplications viz. Binary, Hex and additionally Decimals. it's supported the construct that generation of all partial product may be done and so synchronal addition of those partial product is performed. The similarity in generation of partial product and their summation is obtained exploitation Urdhva Tiryakbhayam. in contrast to different numbers with the rise within the range of bits of number and/or multiplier the time delay in computation of the merchandise doesn't increase proportionately. thanks to this truth the time of computation is freelance of clock frequency of the processor. thus one will limit the clock frequency to a lower worth. Also, since processors exploitation lower clock frequency dissipate lower energy, it's economical in terms of power issue to use low frequency processors using quick algorithms just like the on top of mentioned. The number supported this Sanskrit literature has the advantage that because the range of bits will increase, gate delay and space will increase at a slow pace as compared to different typical multipliers.

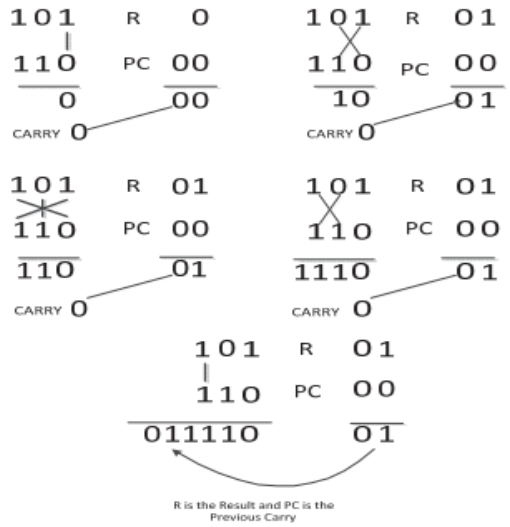

Figure 2: Urdhva Triyabhayam Procedure For Mult.

The Algorithm Implementation:

1.we are going to take the right-hand digits and multiply them along. this may provide US LSB digit of the solution.

2.Multiply LSB digit of the highest variety by the second little {bit of} all-time low variety and therefore the LSB of all-time low variety by the second bit of the highest variety. Once we've got those values, add them along.

3.Multiply the LSB digit of bottom variety with the MSB digit of the highest one, LSB digit of high variety with the MSB digit of bottom and so multiply the second little bit of each, and so add all along.

4.This step is analogous to the second step, simply move one place to the left. we are going to multiply the second digit of 1 variety by the MSB of the opposite variety.

5.Finally, merely multiply the LSB of each numbers along to urge the ultimate product.

IV. IMPLEMENTATION OF THE URDHVA TIRYAKBHAYAM MULTIPLIER

The conventional logic style implementation of a 2x2 Urdhva Tiryakbhayam number mistreatment the irreversible logic gates [8] could be a shown within the Figure three. In [12] the four expressions for the output bits square measure derived from this figure and is employed to get the reversible implementation as shown in Figure four. The circuit uses 5 Peres gates and one Feynman gate. This style encompasses a total quantum value of twenty one, variety of garbage outputs as eleven and variety of constant inputs four. The gate count is vi. This style doesn't take into thought the fan outs. the general performance of the UT number is

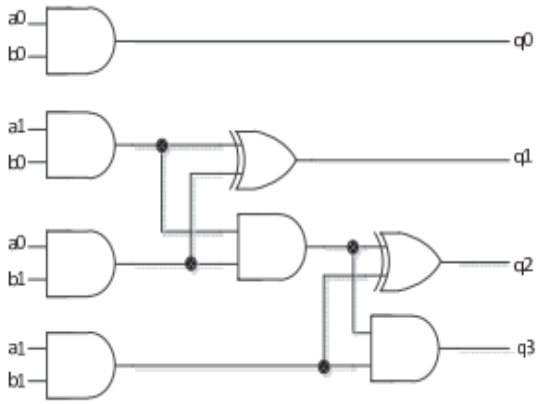

Figure 3: CONVENTIONAL 2X2 UTM

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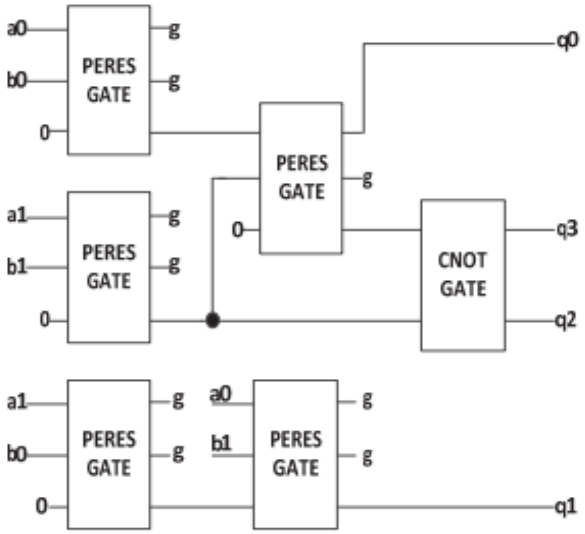

Figure 4: REVERSIBLE 2X2 UT MULTIPLIER

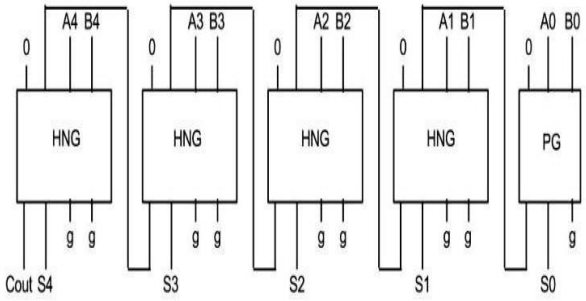

FIGURE 5: PROPOSED MODIFIED 5 BIT RIPPLE CARRY ADDER DESIGN

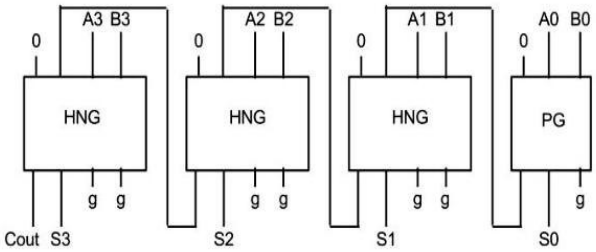

FIGURE 6: PROPOSED MODIFIED 4 BIT RIPPLE CARRY ADDER DESIGN

A. Improved 2x2 Urdhva Tiryakbhayam number

The design expressions may be logically changed thus on optimize the planning. The new style makes use of 1 BVPPG, 3 Peres gates and one Feynman gate. the planning additionally takes into consideration the fan outs. one in all the main style constraints of reversible logic is that the distribute, different being loops not permissible. this implies that the reversible logic circuit with multiple numbers of same inputs isn't best. a way out is to use a separate distribute generator or to make a circuit that inherently takes care of fan outs mistreatment the reversible logic gates employed in the planning. This style encompasses a quantum value of twenty three, variety of garbage outputs as five, variety of gates five and therefore the variety of constant inputs is five.

The reversible logic implementation of the above expressions requires four peres gate and one Feynman(CNOT) gate. The reversible logic implementation of 2X2 UT multiplier is shown in the Fig8 The quantum cost of the 2X2 Urdhva Tiryakbhayam Multiplier is found to be 21.The number of garbage outputs is 9 and number of constant inputs is 4.
The partial products generated using the 2X2 UT multiplier are need to be added using the four bit adder.The four bit ripple carry adder unit was designed using the HNG reversible gate. The four bit ripple carry adder unit.

V. RESULTS AND COMPARISONS

The design of the reversible 2x2 and 4x4 multipliers is logically verified mistreatment XILINX nine.2i and MODELSIM. The simulation results square measure as shown in figures ten and eleven severally. the subsequent square measure the necessary style constraints for any reversible logic circuits.

1.Reversible logic circuits ought to have minimum quantum value.

2.The planning may be optimized thus on turn out minimum variety of garbage outputs.

3.The reversible logic circuits should use minimum variety of constant inputs.

4.The reversible logic circuits should use a minimum variety of reversible gates.

Since TRLIC is that the total of of these desig n parameters, it's commendable to possess a least price of TRL IC. The planned style of Reversible UT multiplier factor is compared with as several as eleven completely different outstanding multiplier factor style s within the literature in terms of Quantum price, garbage outputs,

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range of gates, range of constant inputs and additionally in terms of TRLIC values. This additionally includes a comparison with our ow n previous style and therefore the optimisation is clearly evident from the table of Comparison as shown in table one.

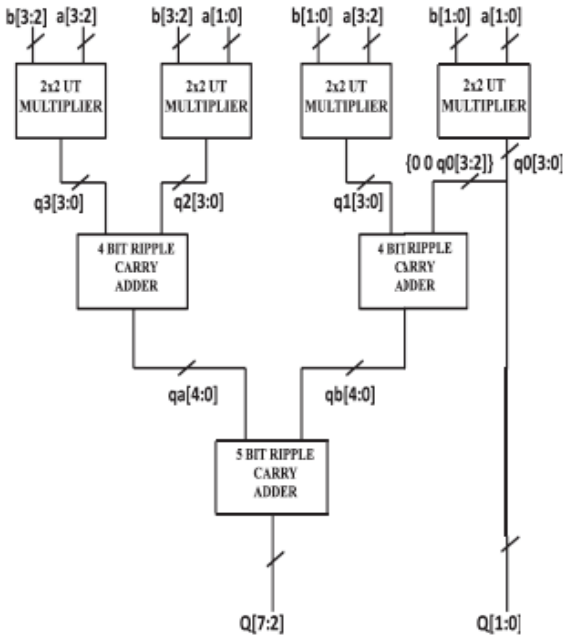

FIGURE 7: BLOCK DIAGRAM OF 4X4 UT MULTIPLIER

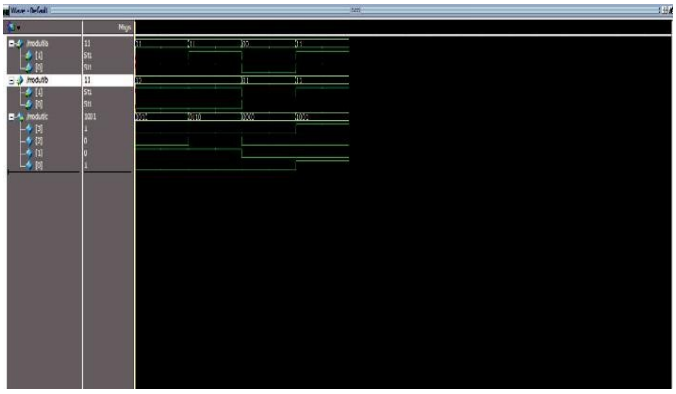

FIGURE 8: SIMULATION RESULTS FOR 2X2 UT MULTIPLIER

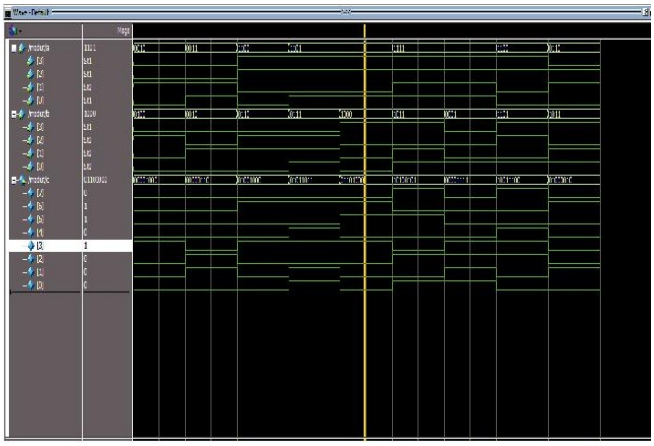

FIGURE 9: SIMULATION RESULTS FOR 4X4 UT MULTIPLIER

substantial decrease within the num ber of garbage outputs (from nine to five and four severally in styles one and 2) and therefore the gate count values (from six to five in each the designs). additionally there's a discount within the quantum price of all the ripple carry adders by a pair of attributable to the structural modifi ion involving replacement of 1st HNG gate by a Peres Gate and reduction in garbage output by one attributable to the SAM e reason. Therefore, notwithstanding the quantum price has exaggerated slightly, the decrease within the garbage outputs AND circuit count have completely invalidated its impact. The minimum improvement within the TRLIC is at five.86% that is with relevancy [12] and th e most improvement stand high at thirty three.6% w.r.t [22]. Als o from the table it's clear that each planned styles have a minimum gate count further as minimum garbage outputs as compared to all or any alternative multipliers studied here. the amount of constant inputs is healthier than ten of the eleven styles. so we have a tendency to c Associate in Nursing say that the look is extremely abundant optimized as compared to others studied here.

CONC LUSIONS

The focus of this paper is especially to style an occasional power high speed multiplier factor that is finished by constructing the multiplier factor exploitation reversible logic gates. T he procedure is applied thus on yield Associate in Nursing optimized style as compared to those within the literature. The potency of a reversible logic circuit is characterised in terms of parameters like quantum price, range of constant inputs, garbage outputs and range of gates used to comprehend the logic implementation. Lower the worth of those parameters additional economical is that the style. In [12] parameter

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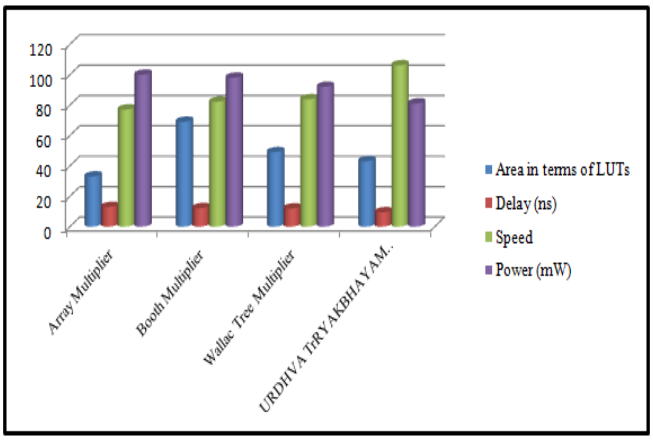
referred to as TRLIC had been planned that is outlined as total of all price metrics of the given style. The quantum price could be a parameter that dire ctly reflects the delay of the quantum circuit. additionally lower TRLIC implicitly suggests that lower the quantum price, therefore low er is that the delay and the other way around. Besides ingestion the look criterion that fan-out should be generated inside the circuit, th e planned styles additionally scale back the TRLIC as compared to the antecedently planned style [12]. The more optimisation of the circuit in terms of the full logical prices is beneath progress and is taken as future work.

COMPARISON OF VARIOUS TECHNIQUES

PARAMETERS	EXISTING MULTIPLIER TECHNIQUES			PROPOSED MULTIPLIER TECHNIQUE
	Array Multiplier	Booth Multiplier	Wallace Tree Multiplier	URDHVA Tiryakbhayam Multiplier
Area in terms of LUTs	33	69	49	43
Delay (ns)	12.971	12.176	11.926	9.418
Speed	77.09	82.12	83.85	106.17
Power (mW)	100	98	92	81

GRAPHICAL COMPARISON



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