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DESIGN AND IMPLEMENTATION OF LOW POWER MODIFIED BOOTH MULTIPLIER FOR DSP UNIT

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Abstract: This paper presents a low power digital signal processor (DSP) unit which is based on booth algorithm. Multiplication and accumulation are the most important DSP operations. In this paper we implemented a multiplication accumulation unit (MAC) using booth encoder. In booth encoder and accumulation section carry save adder (CSA) is used for fastest implementation.

Keywords: modified booth algorithm (MBA), multiply-accumulator (MAC), carries save adder (CSA), booth encoder, Wallace tree.

I. INTRODUCTION

A Multiplier is the most important component in Digital Signal Processors and general purpose microprocessors. In most of scientific and engineering applications multiply accumulation is needed rather than simple multiplication. The speed of processor mainly depends on the speeds of the multiplier unit, because multiplication is most time consuming process.

In VLSI design process three important considerations are to minimize the power and area, then efficiently increase the speed of operations. Area and speed are conflicting constrains in such a way that, improving speed may cause increased area.

Booth‘s Algorithm is a best method for multiplying signed numbers. In this approach

This paper is organized as II. Booth Algorithm III.MAC unit using Modified Booth multiplier IV .Results V. conclusion

II. Booth Algorithm

In Booth encoding methods number of partial product is reduced. The purposed algorithm can be used to achieve a low power conception and high speed of operation.

In radix-4 booth algorithm we are encoding the multiplier bit as shown below.

Steps are,

1. Sign bit position can be extended one position if necessary to ensure n is even.

2. Add a '0' to the right hand side of the LSB of multiplier.

3. Group the multiplier bit according using overlapping technique as a shown in fig.1 below.

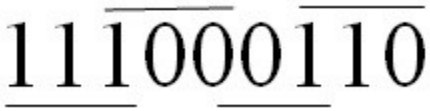

Fig.1. Overlapping

4. According to the value of each group we can make the partial product using Booth Encoding table.

Groups	Partial product
000	0
001	1*multiplicand
010	2* multiplicand
011	2* multiplicand
100	-2*multiplicand
101	-2*multiplicand
110	-1*multiplicand
111	0

Table 1.Booth encoding Table

5. After finding all partial products. We can add the partial product using carry save adder.

III. MAC unit using Modified Booth multiplier.

The multiplier and accumulator are the essential component digital signal processing and image processing. This type system needs filtering, convolution. For this MAC is operation important.

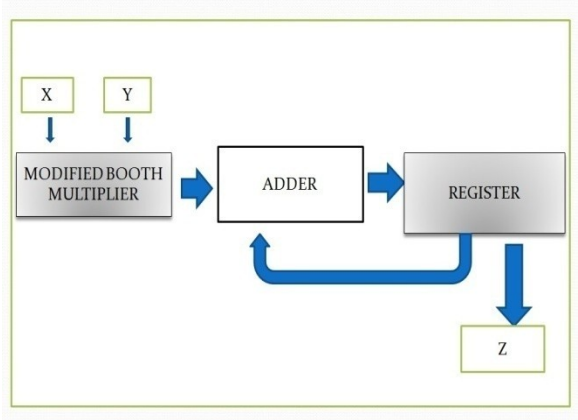

Fig.2.MAC unit

Block diagram of proposed MAC unit shown in fig.2 Main blocks the block diagram are Modified booth multiplier, adder and register.

A. Modified Booth Multiplier

Modified Booth multiplier is the heart of the MAC unit. The steps involved in the proposed modified booth multiplier are illustrated in the fig.3.

The steps involved are,

1. Finding the partial product using radix-4 booth algorithm. This is done by the booth encoder.

2. Before adding the partial product we are arranging it as Wallace tree formation.

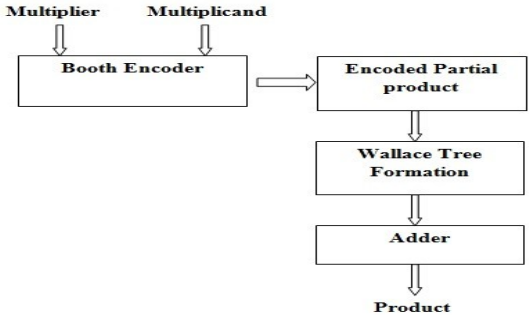

Fig.3. Modified Booth Multiplier

Wallace tree formation is an adder tree designed for high speed partial product addition. Carry save adder, half adder, full adder are used in Wallace tree formation to reduce the partial products. Carry save adder will increases the speed of summation. Wallace tree formation using carry save adder is illustrated in the fig 4.

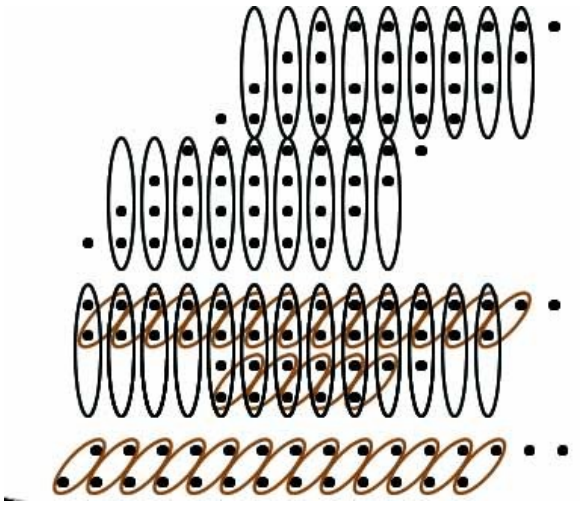

Fig.4. Wallace tree formation

3. After Wallace tree formation propagate adder use finally used for addition.

B. Register and adder

In multiplier accumulation after getting the product result we should accumulate or store it. For this purpose we are created register. This register together works with adder to accumulate the result

V.RESULTS

The simulation results MAC unit using modified booth algorithm is shown fig 5, 6 and comparison of modified booth multiplier and without modification is shown table 2.

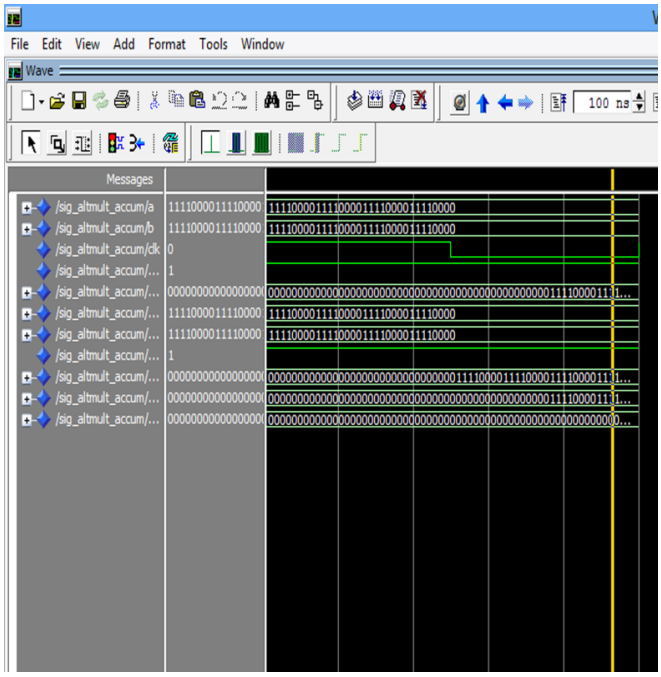

Fig.5. Simulation MAC of unit

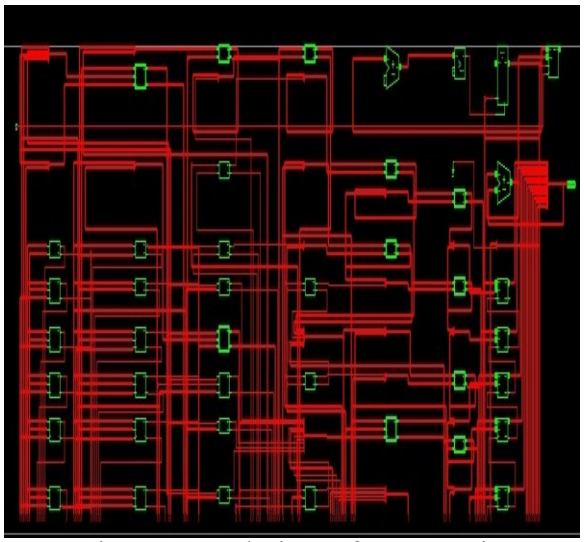

Fig6. Internal view of MAC unit

Multiplier	Area (no of gates used)	Delay (ns)	Power (mw)
Booth without modification	175	28.146	254
Modified Booth	143	21.142	198

Table.2. Comparison of Multiplier for area, delay and power

CONCLUSION

Here implemented a lower power DSP unit based on modified booth algorithm. Modified booth multiplier gives better performance in area, power and speed. Main advantage of the system is its dynamic power saving. Further work can be extended by employing high radix booth algorithm for partial product generation. Expected result will be reduced no of partial products, reduced area, power and delay.

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