An Efficient Adiabatic 2:1 Multiplexer Design Approach for Low Power Applications

Gurpreet Kaur, *Narinder Sharma*
Electronics & communication Department
Amritsar College Of Engineering And Technology

Abstract:-In this paper authors have compared two adiabatic logic designs with conventional CMOS.A 2:1 multiplexer are implemented by these techniques and results are compared such as power dissipation, rise time ,fall time.transistor count and maximum frequency.The designing of schematic and simulation of these logics done on TANNER v7.From results it is found that power consumption of PFAL logic is less as compare to ECRL and CMOS.

***Keywords:*CMOS,Adiabatic,ECRL,PFAL,T-SPICE,ECRL and PFAL 2:1Multiplexer.**

I. INTRODUCTION

As in designing of conventional complementary metal–oxide–semiconductor (CMOS) logic, the power dissipation directly change with the variation in supply voltage. Thus, reduction in power supply voltages is one of the main method to reduce power dissipation . In digital circuits , power consumption is minimize by by recycling its energy from capacitive load.That's called adiabatic approach.Adiabatic method consist of sinusoidal voltage or ramp voltage which is used to recycle back the energy which is stored on capacitor. There are two methods for adiabatic switching.One is partial and another is full adiabatic method.Authors design 2:1 multiplexer using ECRL,PFAL and compare with Conventional CMOS.

In section 2,need for low power and concept of adiabatic or energy recovery principle are discussed. Section 3,Overview of adiabatic families and discussed the working of ECRL and PFAL logics.Section 4, Designing of 2:1 Multiplexer using Conventional CMOS and Adiabatic techniques ECRL and PFAL.Section 5, Simulation waveforms of 2:1 Multiplexer are shown.Section 6,Results are shown include graphs and tables. Section 7, future scope is also given.

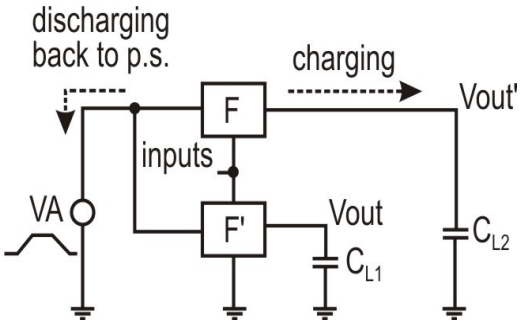
2.MOTIVATION

2.1.Need For Low Power

In VLSI designing,low power is main contributor which increase the demand of low power consumer devices. The INTEL 4004 microprocessor designed using 2300 transistor and power consumption upto one watt and its operating clock frequency is 1MHZ.In 2001,Pentium processor was designed by using 42 million transistors.Its power consumption was 65W with operating clock frequency is 2.40GHZ. All consumer electronics industry depend on batteries.Batteries consume more power so this power is to be minimized and essential.[1] .Consequently ,small ,light in weight and reliable products can be designed by low power technology.

2.2 ENERGY RECOVERY PRINCIPLE

Energy recovery principle is the thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat .Instead of using a separate power supply for VDD and for clock, the clock signal can be reshaped and be used for both the purposes. This clock signal is called power-clock. Dynamically adjusting the power-clock voltage to comply with constant-current charging results in adiabatic-charging effect. A ramp type power-clock supply VA. The power-clock voltage may be sinusoidal signal also. The power clock supply charges the load capacitor adiabatically during the time it is ramping up and allows the load capacitor energy to recycle back when it is ramping down. This adiabatic cycling of energy between the logic circuit load and the power clock supply needs an adiabatic path[2]. It is possible to have the same path for charging and discharging, called as temporal or trivial reversibility. Adiabatic circuit may have separate paths for charging and discharging .



.

Fig.1:Adiabatic(Energy recovery principle)

ISSN: 2278 – 909X

3. ADIABATIC LOGIC FAMILY

Practically adiabatic method broadly categorized as partial adiabatic and full adiabatic .In a partial adiabatic method, partial part of total energy is transferred to the ground level and in full adiabatic method, whole energy is recycled to the threshold voltage.There is no loss of energy . But due to this ,full adiabatic circuits have less operating speed and synchronization problems.

3.1Partial adiabatic methods are:

- Efficient Charge Recovery Logic (ECRL)
- 2N-2N2P Adiabatic Logic
- Positive Feedback Adiabatic Logic (PFAL)
- NMOS Energy Recovery Logic (NERL)
- Clocked Adiabatic Logic (CAL)
- True Single-Phase Adiabatic Logic (TSEL)
- Source-coupled Adiabatic Logic (SCAL)

3.2Full adiabatic methods are:

- Pass Transistor Adiabatic Logic (PAL)
- Split- Rail Charge Recovery Logic (SCRL)[3]

3.1.1. ECRL Technology

ECRL stands for efficient charge recovery logic.It has a latch of cross-coupled PMOSFETS . The basic construction of ECRL is matched with cascade voltage switch logic (CVSL).It has two PMOSFETS which are connected back to back like out/ is gives the input to m2 and out gives the input to m1. For logic operation,F n-tree and F/ n-tree blocks are used[4].
A ramp or pulse voltage is applied to the circuit and in ECRL ,it will be recycled back to the main supply.Two outputs out and out/ are used to describe the condition of ECRL operation. An oscillations are occurred due to the PMOSFETS switches works in pre-charge and recoverable states.There is irreversible condition because of thresholding of PMOSFETS in pre-charge and recoverable states[5]. When ramp voltage and threshod voltage are equal then PMOSFETS will be in off condition.

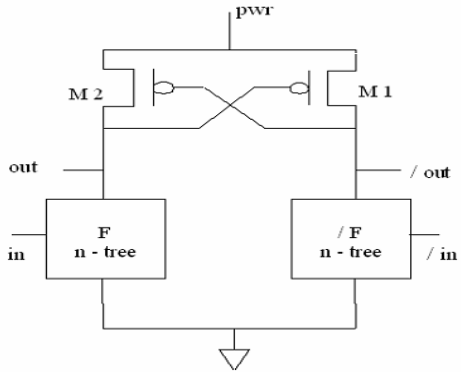


Fig.2:ECRL Logic Circuit."

3.1.2.PFAL Technology

PFAL stands for positive feedback adiabatic logic.This circuit has less power consumption. It is partial adiabatic method with dual railing[6]. PFAL basic circuit is given below Fig.3. Adiabatic amplification is necessary for PFAL. PFAL latch consist of 2 PMOSFET'S m1 and m2, 2 NMOSFET'S m3 and m4 .PFAL minimize the deterioratization on the outputs out and out/. It gives full swing . like transmission gate technology, the logic F and F/ tree are in parallel with PMOSFET'S. F and F/ functions handles the logic inputs. To compare the ECRL and PFAL ,the main differentiation is that PFAL latch consist of two PMOSFET'S and two NMOSFET'S instead of two PMOSFET'S and logic inputs NMOSFET'S are in parallel with PMOSFET'S.consequently,resistance offered is lesser as compare to ECRL circuits[7].

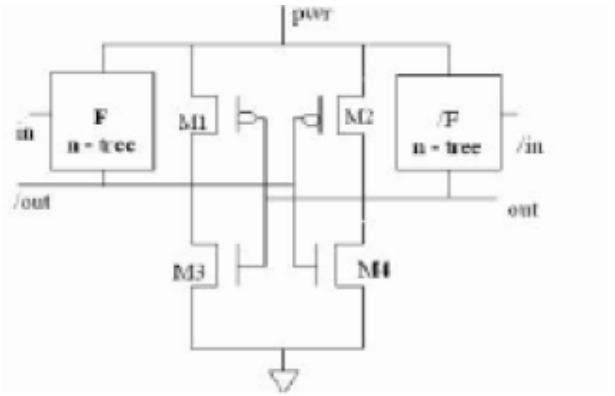


Fig.3:PFAL Logic Circuit."

Thus the equivalent resistance is smaller when the capacitance needs to be charged.

4.CIRCUIT

Multiplexer circuit:

4.1.2:1 Conventional CMOS multiplexer:

A circuit that generates an output that exactly reflects state of one of a number of data inputs, based on value of one or more control inputs is called "multiplexer". A multiplexer with two data inputs is referred as "2-to-1 or 2:1" multiplexer[8]. Commonly used circuit and graphical symbol for 2:1 multiplexer is shown in Circuit and Graphical symbol of 2:1 Multiplexer Logic expression for multiplexer output is given below figure 4.

$F = \hat{S}\, x1 + S\, x2$ 5

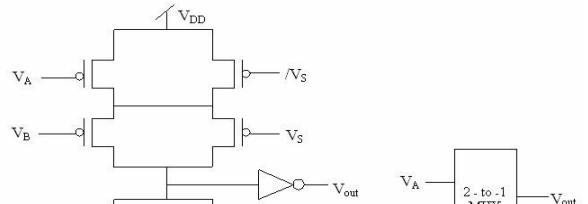


Fig.4: The Basic Structure of an 2:1 CMOS Multiplexer.

4.2.2:1 multiplexer using ECRL logic:

The advantage of ECRL is in its logic density that is achieved by elimination of large PFETS from each logic function. All functions are implemented using NFETS only, and PFETS serve only as the pull-up devices. ECRL circuit can be divided into two basic parts: A differential latching circuit and a cascaded complementary logic array [9]. The latch in these logic circuits is realized with two cross-coupled PMOS transistors. The cascade complementary logic array is realized with a NMOS logic tree .

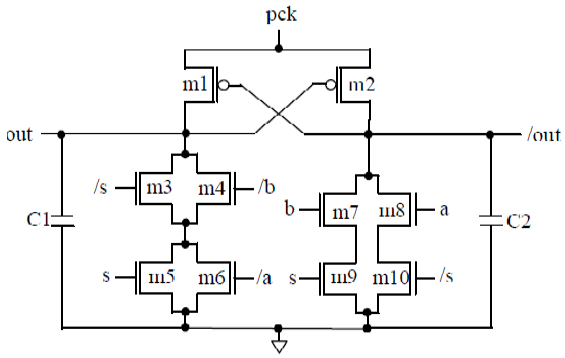


Fig.5:.2:1 Mux Using ECRL Logic.

4.3.2:1 multiplexer using PFAL logic:

An adiabatic PFAL two-to-one Multiplexer can be implemented 0.18 µm technology.It implements the function F = (A) (/S) + (B) (S). When the select (S) signal is low, it outputs the signal A and when the select (S) signal is high, it outputs the signal B[10].

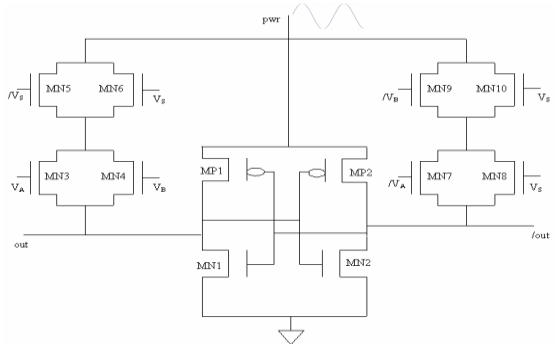


Fig.6:.2:1 Mux Using PFAL Logic.

5. SIMULATION

In this paper, two adiabatic and conventional CMOS logic styles,were used to design 2:1 multiplxer.These multiplexer were design on s-edit of tanner tool on 180nm technology.Figures shows schematics of multiplexers designed using two logic styles.

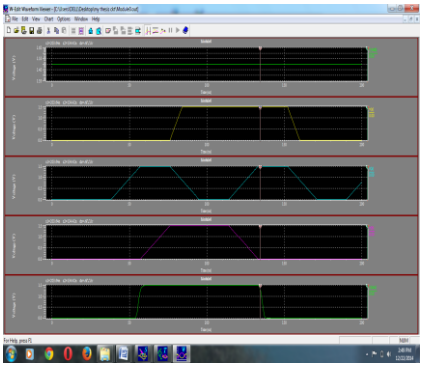


Fig.7: Simulated Waveform Of 2:1 CMOS multiplexer.

Fig.7shows the simulated waveforms of 2:1 CMOS multiplexer , where the bottom one signal is output signal and the Uppermost three signals are output .

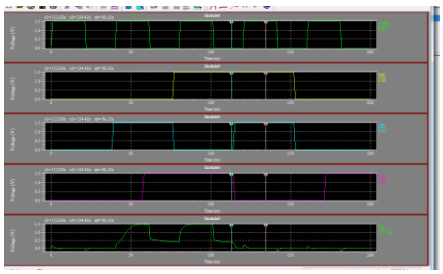


Fig.8: Simulated Waveform Of 2:1 multiplexer Using ECRL.

Fig.8shows the simulated waveforms of ECRL 2:1 multiplexer , where the bottom one signal is output signal and the Uppermost three signals are output .

ISSN: 2278 – 909X

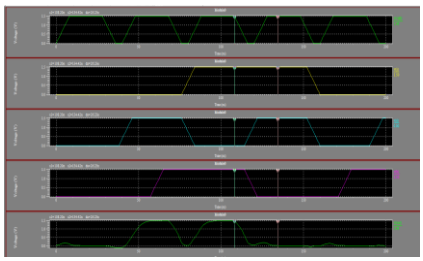


Fig.9:Simulation results Of 2:1Multiplexer Using PFAL.

Fig. 9 shows the simulated waveforms of 2:1 multiplexer using PFAL,where the bottom one signal indicate output while the top three signals are inputs.

6. RESULTS

This section deals with the comparison of the CMOS logic style with the adiabatic logic style in terms of the average dynamic power dissipation, rise time and fall time.The 2:1 multiplexer was simulated on tanner v7 in 180nm technology.

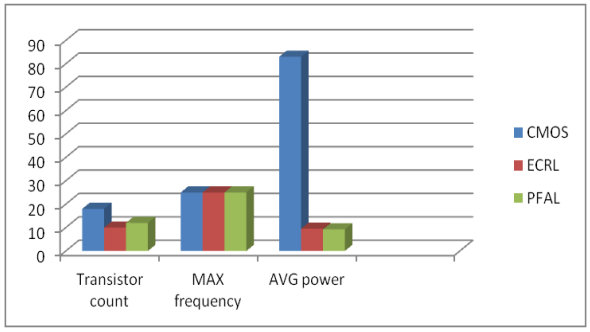


Fig.10:Graph For Transistor Count,MAX Frequency and Average Power For 2:1 Multiplexer.

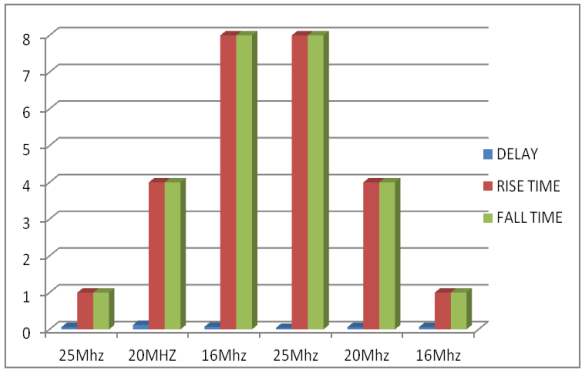


Fig.11: Graph For Delay,Rise Time and Fall Time For Two-To-One Multiplexer(ECRL and PFAL).

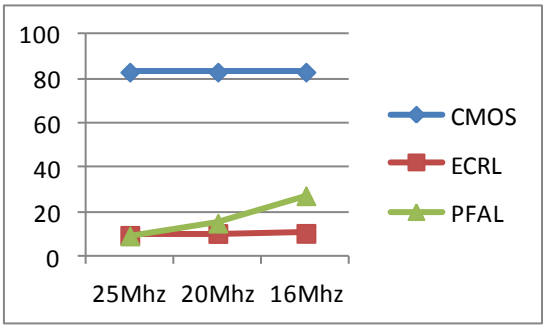


Fig.12: Avg. power verse Frequency For 2:1 Multiplexer.

Table1:Power dissipation results for various circuits with Frequency

Table 1 shows power dissipation of adiabatic circuits and conventional circuit.so dissipation in adiabatic circuit is less compared to conventional circuits.

FREQUENCY	2:1MUX(CMOS)	2:1MUX(ECRL)	2:1MUX(PFAL)
16 MHZ	83uw	10.42 uw	27.35 uw
20 MHZ	83uw	10.36 uw	15 uw
25 MHZ	83uw	9.53uw	9.24uw

Table2:Averagepowerdissipated,max.frequency,transistor count of cmos family and adiabatic ECR and PFAL family for 2:1 multiplexer.

Table 2 shows the comparison of CMOS ,ECRL and PFAL in terms of transistor count,max. frequency and average power dissipated.

Parameters	CMOS	ECRL	PFAL
Transisitor count	**18**	**10**	**12**
MAX.frequency	**25mhz**	**25mhz**	**25mhz**
AVG.power	**83uw**	**9.53uw**	**9.24uw**

Table3: Delay,rise time and fall time of cmos family and adiabatic ecrl and pfal family for 2:1 multiplexer for different power clockfrequencies.

Table 3 shows the parameters like delay,rise time and fall time which are used in simulation.

ISSN: 2278 – 909X

Frequency	DELAY	RISE TIME	FALL TIME
25Mhz	0.06	1	1
20MHZ	0.12	4	4
16Mhz	0.07	8	8
25Mhz	0.04	8	8
20Mhz	0.06	4	4
16Mhz	0.06	1	1

7.FUTURE SCOPE

Authors have implemented the 2:1 multiplexer adiabatic techniques ECRL and PFAL and compare with Conventional CMOS on 180nm technology.In this analysis, it is investigated that the PFAL has the highest level of power reduction of 9.43uw whereas in ECRL with lowest level of power reduction of 9.53uw at adiabatic logic level but bothe techniques have less power consumption as compare with CMOS. All the parameters are computed on Tanner Tool at 180 nm Technology at 1.5V supply voltage. A 4:1 Multiplexer can be design by adiabatic techniques for further usage in applications such as Memory Designing, in high performance low power circuits and various high end processors.

References:

[1] Arun Kumar and Manoj Sharma ,"Design and Analysis of mux using adiabatictechnique ECRL And PFAL"International Conference On AdvancesIComputing,Communications And Infomatics 2013.

[2] A.G.Dickinson and J.S.Denker,(1995) "Adiabatic Dynamic Logic," IEEE. Journal of Solid-state Circuits, Vol. 30 No.3, pp 311-315.

[3] V.G.S.Rajendra Prasad and Y. Sunil Gavaskar Reddy, "POWER COMPARISONOF CMOS AND ADIABATIC FULL ADDER CIRCUITS" IEEE Journal of Solid state Circuits, Vol. 27, No. 5, pp 840-844.

[4] W. C. ATHAS, J. G. KOLLER, L. SVENSSON, "An Energy- Efficient CMOS Line Driver using Adiabatic Switching," Fourth Great Lakes symposium on VLSI, California, March 2005.

[5] A. P. CHANDRAKASAN AND R. W. BRODERSEN, Low-power CMOS digital design, Kluwer Academic, Norwell, Ma, 1995.

[6] A.Blotti And R. Saletti, "Ultralow- Power Adiabatic Circuit Semi-Custom Design" IEEE Transaction on VLSI system, vol. 12, no. 11, pp. 1248-1253, November 2004.

[7] Y. Moon and D. K. Jeong, "An Efficient Charge Recovery Logic Circuit," IEEE JSSC ,Vol.31, No. 04, pp. 514-522, April 1996.

[8] B.Yasoda and S.Kaleem basha, "Performance Analysis of Energy Efficient and Charge Recovery Adiabatic Techniques for Low Power Design" IOSR Journal of Engineering Vol. 3, Issue (June. 2013).

[9] Arjun Mishra and Neha Singh, "Low Power Circuit Design Using Positive Feedback Adiabatic Logic" International Journal of Science and Research (IJSR) (2012).

[10] Priyanka and Veena Rani, "Design and Analysis of 2:1 Multiplexer Using Low Power Adiabatic Technique and Its Application in Nibble Multiplexer" IJSRD - International Journal for Scientific Research & Development| Vol. 2, Issue 05, 2014.

Gurpreet kaur ,Student, is currently Pursuing her M.Tech, in ECE department of Amritsar collegeof Engineering and Technology,Amritsar. She has completed her B.Tech degree in Electronics and communication engineering from shiv Shankar institute of engineering and technology ,patti,Amritsar in 2010.She was a lectuer in Guru Gobind Singh group of institutes,Bathinda from 2010 to 2012. At present , She is working as lecturer in Satyam group of institutes, Amritsar.Her research interest include digital signal processing,VLSI and Analog communication.

ISSN: 2278 – 909X