Testing SOC by Using Reconfigurable Compression Techniques

V.VINOTHINI, S.YAMUNA

Abstract— **The main aim of this project is used to reduce the test data volume and test application time by using hybrid compression technique. Today the silicon densities increase day by day, so it become very difficultly to test SOC, because it need the large test pattern. To minimize on-chip storage besides testing time, the test data volume is first reduced by compaction in a hybrid manner. The method consists of two steps: Burrow wheeler transform (BWT) and Huffman coding method. The method uses a set of adaptive coding techniques for realizing lossless compression. BWT is mainly used for the full scan chain method. BWT is a block sorting lossless and reversible data transform. It improves the efficiency of text compression algorithm. The hybrid based compression scheme provides the high compression ratio and fast testing time. It adapts any coding efficiency of compression ratio. Testing SOC by using reconfigurable compression techniques. Huffman coding achieves the accuracy in high rate.**

Index Terms— **Automatic Test Equipment (ATE), Burrows–Wheeler Transformation (BWT), Design-For-Testability (DFT), Huffman Coding, Intellectual property (IP) core, System-On-Chip (Soc) Test.**

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I. INTRODUCTION

An important objective to realize through elaborate testing of very large scale integration (VLSI) circuits and systems is to ensure that the manufactured products are free from defects and simultaneously guarantee that they meet deemed specifications.

In addition, the information collected during the test process may help in an increase of the product yield by improving the process technology with consequent lowering of the production cost. The integrated circuit (IC) fabrication process involves various steps, viz., photolithography, printing, etching, and doping. Testing SOC is very complexity because soc contain many IP cores. An SOC often includes multiple types of circuitry, such as digital logic, memories, and analog circuitry To reduce the complexity of testing use the hybrid test vector compression to minimize the test data volume and testing time by using the two method BWT(Burrow Wheeler Transform) and Huffman coding.

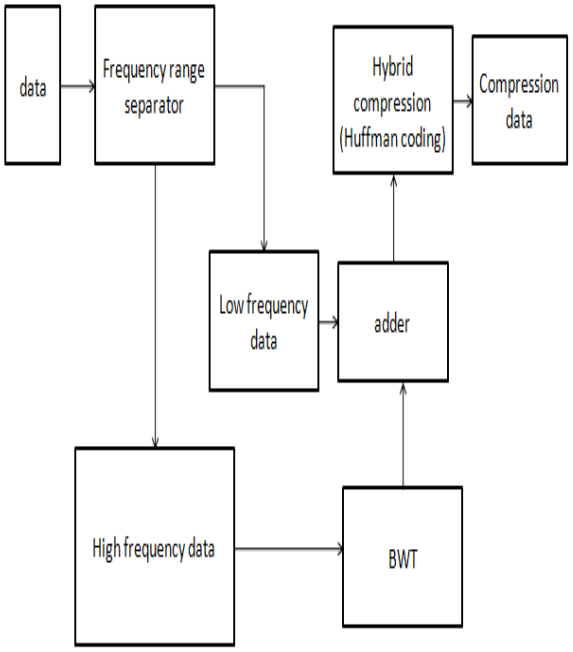

Fig. 1. Block diagram of the proposed method.

As shown in Fig. 1, LFSR is generates the test pattern. Test vector size is large. Frequency range separator is used to separate the data into two frequency that is low frequency data and high frequency data. High frequency data that contain many non-matching pattern. The BWT is used to create more matching pattern. The two frequency data is added then the data is compressed by Huffman coding.

II. PROPOSED METHODOLOGY

Fig.1 shows the block diagram of the developed technique. All the test vectors required for testing an SoC are first compressed in software mode. The compressed test vectors and an efficient decompression program are then loaded into the embedded processor core of the SoC The processor executes the decompression program and then applies all the uncompressed original test vectors to each and every core of the SoC for generating and analyzing the output responses. In the execution of the proposed technique, the undernoted four steps are involved.

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V.Vinothini, *M.E(VLSI DESIGN), Sri Shakthi Institute Of Engineering And Technology.Madurai,India,*
S.Yamuna, *Assistant professor, Sri Shakthi Institute Of Engineering And Technology, Coimbatore, India*.

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A. Division of Test Data Into Blocks

All the test vectors are divided into several blocks of equal size; the size of a block depends on the total number of bits in each vector.

Block number	1	2	3	4	5	6	7
Vector 1	0100	1100	0001	1000	0110	1000	0111
Vector 2	0110			1011	0011		0101
Vector 3	0100	1001			0010		0010

Fig. 2. Original test vector divided into several blocks.

As shown in Fig. 2, test vector-1 has seven blocks of size four bits each. The test vector-2 also has seven blocks of the same size but all the bits in its second, third, and sixth blocks are the same as that in the test vector-1.Similarly, the third, fourth, and sixth blocks in the testvector-3 are the same as in the test vector-2. If we have the information of the first, fourth, aft, and seventh blocks in the test vector- 2 along with the reference test vector-1, then, we can easily compute the entire set of test vector-2. One of the test vectors is then considered as a reference test vector and the next test vector is generated from the previous vector by storing only those blocks that differ from the previous one

B. Frequency Computation of Data Blocks

On completion of this block matching process, the high frequency and low frequency blocks are separated for further computation (viz., high frequency groups such as data sets in columns 1, 5, and 7 and low frequency groups such as data sets in columns 2, 3, 4, and 6 in Fig. 2).

Block number	1	2	3	4	5	6	7
Vector 1	01XX	0XX0	X0X0	10XX	X1X1	0XX1	X0X1
Vector 2	01X0	01XX	X01X	10X1	0X1X	1XX0	0X01
Vector 3	0XX0	10X1	10X0	XX01	00XX	10X0	01X1

Fig .3. Original test vector divided into several blocks.

As shown in Fig. 3,there will be lots of unspecified data (represented by x for *don't care*) that appear in practical situations. Those data are redefined in such a way that we can maximize the frequency of data block.

There are 28 test data sets for three test vectors that are divided into seven blocks each. Since, there are only four data sets in block of data; we can have 16 possible combinations (viz., minterms) in each block. The frequency of a block is determined by analyzing the number of unspecified data in all the blocks. For example, the minterm 1001 is contained in block numbers 2, 4, and 7 in the test vector-1. The same minterm also appears in block number 4 of the test vector-2 and in block number 2 of the testvector-3, respectively. So, the frequency of 1001 in these sets of test vectors is determined as 5.

C. Preprocessing of High Frequency Data Blocks

The BWT algorithm is executed on all high frequency blocks of data. Burrows and Wheeler have

	F						L
S4	B	B	S	D	R	D	O
S5	B	S	D	R	D	O	B
S2	D	O	B	B	S	D	R
S0	D	R	D	O	B	B	S
S3	O	B	B	S	D	R	D
S1	R	D	O	B	B	S	D
S6	S	D	R	D	O	B	B

Fig. 4. Original set of strings (*S* 0) associated with the buffer

the details of a transformation function that opens the door to some revolutionary new data compression techniques.BWT converts a block of data into a format that is extremely well suited from the standpoint of data compression. The BWT is performed on an entire block of data, all at once. This transformation takes a block of data and rearranges them using a sorting algorithm known as lexicographical sorting. The detail of the sorting process is explained as follows using an example string DRDOBBS.

	F						L
S4	B	B	S	D	R	D	O
S5	B	S	D	R	D	O	B
S2	D	O	B	B	S	D	R
S0	D	R	D	O	B	B	S
S3	O	B	B	S	D	R	D
S1	R	D	O	B	B	S	D
S6	S	D	R	D	O	B	B

Fig.5 Set of strings after sorting.

As shown in Fig. 5,the resulting output block contains exactly the same data elements that it started with, but differing only in their ordering. This transformation is a reversible process, meaning thereby that the original ordering of the data elements can be restored with no loss of fidelity. Also, a block of data transformed by BWT can be compressed using any or a combination of standard techniques As shown in Fig. 5, the matrix is formed by rotating the original sequence of the string. Then, the matrix of Fig. 4is lexicographically sorted. After sorting, the set of strings is arranged, as shown in Fig. 5.

Algorithm

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Step 1: Sort source outputs in decreasing order of their probabilities.

Step 2: Merge the two least probable outputs into a single output of which the probability is the sum of the corresponding probabilities.

Step 3: If the number of remaining outputs is more than two, go to Step 1.

Step 4: Arbitrarily assign 0 and 1 as codeword for the two remaining outputs.

Step 5: If an output is the result of merger of two outputs in a preceding step, append the current codeword with a 0 and a 1 to obtain the codeword of the preceding outputs and repeat Step 5. If no output is preceded by another output in a previous step, stop.

Huffman coding approximates the probability for each character as a power of 1/2 to avoid complications associated with using a non-integral number of bits to encode characters using their actual probabilities. Huffman coding works on a list of weights $\{wi\}$ by building an extended binary tree with minimum weighted path length and proceeds by finding the two smallest ws, $w1$, and $w2$, viewed as external nodes, and replacing them with an internal node of weight $w1+ w2$.

III. SOFTWARE REQUIREMENTS

A. *Modelsim se 6.3f*

In this paper the Models SE 6.3f software is used for simulation and verification. Models is a verification and simulation tool for VHDL, Verilog, SystemVerilog, and mixed- language designs. ModelSim's architecture allows platform independent compile with the outstanding performance of native compiled code.

The basic simulation flow is given by working libraries, Compile design files, Load and run simulation, Debug results. ModelSim offers numerous tools for debugging and analyzing the design. The project flow for Modelsim is given by Create a project, add files to the project, compile the project, run the simulation, Debug the results

IV. RESULT

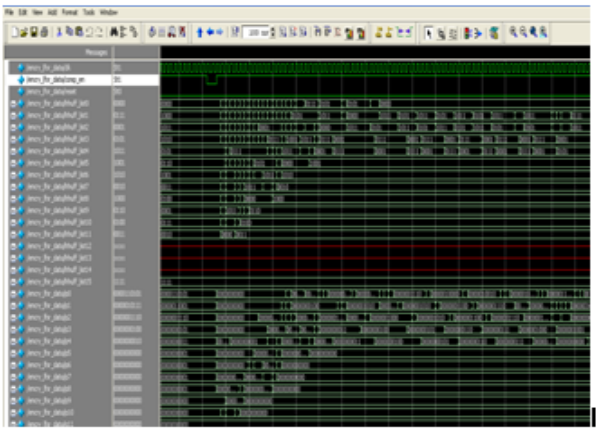

Fig.6 Encode LFSR output

V. CONCLUSIONS

The compression method presented herein is based on a hybrid technique that targets the unique characteristics of the block matching test data compression, BWT along with several coding algorithms on test data sequences. The BWT reduces the number of transitions for the test vector sequences, reduce the delay and test data volume size. Although, BWT involves a very complex method of computation and takes a longer time for compression, the reverse process is very simple and quite faster. It improves the efficiency of text compression algorithm. The hybrid based compression scheme that provides the high compression ratio and achieve the output with high accuracy. This technique achieved the high fault coverage. The activity of hybrid test data set is less than original test data.

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BIOGRAPHIES

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First Author.

V.Vinothini received the B.E. degree from Latha mathavan Engineering College Madurai, India in 2012 and doing Masters of Engineering in VLSI Design at Sri Shakthi Institute of Engineering and Technology, Coimbatore, India .Her research interests include Body Genetic Algorithm, VLSI Design, VLSI testing.

Second Author

D **S.Yamuna** received the B.E. degree from Tamilnadu College of Engineering Coimbatore, India, in 2012, the M.E degree from Sri Shakthi Institute of Engineering and Technology, Coimbatore, Indian in 2014.She is currently an Assistant Professor with the Department of Electronics and Communication Engineering, Sri Shakthi Institute of Engineering and Technology, Coimbatore. Her research interests include functional verification, VLSI Design, VLSI testing, and Low Power of VLSI Circuits.

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